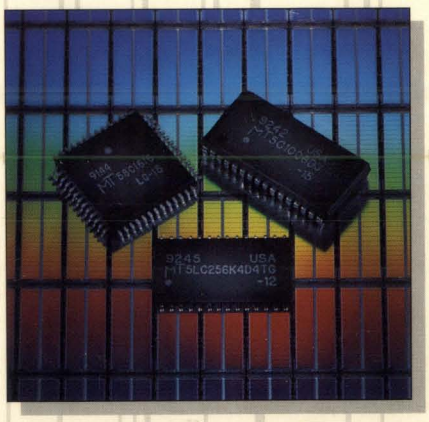
SRAM

1993 DATA BOOK



MICRON

SEMICONDUCTOR, INC.

MICRON

ABOUT THE COVER:

Front — A variety of features highlight Micron's SRAM product line, shown here against a circuitry backdrop rendered from a scanning electron microscope. Pictured are a 1 Meg SRAM wafer, 1 Meg SRAMs operating at 5 and 3.3 volts in SOJ and TSOP packages, and Micron's 16K x 16 Synchronous SRAM in a PQFP package.

Back — Micron's Boise, Idaho, headquarters.

IMPORTANT NOTICE

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice. Customers are advised to obtain the latest versions of product specifications, which should be considered in evaluating a product's appropriateness for a particular use. There is no assurance that Micron's semiconductors are appropriate for any application by a customer.

MICRON SEMICONDUCTOR, INC., MAKES NO WARRANTIES EXPRESSED OR IMPLIED OTHER THAN COMPLIANCE WITH MICRON'S SPECIFICATION SHEET FOR THE COMPONENT AT THE TIME OF DELIVERY. ANY CLAIM AGAINST MICRON MUST BE MADE WITHIN NINETY (90) DAYS FROM THE DATE OF SHIPMENT FROM MICRON, AND MICRON HAS NO LIABILITY THEREAFTER. ANY MICRON LIABILITY IS LIMITED TO REPLACEMENT OF DEFECTIVE ITEMS OR RETURN OF AMOUNTS PAID FOR DEFECTIVE ITEMS (AT THE BUYER'S ELECTION).

MICRON'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRON SEMICONDUCTOR, INC., AS USED HEREIN:

A. LIFE SUPPORT DEVICES OR SYSTEMS ARE DEVICES OR SYSTEMS WHICH (1) ARE INTENDED FOR SURGICAL IMPLANT INTO THE BODY, OR (2) SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS FOR USE PROVIDED IN THE LABELING CAN BE REASONABLY EXPECTED TO RESULT IN A SIGNIFICANT INJURY TO THE USER.

B. CRITICAL COMPONENT IS ANY COMPONENT OF A LIFE SUPPORT DEVICE OR SYSTEM WHOSE FAILURE TO PERFORM CAN BE REASONABLY EXPECTED TO CAUSE THE FAILURE OF THE LIFE SUPPORT DEVICE OR SYSTEM OR TO AFFECT ITS SAFETY OR EFFECTIVENESS.

Dear Customer:

Micron Semiconductor, Inc., is dedicated to the design, manufacture and marketing of high-quality, highly-reliable memory components. Our corporate mission is:

"To be a world class team developing advantages for our customers."

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX®, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And, when you have a design or application question, you can get the answers you need from the source through one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

ADVANTAGES

Micron Semiconductor brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on your expectations, including JIT programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron Semiconductor entered the memory market in 1978, first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and Triple Port DRAM), and a variety other memory products.

As we bring innovative memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. Micron's Triple Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the Triple Port's tradition. From FIFOs to programmable products, Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install 88-pin IC DRAM Card. Ideal for laptop, notebook and other portable systems, Micron's IC DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

MILITARY CERTIFIED PRODUCTS

As one of the few manufacturers of military-grade memory in North America, Micron is proud to provide a documented source inspection from wafer start to finished product. We've earned recognition from U.S. and European space agencies as well as Joint Army/Navy certification for both our NMOS and CMOS process technologies.

DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for commercial and military use in highly specialized applications. Micron's bare die products are available both in 6" wafers and singulated die form.

CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers value-added services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the component products you need are readily available.

QUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with every Micron shipment. We believe that quality must be internalized consistently at every level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program, the Micron Challenge, formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX® intelligent burn-in and test system** gives Micron a unique edge in product reliability.

*See NOTE, page v.
**For more information on Micron's AMBYX®, see Section 10.

ABOUT THIS BOOK

CONTENT

The 1993 *SRAM Data Book* from Micron Semiconductor provides complete specifications on all standard SRAMs and SRAM modules as well as specialty and derivative products based on our SRAM production process.

The *SRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes include our *DRAM Data Book* and *Military Data Book*. As our product lines continue to diversify, more data books will be released.

SECTION ORGANIZATION

Micron's 1993 *SRAM Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The Data Book is organized into 12 sections:

- **Sections 1–8:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 9:** Application/technical notes.
- **Section 10:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX* intelligent burn-in and test system.*
- **Section 11:** Packaging information.
- **Section 12:** Product ordering information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the SRAM section begins with the 16 Meg x 1 followed by 64 Meg x 1 and all other x1 configurations in order of ascending depth. Next come the x4 products, followed by x8, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either Advance, Preliminary or Final. In addition, product data sheets that are new additions are designated with a "New" indicator in the tab area of the front page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact:

Micron Semiconductor, Inc.
2805 East Columbia Road
Boise, ID 83706
Phone: (208) 368-3900
FAX: (208) 368-4431
Customer Comment Line:
800-932-4992 (USA)
01-208-368-3410 (Intl.)

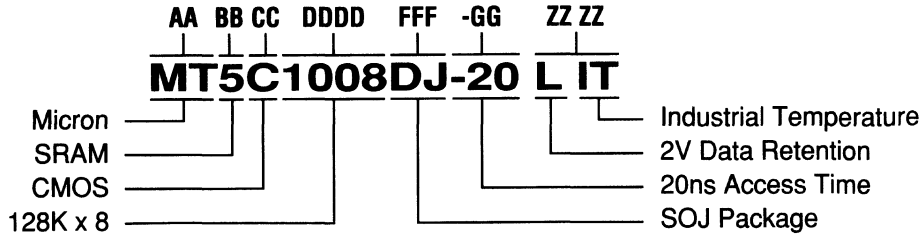
DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
"Advance"	This data sheet contains initial descriptions of products still under development.
"Preliminary"	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking (Final)	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
"New"	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the data book.

NOTE: Micron uses acronyms to refer to certain industry-standard-setting bodies. These are defined below for your reference:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council.
JEIDA—Japanese Electronics Industry Development Association.
PCMCIA—Personal Computer Memory Card International Association.

*Micron's *Quality/Reliability Handbook* is available by calling (208) 368-3900.

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM (VRAM)	42
TPDRAM	43
SRAM	5
FIFO	52
Cache Data SRAM	56
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM	Width, Density
DPDRAM (VRAM)	Width, Density
TPDRAM	Width, Density
SRAM	Total Bits, Width
CACHE	Density, Width
Latched SRAM	Total Bits, Width
FIFO	Width, Total Bits
Synchronous SRAM	Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required)

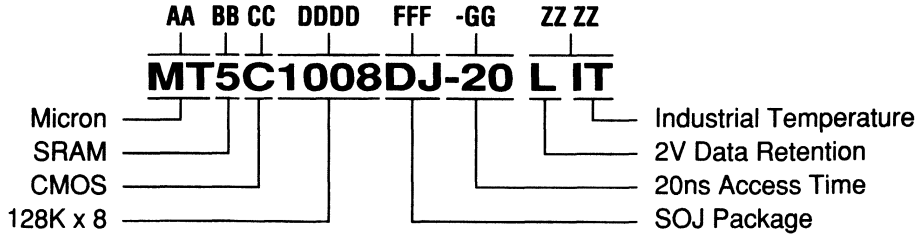
JEDEC Test Mode (4 Meg DRAM)	J
Errata on Base Part	Q

FFF – PACKAGE CODES

PLASTIC	
DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL
DIE	
Die	XDC†
Wafer	XWC†
Military Die	XDM†
Military Wafer	XWM†
Ceramic	
DIP	C
DIP (Narrow Body)	CN
DIP (Wide Body)	CW
LCC	EC
LCC (Narrow Body)	ECN
LCC (Wide Body)	ECW
SOP/SOIC	CG
SOJ	DCJ
PGA	CA
FLAT PACK	F

† A "1", "2" or "3" appears as part of the die identifier (e.g. XDM1.) A "1" indicates standard probe. A "2" indicates hot probe with speed grading. A "3" indicates that the die has been tested to meet all data sheet AC and DC parametrics as well as having gone through the full AMBYX® burn-in process.

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order).

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

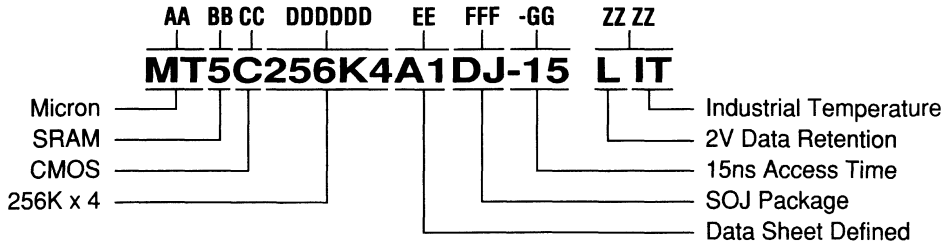
Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL

ZZ ZZ – PROCESSING CODES (continued)

Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP
Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape and Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM (VRAM)	42
TPDRAM	43
Synchronous DRAM	48
SRAM	5
FIFO	52
Latched SRAM	56
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory

No Letter	Bits
K	Kilobits
M	Megabits
G	Gigabits

EE – DEVICE VERSIONS

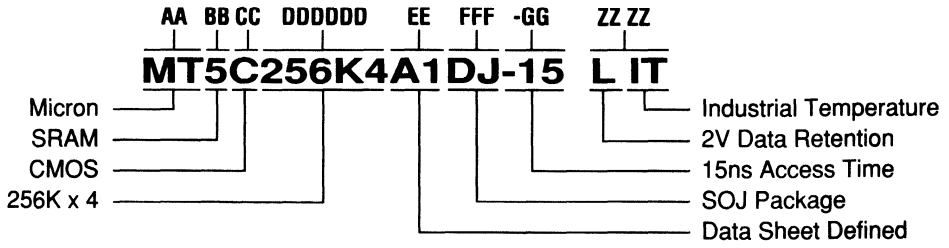
(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet

FFF – PACKAGE CODES

Plastic	
DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL
DIE	
Die	XDC†
Wafer	XWC†
Military Die	XDM†
Military Wafer	XWM†
CERAMIC	
DIP	C
DIP (Narrow Body)	CN
DIP (Wide Body)	CW
LCC (Narrow Body)	ECN
LCC	EC
LCC (Wide Body)	ECW
SOP/SOIC	CG
SOJ	DCJ
PGA	CA
FLAT PACK	F

† A "1", "2" or "3" appears as part of the die identifier (e.g. XDM1.) A "1" indicates standard probe. A "2" indicates hot probe with speed grading. A "3" indicates that the die has been tested to meet all data sheet AC and DC parametrics as well as having gone through the full AMBYX® burn-in process.

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:
V L IT

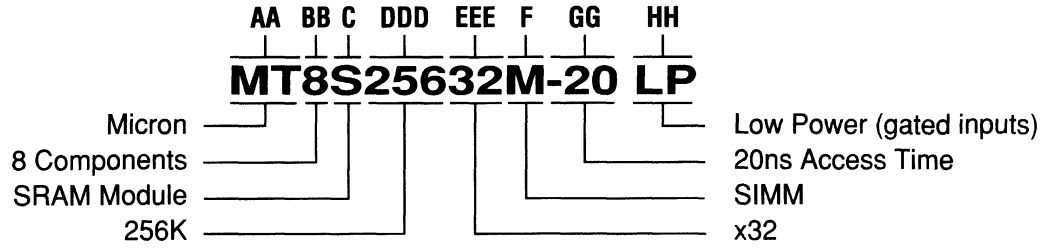
Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL

ZZ ZZ – PROCESSING CODES (continued)

Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP
Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape and Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
- SRAM ..... S
- DRAM ..... D

DDD – DEPTH

EEE – WIDTH

F – PACKAGE CODE
- DIP ..... D
- ZIP ..... Z
- SIMM ..... M
- SIP ..... N
- Gold SIMM ..... G

GG – ACCESS TIME
- -10 ..... 10ns
- -12 ..... 12ns
- -15 ..... 15ns
- -20 ..... 20ns
- -25 ..... 25ns
- -30 ..... 30ns
- -35 ..... 35ns

HH – SPECIAL DESIGNATOR
- Low Volt, Data Retention L
- Low Power (gated inputs) ..... LP

5V STATIC RAMS

CE ... CHIP ENABLE
LP ... LOW POWER, LOW VOLTAGE DATA RETENTION
OE ... OUTPUT ENABLE

3.3V STATIC RAMS

CE ... CHIP ENABLE
LP ... LOW VOLTAGE, LOW VOLTAGE DATA RETENTION and LOW POWER
OE ... OUTPUT ENABLE

5V SYNCHRONOUS SRAMS

SR ... SYNCHRONOUS READS
DSCE ... DUAL SYNCHRONOUS CHIP ENABLE
BW ... BYTE WRITE
STW ... SELF-TIMED WRITES
SWE ... SYNCHRONOUS WRITE ENABLE
SCE ... SYNCHRONOUS CHIP ENABLE

3.3V SYNCHRONOUS SRAMS

SR ... SYNCHRONOUS READS
DSCE ... DUAL SYNCHRONOUS CHIP ENABLE
BW ... BYTE WRITE
STW ... SELF-TIMED WRITES
SWE ... SYNCHRONOUS WRITE ENABLE
SCE ... SYNCHRONOUS CHIP ENABLE

5V CACHE DATA/LATCHED SRAMS

CE ..... CHIP ENABLE
OE ..... OUTPUT ENABLE
BW ..... BYTE WRITE
LA/Data ..... LATCHED ADDRESS AND DATA
DCE ..... DUAL CHIP ENABLE
SWE ..... SYNCHRONOUS WRITE ENABLE
BS ..... BYTE SELECT
DBE ..... DUAL BYTE ENABLE

3.3V CACHE DATA/LATCHED SRAMS

CE ..... CHIP ENABLE
OE ..... OUTPUT ENABLE
BW ..... BYTE WRITE
DCE ..... DUAL CHIP ENABLE
LA/Data ..... LATCHED ADDRESS AND DATA
DBE ..... DUAL BYTE ENABLE

FIFO (FIRST-IN FIRST-OUT) MEMORIES

E ..... EXPANDABLE DEPTH AND WIDTH
S ..... SYNCHRONOUS OPERATION
PF ..... PROGRAMMABLE FLAG

SRAM MODULES

APPLICATION/TECHNICAL INFORMATION

PRODUCT RELIABILITY

PACKAGE INFORMATION

SALES INFORMATION

NUMERICAL INDEX

Part #, MT:

NUMERICAL INDEX (continued)

Part #, MT:

5V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Time (ns)	Access Package and Number of Pins					Page
				PDIP	SOJ	ZIP	SOIC	TSOP	
16K x 1	$\overline{CE}$ only	MT5C1601	8 to 25	20	24	-	-	-	1-1
64K x 1	$\overline{CE}$ only	MT5C6401	8 to 25	22	24	-	-	-	1-9
256K x 1	$\overline{CE}$ only	MT5C2561	10 to 35	24	24	-	-	-	1-17
1 Meg x 1	$\overline{CE}$ only	MT5C1001	12 to 45	28	28	-	-	-	1-25
4K x 4	$\overline{CE}$ only	MT5C1604	8 to 25	20	24	-	-	-	1-33
4K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1605	8 to 25	22	24	-	-	-	1-41
16K x 4	$\overline{CE}$ only	MT5C6404	8 to 25	22	24	-	-	-	1-49
16K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C6405	8 to 25	24	24	-	-	-	1-57
64K x 4	$\overline{CE}$ only	MT5C2564	10 to 35	24	24	-	24	-	1-65
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C2565	10 to 35	28	28	-	-	-	1-73
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1005	12 to 45	28	28	-	-	-	1-81
256K x 4	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C256K4A1	12 to 25	-	32	-	-	-	1-89
1 Meg x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1M4A1	20 to 55	-	32	-	-	-	1-99
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C1M4B2	20 to 35	-	32	-	-	32	1-101
2K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C1608	8 to 25	24	24	-	-	-	1-109
8K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C6408	8 to 25	28	28	-	-	-	1-117
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C2568	10 to 35	28	28	28	-	-	1-125
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C1008	12 to 45	32	32	-	-	-	1-133
128K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C128K8A1	12 to 25	-	32	-	-	-	1-141
512K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C512K8A1	20 to 55	-	32	-	-	-	1-151
512K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C512K8B2	20 to 35	-	36	-	-	36	1-153
32K x 9	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C2889	15 to 25	-	32	-	-	-	1-161
128K x 9	$\overline{CE}$ and $\overline{OE}$	MT5C1189	15 to 35	-	32	-	-	-	1-169
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5C64K16A1	12 to 25	-	44	-	-	44	1-177
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5C256K16B2	20 to 35	-	44	-	-	-	1-187

NOTE: 1. Automotive, industrial and extended temperature specifications begin on page 1-189.
2. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

3.3V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Time (ns)	Access Package and Number of Pins					Page
				PDIP	SOJ	ZIP	SOIC	TSOP	
256K x 1	$\overline{CE}$ only with separate I/O	MT5LC2561	15, 20, 25, 35	24	24	-	-	-	2-1
1 Meg x 1	$\overline{CE}$ only with separate I/O	MT5LC1001	20, 25, 35, 45	28	28	-	-	-	2-9
64K x 4	$\overline{CE}$ only	MT5LC2564	15, 20, 25, 35	24	24	-	24	-	2-17
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC2565	15, 20, 25, 35	28	28	-	-	-	2-25
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1005	20, 25, 35, 45	28	28	-	-	-	2-33
256K x 4	$\overline{CE}$ and center pin power and ground	MT5LC256K4D4	20, 25	-	32	-	-	32	2-41
1 Meg x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1M4C3	20, 25, 35, 55	-	32	-	-	-	2-51
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5LC1M4D4	20, 25, 35	-	32	-	-	32	2-53
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC2568	15, 20, 25, 35	28	28	28	-	-	2-61
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5LC1008	20, 25, 35, 45	32	32	-	-	-	2-69
128K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5LC128K8D4	20, 25	-	32	-	-	32	2-77
512K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC512K8C3	20, 25, 35, 55	-	32	-	-	-	2-87
512K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5LC512K8D4	20, 25, 35	-	36	-	-	36	2-89
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5LC64K16D4	20, 25	-	44	-	-	44	2-97
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5LC256K16D4	20, 25, 35	-	44	-	-	-	2-107

NOTE: 1. Automotive, industrial and extended temperature specifications begin on page 1-189.
2. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

5V SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Die	Page
				PLCC	PQFP	SOJ	TSOP		
128K x 9	Synchronous SPARC® Cache SRAM	MT58C1289	16, 20	-	-	32	-	CD1 CD2	3-1
16K x 16	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58C1616	12, 15, 20, 25	52	52	-	-	CD1 CD2	3-11
16K x 18	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58C1618	12, 15, 20, 25	52	52	-	-	CD1	3-21

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

3.3V SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Die	Page
				PLCC	PQFP	SOJ	TSOP		
16K x 16	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58LC1616	20, 25	52	52	-	-	CD1 CD2	4-1
16K x 18	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58LC1618	20, 25	52	52	-	-	CD1	4-11

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

5V CACHE DATA/LATCHED SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package				Die	Page
				PLCC	PQFP	SOJ	TSOP		
Single 8K x 16 or Dual 4K x 16	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A11)	MT56C0816	20, 25, 35	52	52	-	-		5-1
Single 8K x 16 or Dual 4K x 16	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A12)	MT56C3816	20, 25, 35	52	52	-	-		5-13
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Write Controls, Output Enable	MT5C2516	12, 15, 20, 25	52	52	-	-	CD1 CD2	5-25
Single 8K x 18 or Dual 4K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A11)	MT56C0818	20, 25, 35	52	52	-	-		5-39
Single 8K x 18 or Dual 4K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Synchronous Write Enable	MT56C2818	24	52	52	-	-		5-51
Single 8K x 18 or Dual 4K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A12)	MT56C3818	20, 25, 35	52	52	-	-		5-61
16K x 18	Latched Address and Data, Dual Chip Enables, Byte Write Controls	MT5C2818	12, 15, 20, 25	52	52	-	-	CD1 CD2	5-73
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Enables	MT56C16K16B2	12, 15, 20, 25	52	52	-	-	CD1 CD2	5-87

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

3.3V CACHE DATA/LATCHED SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package				Die	Page
				PLCC	PQFP	SOJ	TSOP		
16K x 16	Latched Address and Data, Dual Chip Enables, Output Enable, Byte Write Controls	MT5LC2516	20, 25	52	52	-	-	CD1 CD2	6-1
16K x 18	Latched Address and Data, Dual Chip Enables, Byte Write Controls Byte Write Controls	MT5LC2818	20, 25	52	52	-	-	CD1 CD2	6-15
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Enables	MT56LC16K16C3	20, 25	52	52	-	-	CD1 CD2	6-29

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

FIFO MEMORIES PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Cycle Time (ns)	Package/Number of Pins		Page
				PDIP	PLCC	
512 x 9	Expandable Depth and Width	MT52C9005	15, 20, 25, 35	28	32	7-1
512 x 9	Programmable Flag Expandable Depth and Width	MT52C9007	15, 20, 25, 35	28	32	7-13
1K x 9	Expandable Depth and Width	MT52C9010	15, 20, 25, 35	28	32	7-29
1K x 9	Programmable Flag Expandable Depth and Width	MT52C9012	15, 20, 25, 35	28	32	7-41
2K x 9	Expandable Depth and Width	MT52C9020	15, 20, 25, 35	28	32	7-57
2K x 9	Programmable Flag Expandable Depth and Width	MT52C9022	15, 20, 25, 35	28	32	7-69
4K x 9	Expandable Depth and Width	MT52C4K9A1	15, 20, 25, 35	28	32	7-85
4K x 9	Programmable Flag Expandable Depth and Width	MT52C4K9E5	15, 20, 25, 35	28	32	*
8K x 9	Expandable Depth and Width	MT52C8K9B2	15, 20, 25, 35	28	32	7-85
8K x 9	Programmable Flag Expandable Depth and Width	MT52C8K9F6	15, 20, 25, 35	28	32	*
512 x 18	Synchronous FIFO with clocked, registered I/O	MT53C51218A1	15, 20, 25, 35	-	68	7-97
1K x 18	Synchronous FIFO with clocked, registered I/O	MT53C1K18B2	15, 20, 25, 35	-	68	7-97
2K x 18	Synchronous FIFO with clocked, registered I/O	MT53C2K18C3	15, 20, 25, 35	-	68	7-97
4K x 18	Synchronous FIFO with clocked, registered I/O	MT53C4K18D4	15, 20, 25, 35	-	68	7-97

NOTE: 1. Automotive and industrial temperature specifications begin on page 7-115.
2. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

*Consult factory for availability and data sheet.

SRAM MODULES PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins			Page
				DIP	ZIP	SIMM	
128K x 8	$\overline{CE}$ and $\overline{OE}$	MT4S1288	20*, 25, 30	32	-	-	8-1
32K x 16	$\overline{CE}$ and $\overline{OE}$	MT2S3216	20*, 25, 30	40	-	-	8-9
64K x 16	$\overline{CE}$ and $\overline{OE}$	MT4S6416	20*, 25, 30	40	-	-	8-17
16K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S1632	10*, 15, 20, 25, 35	-	64	64	8-25
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S6432	15*, 20, 25, 30, 35	-	64	64	8-33
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4S12832	15*, 20, 25, 35	-	64	64	8-41
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S25632	15*, 20, 25, 35	-	64	64	8-49

*Preliminary

APPLICATION/TECHNICAL NOTE SELECTION GUIDE

MICRON

5V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Time (ns)	Access Package and Number of Pins					Page
				PDIP	SOJ	ZIP	SOIC	TSOP	
16K x 1	$\overline{CE}$ only	MT5C1601	8 to 25	20	24	-	-	-	1-1
64K x 1	$\overline{CE}$ only	MT5C6401	8 to 25	22	24	-	-	-	1-9
256K x 1	$\overline{CE}$ only	MT5C2561	10 to 35	24	24	-	-	-	1-17
1 Meg x 1	$\overline{CE}$ only	MT5C1001	12 to 45	28	28	-	-	-	1-25
4K x 4	$\overline{CE}$ only	MT5C1604	8 to 25	20	24	-	-	-	1-33
4K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1605	8 to 25	22	24	-	-	-	1-41
16K x 4	$\overline{CE}$ only	MT5C6404	8 to 25	22	24	-	-	-	1-49
16K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C6405	8 to 25	24	24	-	-	-	1-57
64K x 4	$\overline{CE}$ only	MT5C2564	10 to 35	24	24	-	24	-	1-65
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C2565	10 to 35	28	28	-	-	-	1-73
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1005	12 to 45	28	28	-	-	-	1-81
256K x 4	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C256K4A1	12 to 25	-	32	-	-	-	1-89
1 Meg x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1M4A1 •	20 to 55	-	32	-	-	-	1-99
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C1M4B2	20 to 35	-	32	-	-	32	1-101
2K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C1608	8 to 25	24	24	-	-	-	1-109
8K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C6408	8 to 25	28	28	-	-	-	1-117
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C2568	10 to 35	28	28	28	-	-	1-125
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C1008	12 to 45	32	32	-	-	-	1-133
128K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C128K8A1	12 to 25	-	32	-	-	-	1-141
512K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C512K8A1	20 to 55	-	32	-	-	-	1-151
512K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5C512K8B2	20 to 35	-	36	-	-	36	1-153
32K x 9	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C2889	15 to 25	-	32	-	-	-	1-161
128K x 9	$\overline{CE}$ and $\overline{OE}$	MT5C1189	15 to 35	-	32	-	-	-	1-169
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5C64K16A1	12 to 25	-	44	-	-	44	1-177
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5C256K16B2	20 to 35	-	44	-	-	-	1-187

NOTE: 1. Automotive, industrial and extended temperature specifications begin on page 1-189.
2. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

SRAM

16K x 1 SRAM

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

OPTIONS MARKING

- Timing

8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention — L

- Temperature

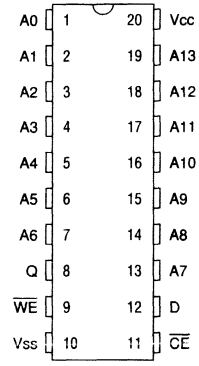
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C1601DJ-12 L IT

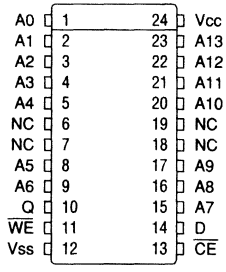
*Preliminary

PIN ASSIGNMENT (Top View)

20-Pin DIP
(SA-1)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

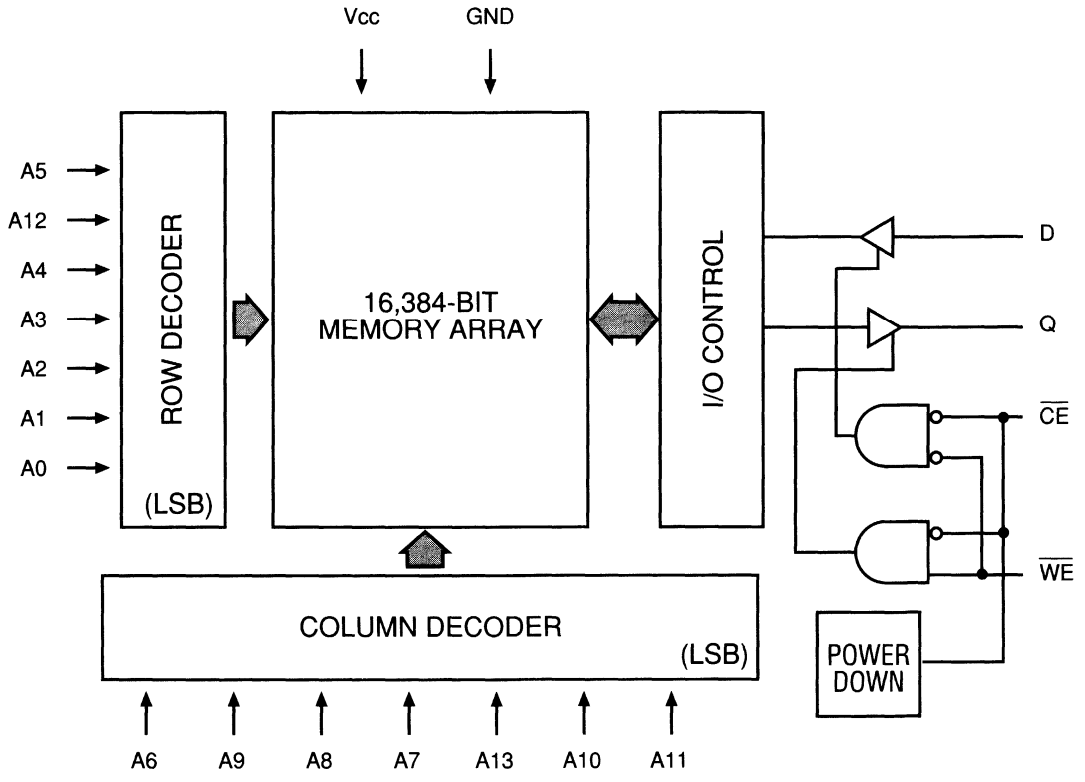
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8+	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	7	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-8* MIN	-8* MAX	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	-20 MIN	-20 MAX	-25 MIN	-25 MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	8		10		12		15		20		25		ns	
Address access time	^tAA		8		10		12		15		20		25	ns	
Chip Enable access time	^tACE		7		8		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE†	2		2		2		3		4		5		ns	7, 15
		2		2		2		2		2		2			
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	8		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	6.5		8		10		12		15		20		ns	
Address valid to end of write	^tAW	6.5		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	5.5		7		8		10		12		15		ns	
Data setup time	^tDS	4.5		6		7		8		9		10		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

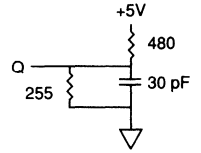


Fig. 1 OUTPUT LOAD EQUIVALENT

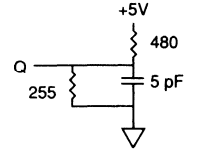


Fig. 2 OUTPUT LOAD EQUIVALENT

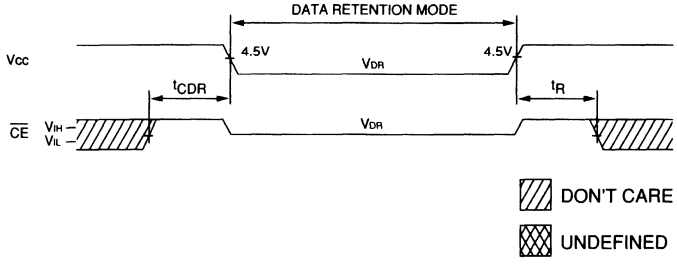
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

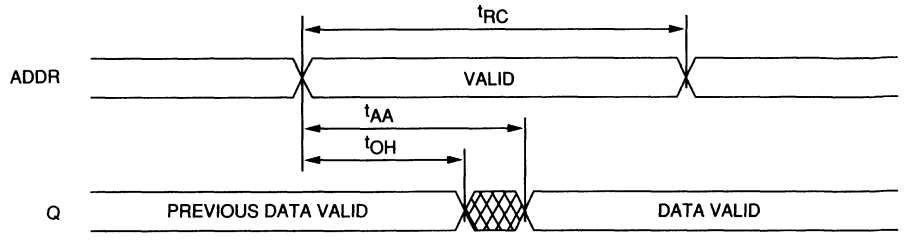
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

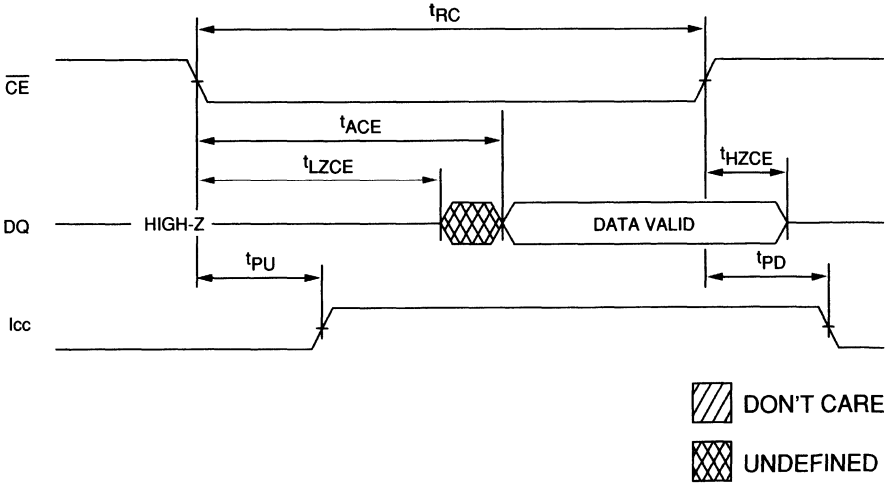
LOW Vcc DATA RETENTION WAVEFORM



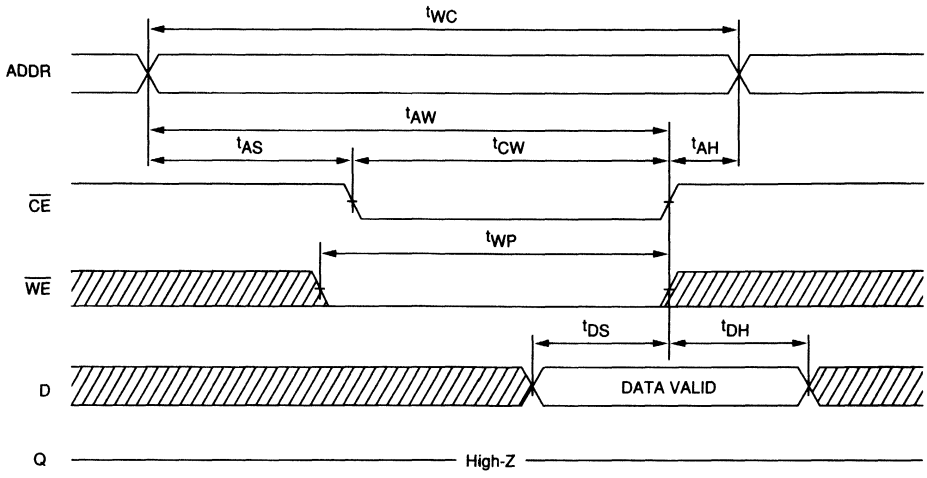
READ CYCLE NO. 1 [8, 9]



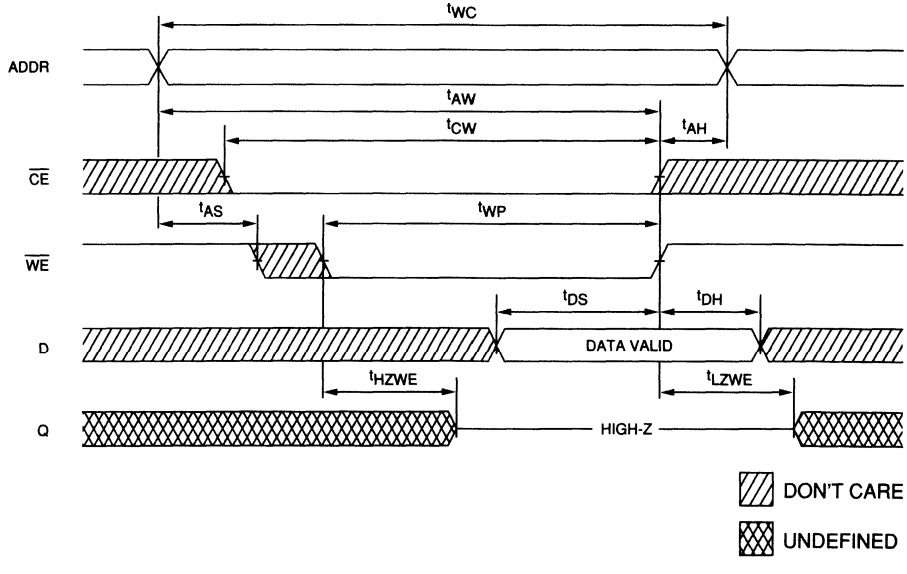
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 1 SRAM

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

OPTIONS

	MARKING
• Timing	
8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

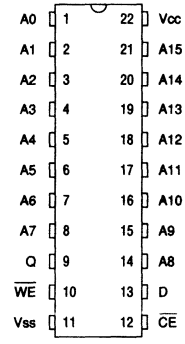
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C6401DJ-10 L IT

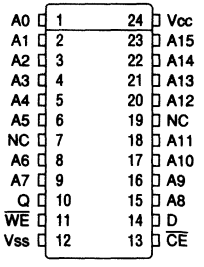
*Preliminary

PIN ASSIGNMENT (Top View)

22-Pin DIP
(SA-2)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

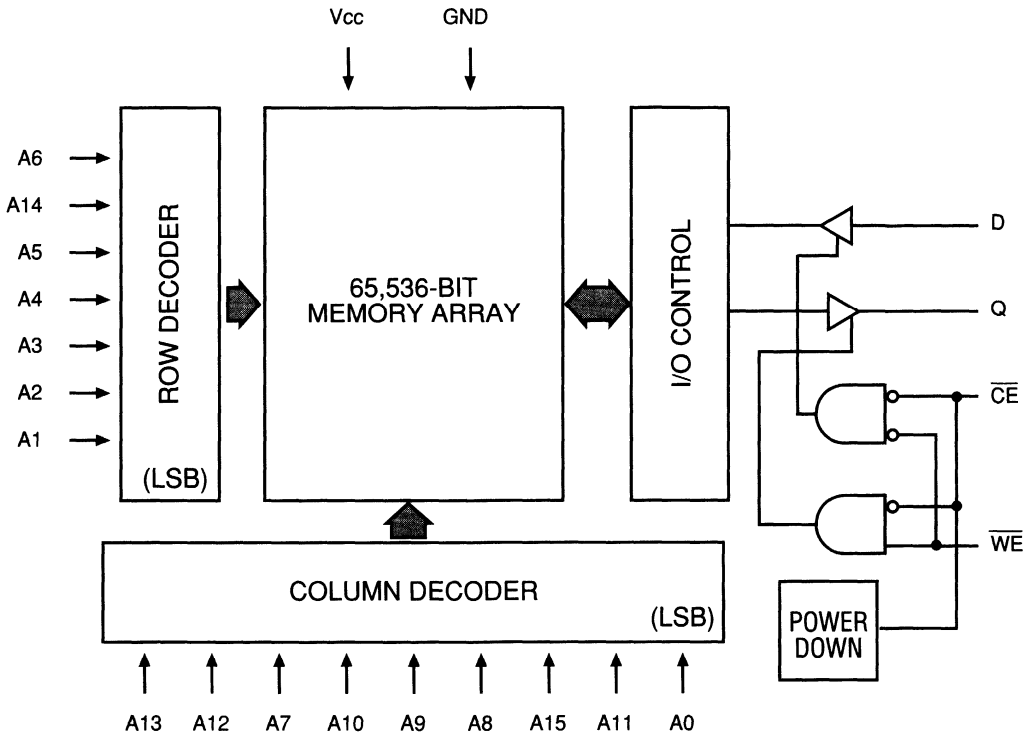
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8†	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

†Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	7	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	SYM	-8* MIN	-8* MAX	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	-20 MIN	-20 MAX	-25 MIN	-25 MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	8		10		12		15		20		25		ns	
Address access time	^tAA		8		10		12		15		20		25	ns	
Chip Enable access time	^tACE		7		8		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE†	2 / 2		2 / 2		2 / 2		3 / 2		5 / 2		5 / 2		ns	7, 15
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	8		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	6.5		8		10		12		15		20		ns	
Address valid to end of write	^tAW	6.5		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	5.5		7		8		10		12		15		ns	
Data setup time	^tDS	4.5		6		7		8		9		10		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

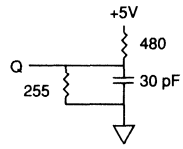


Fig. 1 OUTPUT LOAD EQUIVALENT

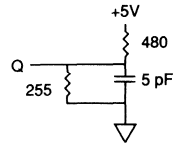


Fig. 2 OUTPUT LOAD EQUIVALENT

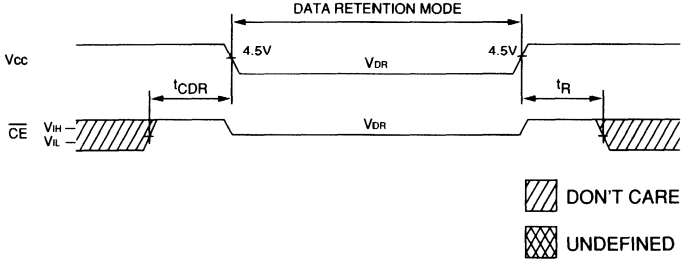
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

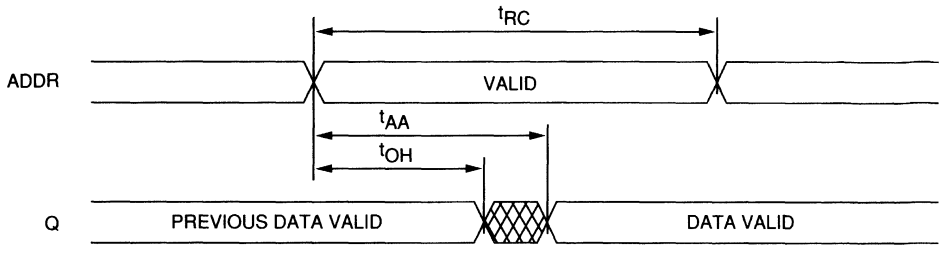
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

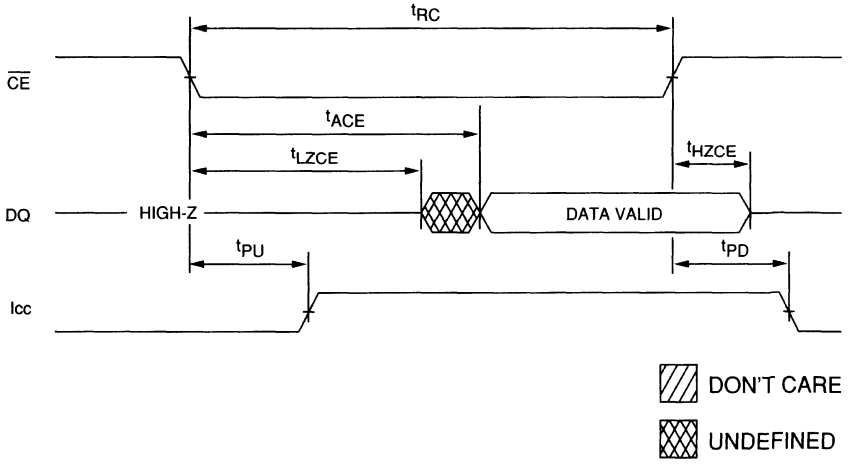
LOW Vcc DATA RETENTION WAVEFORM



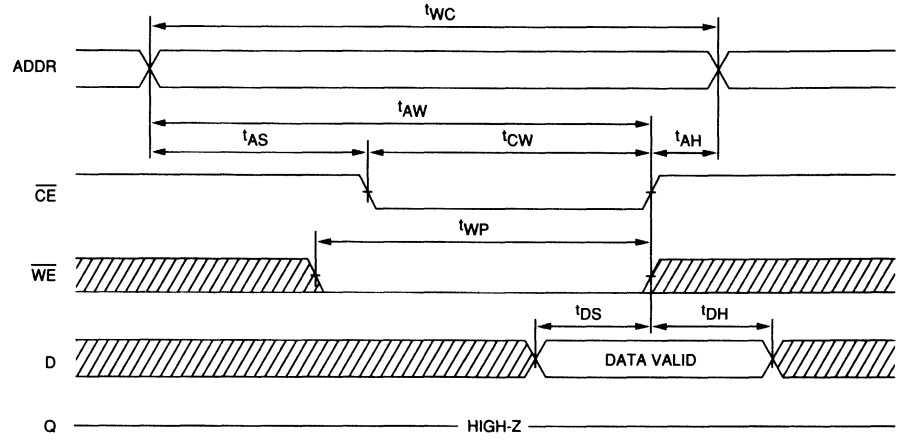
READ CYCLE NO. 1 [8, 9]



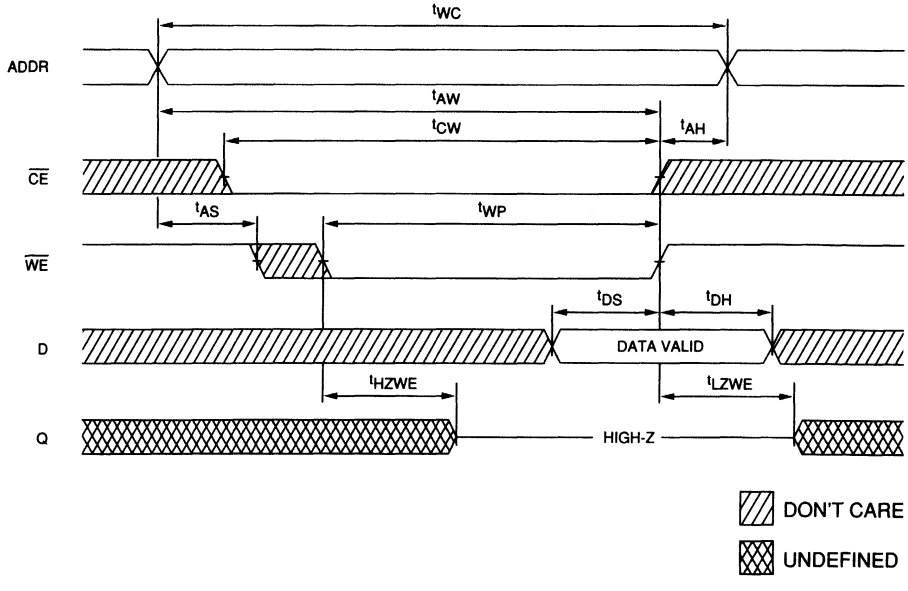
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

256K x 1 SRAM

FEATURES

- High speed: 10*, 12*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

OPTIONS MARKING

- Timing

10ns access	-10*
12ns access	-12*
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention — L
- 2V data retention, low power — LP

- Temperature

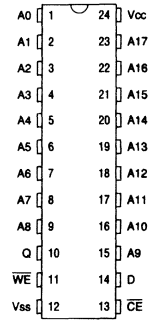
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C2561DJ-15 LP IT

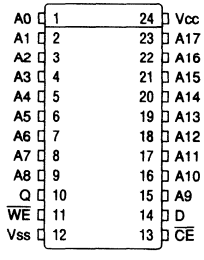
*Preliminary

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

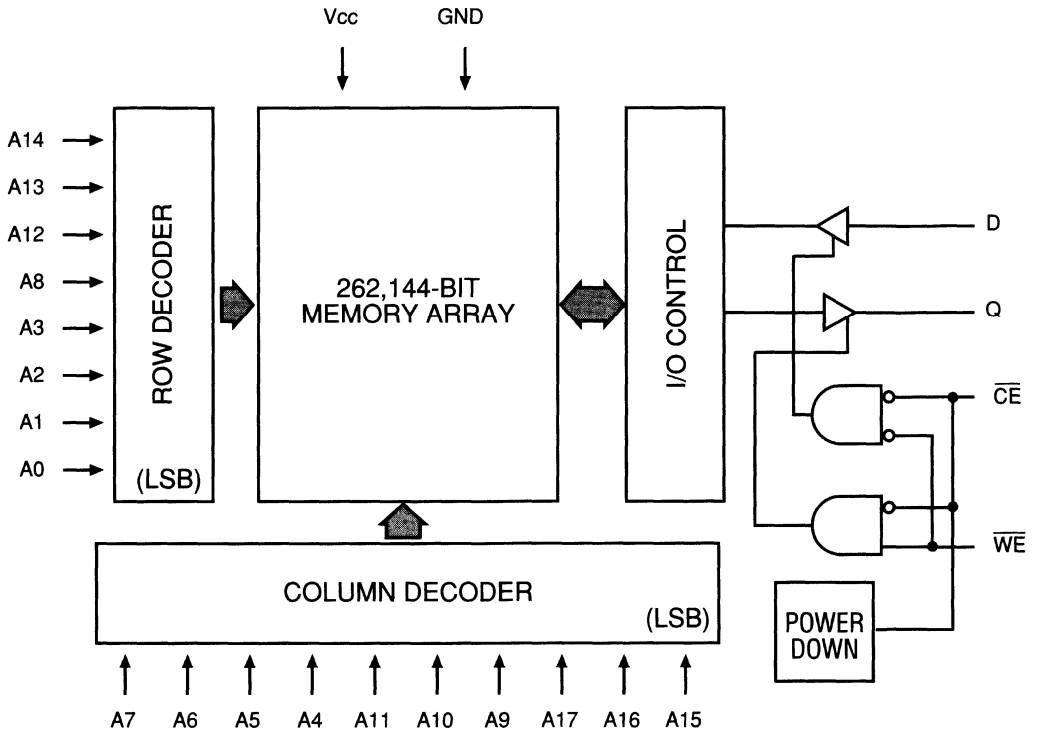
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW.

The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10+†	-12+†	-15†	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	85	180	160	140	120	110	90	mA	3, 14
	"LP" VERSION	I_{CC}	65	-	-	-	110	100	80	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	11	45	40	30	30	25	25	mA	14
	"LP" VERSION	I_{SB1}	3	-	-	-	7	7	7	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	14

+Preliminary
† LP version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10*		-12*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	tRC	10		12		15		20		25		35		ns	
Address access time	tAA		10		12		15		20		25		35	ns	
Chip Enable access time	tACE		10		12		15		20		25		35	ns	
Output hold from address change	tOH	2		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	3		4		4		4		6		6		ns	7
Chip disable to output in High-Z	tHZCE		6		8		8		9		9		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		10		12		15		20		25		35	ns	
WRITE Cycle															
WRITE cycle time	tWC	10		12		15		20		25		30		ns	
Chip Enable to end of write	tCW	9		10		10		15		15		20		ns	
Address valid to end of write	tAW	9		10		10		15		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
WRITE pulse width	tWP	9		10		10		15		15		20		ns	
Data setup time	tDS	6		7		7		10		10		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		4		4		4		5		5		ns	7
Write Enable to output in High-Z	tHZWE		6		7		7		10		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

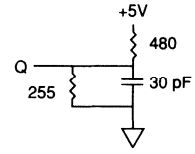


Fig. 1 OUTPUT LOAD EQUIVALENT

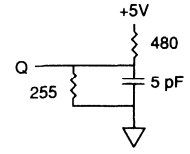


Fig. 2 OUTPUT LOAD EQUIVALENT

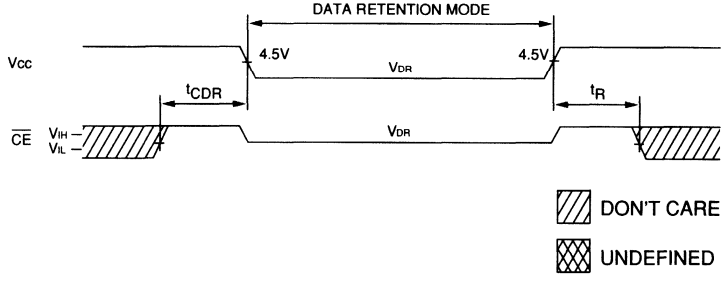
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

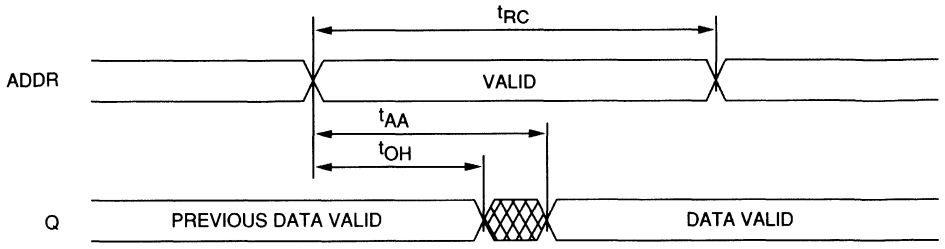
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	300	µA	
		Vcc = 3V	ICCDR		90	500	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

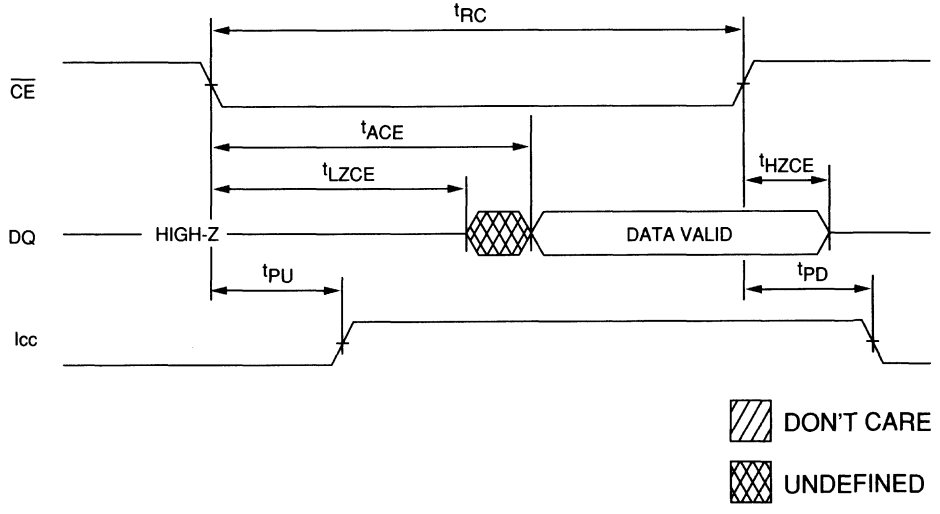
LOW Vcc DATA RETENTION WAVEFORM



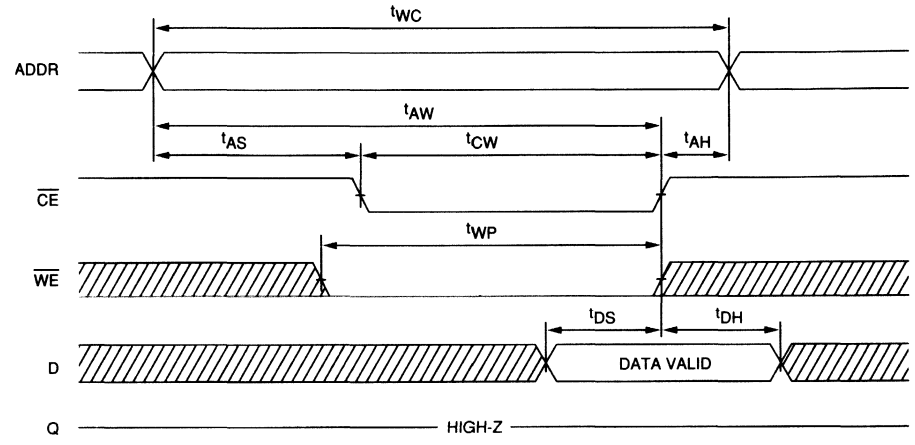
READ CYCLE NO. 1 [8, 9]



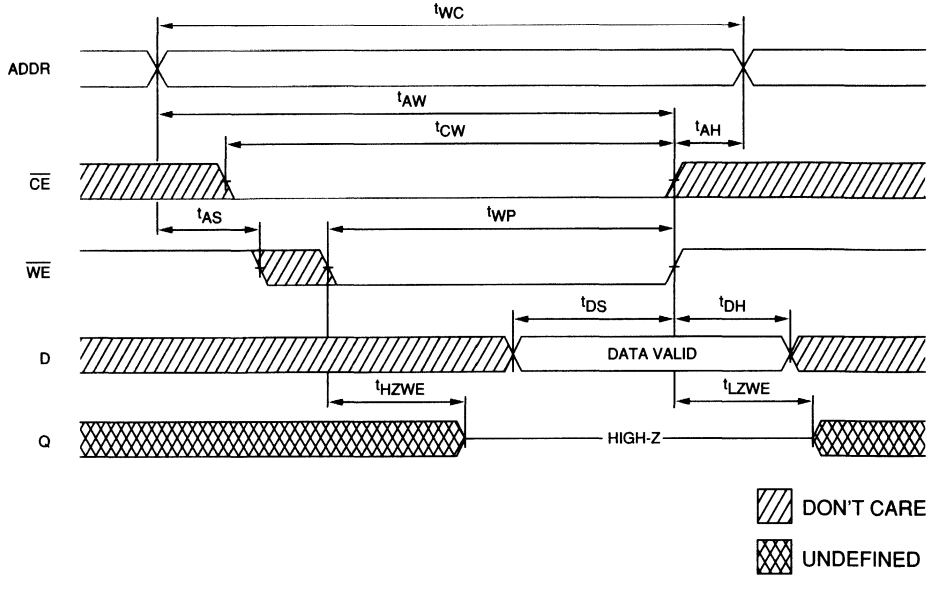
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

1 MEG x 1 SRAM

FEATURES

- High speed: 12*, 15*, 17, 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12*
15ns access	-15*
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

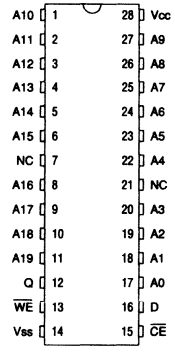
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C1001DJ-20 L IT

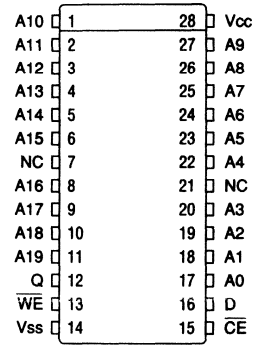
*Preliminary

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-5)



28-Pin SOJ (SD-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

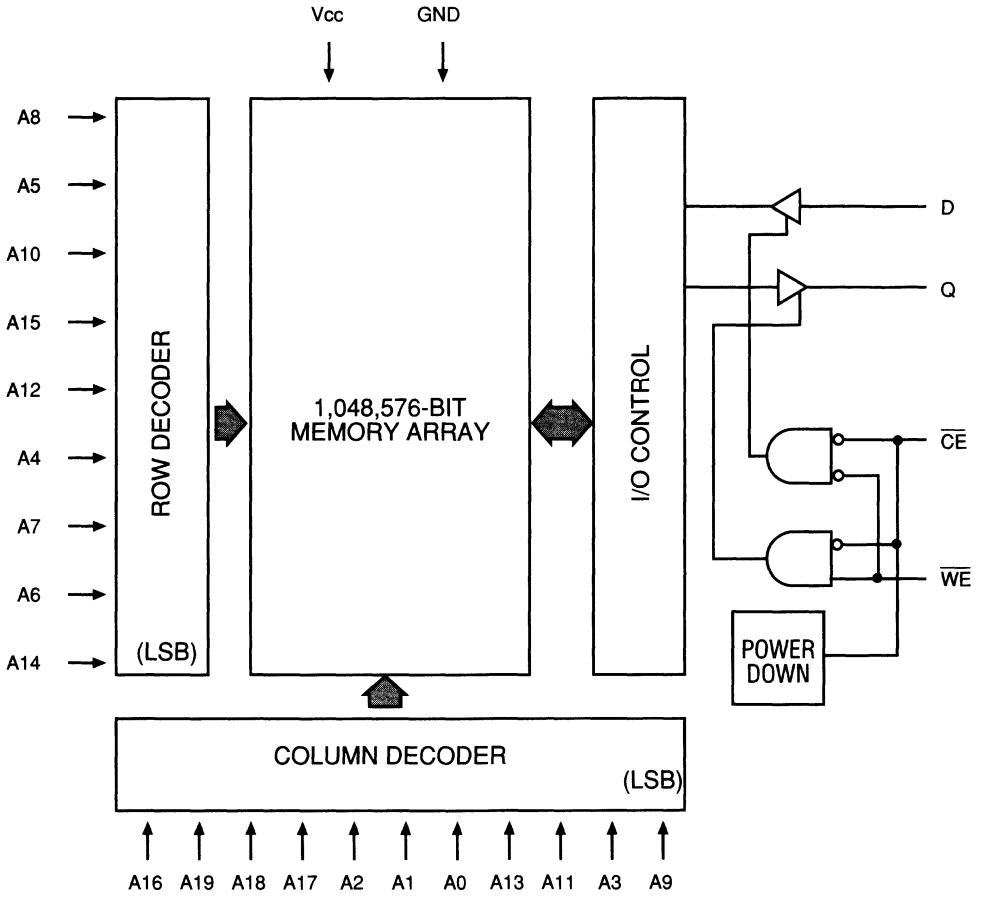
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A6 and A14) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12+	-15+	-17	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	95	190	165	155	140	125	115	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	17	45	40	40	35	30	25	25	mA	14
	"LP" Version Only	I_{SB1}	1.3	3	3	3	3	3	3	3	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	5	5	5	mA	14
	"L" and "LP" Versions Only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION		-12*		-15*		-17		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^tRC	12		15		17		20		25		35		45		ns	
Address access time	^tAA		12		15		17		20		25		35		45	ns	
Chip Enable access time	^tACE		12		15		17		20		25		35		45	ns	
Output hold from address change	^tOH	3		3		3		3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		7		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		17		20		25		35		45	ns	
WRITE Cycle																	
WRITE cycle time	^tWC	12		15		17		20		25		35		45		ns	
Chip Enable to end of write	^tCW	8		10		12		12		15		20		25		ns	
Address valid to end of write	^tAW	8		10		12		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	^tWP	8		9		12		12		15		20		25		ns	
Data setup time	^tDS	6		7		8		8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		15		18	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

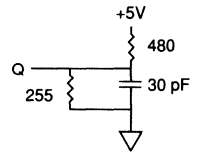


Fig. 1 OUTPUT LOAD EQUIVALENT

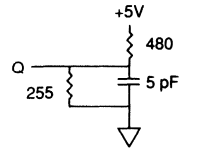


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

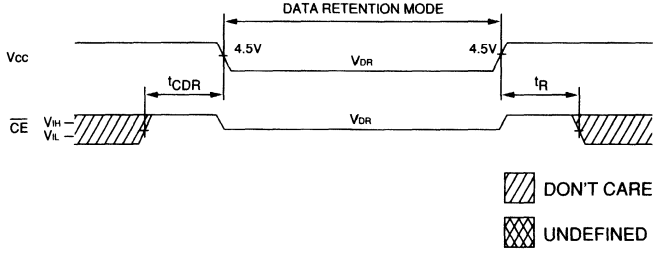
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

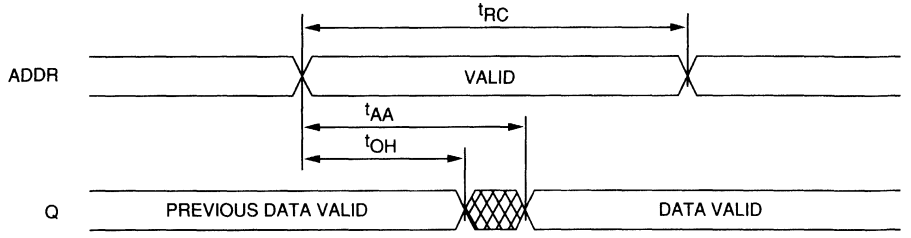
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	150	µA	
		Vcc = 3V			60	250	µA	
		Vcc = 3V*			30	100	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

*Preliminary

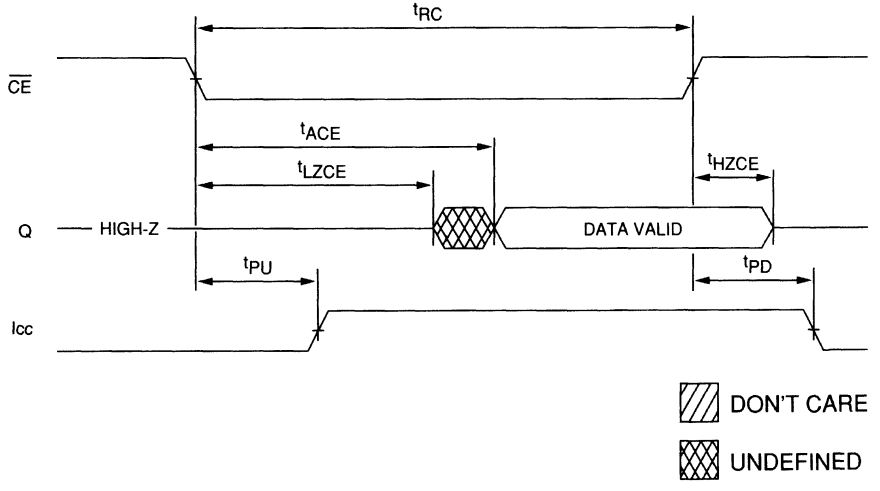
LOW Vcc DATA RETENTION WAVEFORM



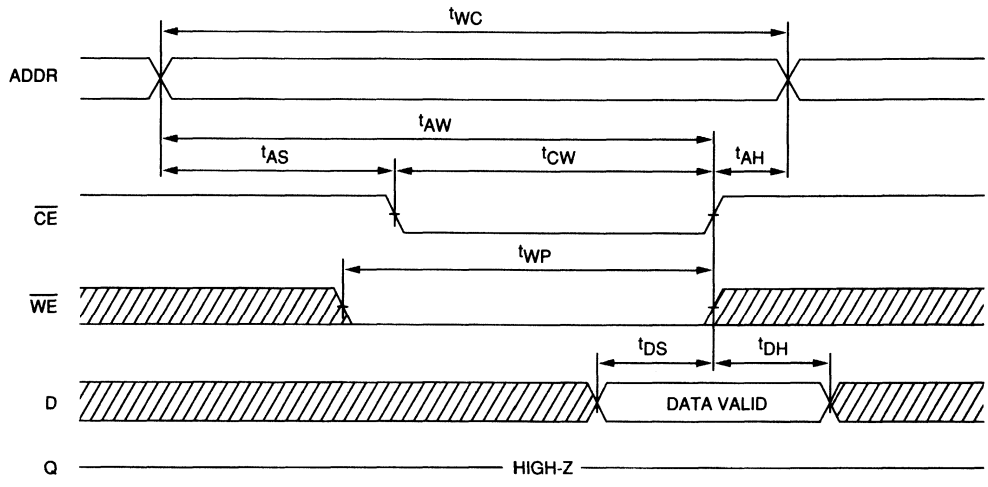
READ CYCLE NO. 1 [8, 9]



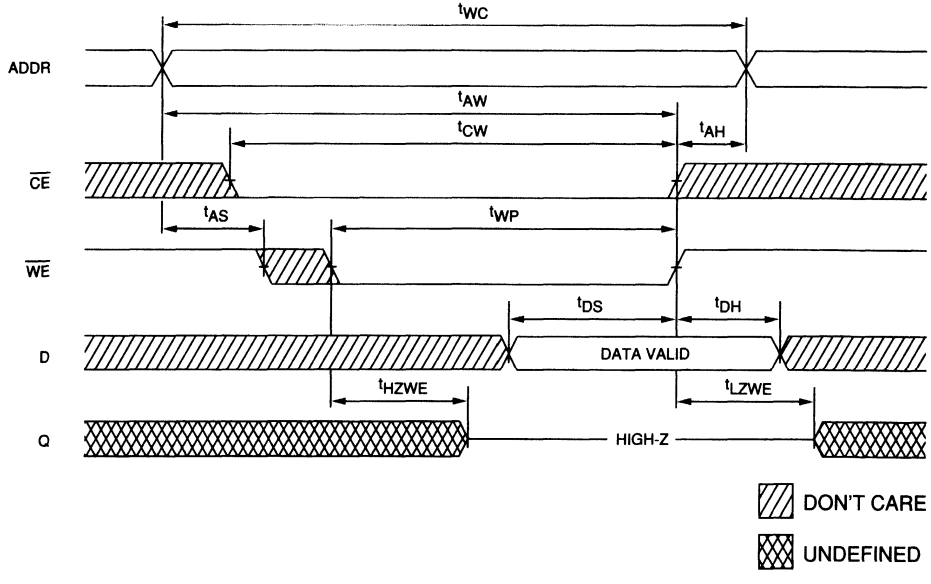
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

4K x 4 SRAM

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

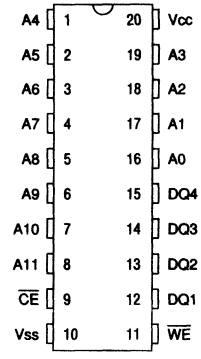
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C1604DJ-10 L AT

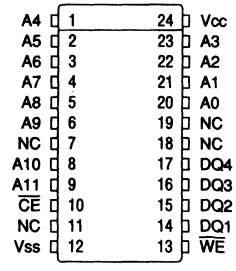
*Preliminary

PIN ASSIGNMENT (Top View)

20-Pin DIP
(SA-1)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

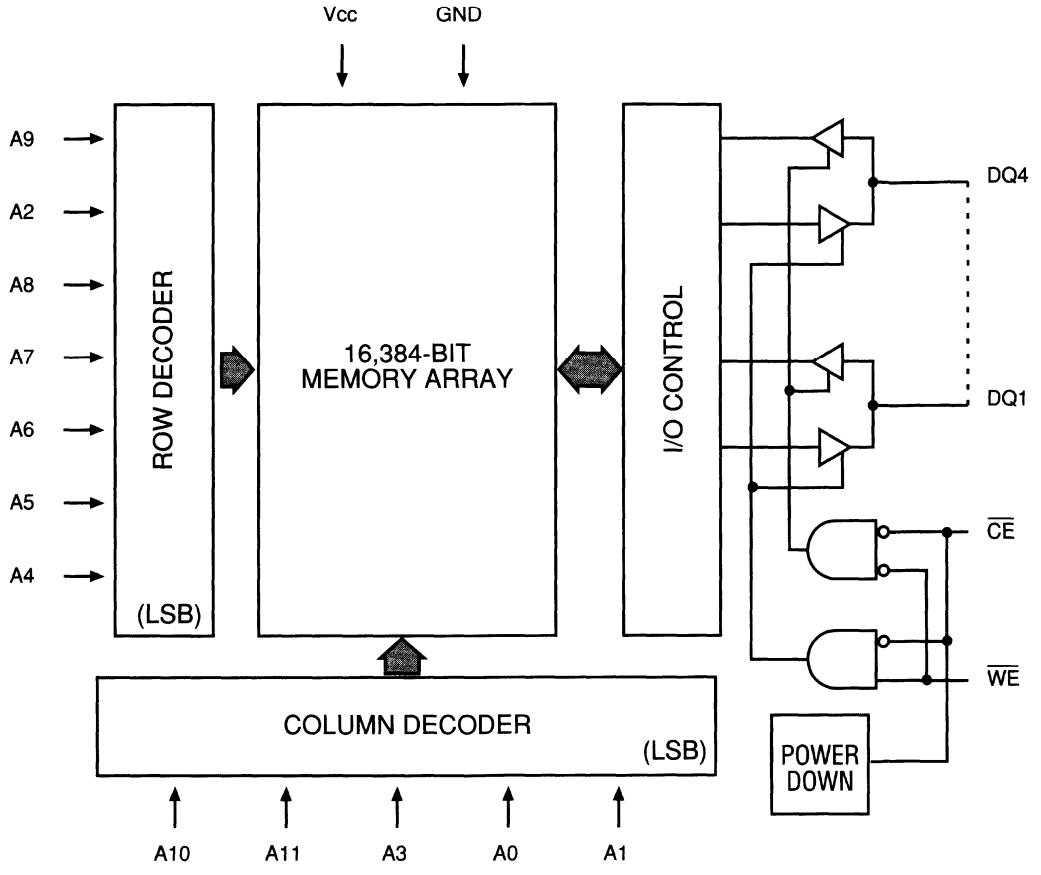
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8+	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-8*		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	8		10		12		15		20		25		ns	
Address access time	^tAA		8		10		12		15		20		25	ns	
Chip Enable access time	^tACE		7		8		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE†	2		2		2		3		5		5		ns	7, 15
		2		2		2		2		2		2			
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	8		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	6.5		8		10		12		15		20		ns	
Address valid to end of write	^tAW	6.5		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	5.5		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	4.5		6		7		8		9		10		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

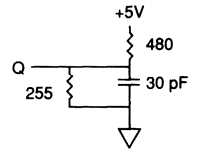


Fig. 1 OUTPUT LOAD EQUIVALENT

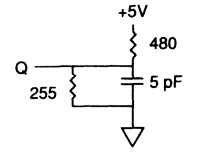


Fig. 2 OUTPUT LOAD EQUIVALENT

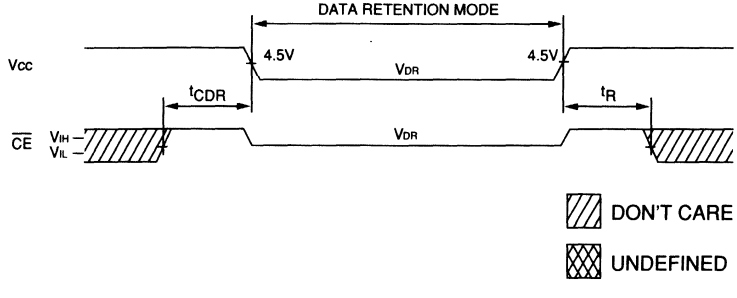
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

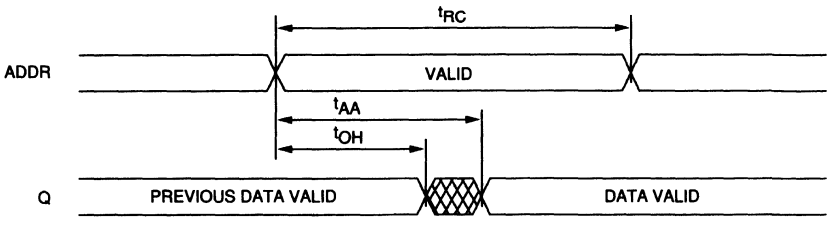
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

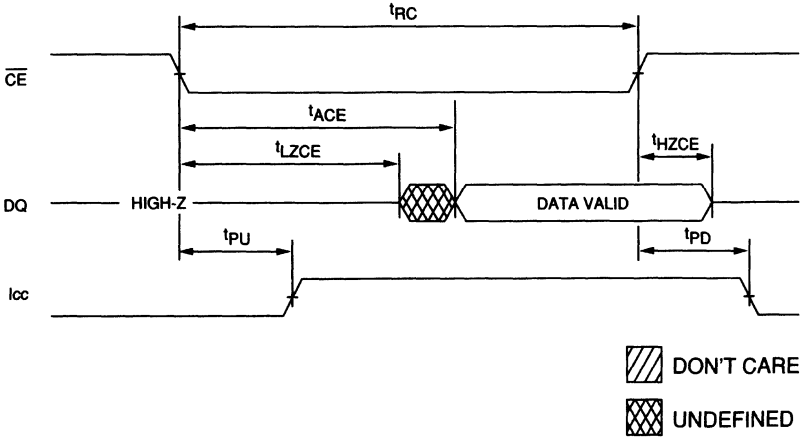
LOW Vcc DATA RETENTION WAVEFORM



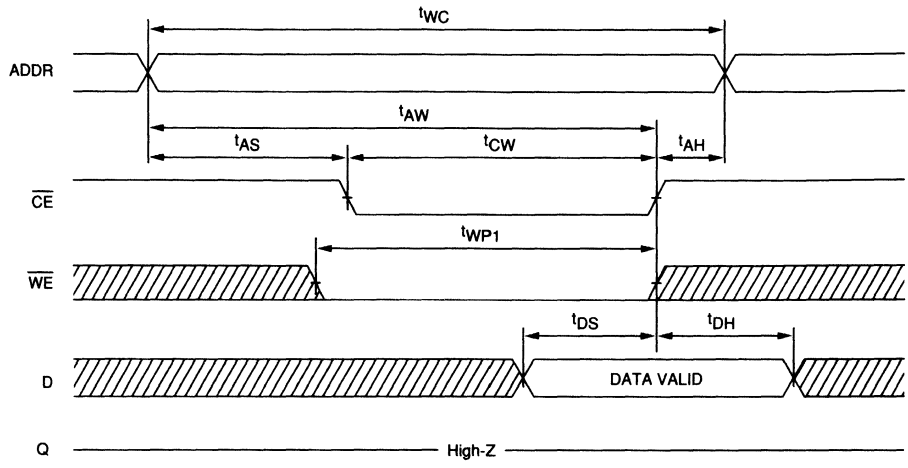
READ CYCLE NO. 1 [8, 9]



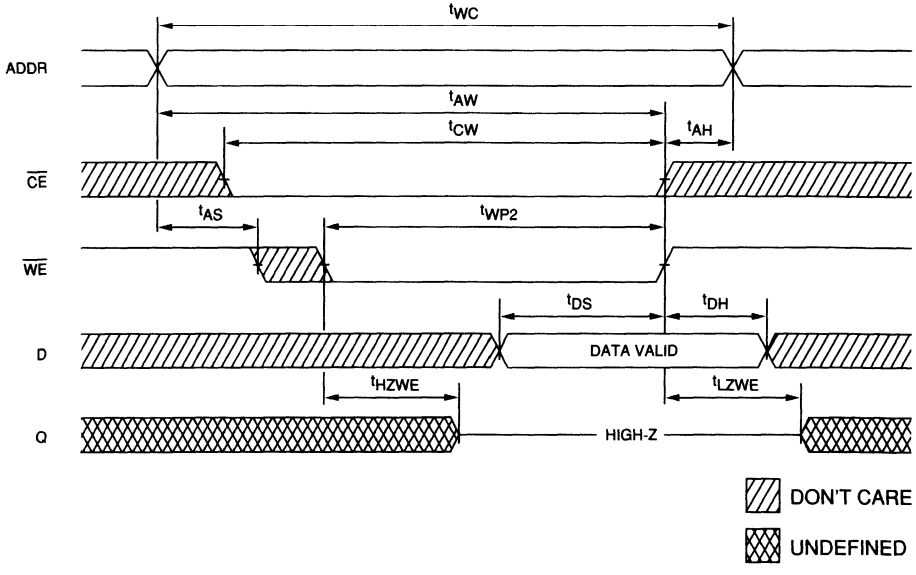
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

4K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

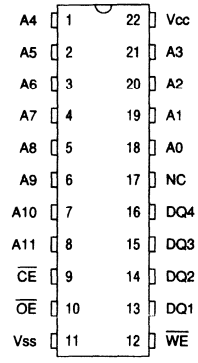
NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- Part Number Example: MT5C1605DJ-10 L IT

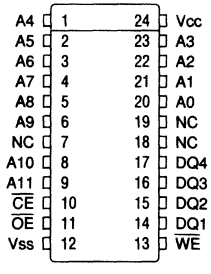
*Preliminary

PIN ASSIGNMENT (Top View)

22-Pin DIP
(SA-2)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

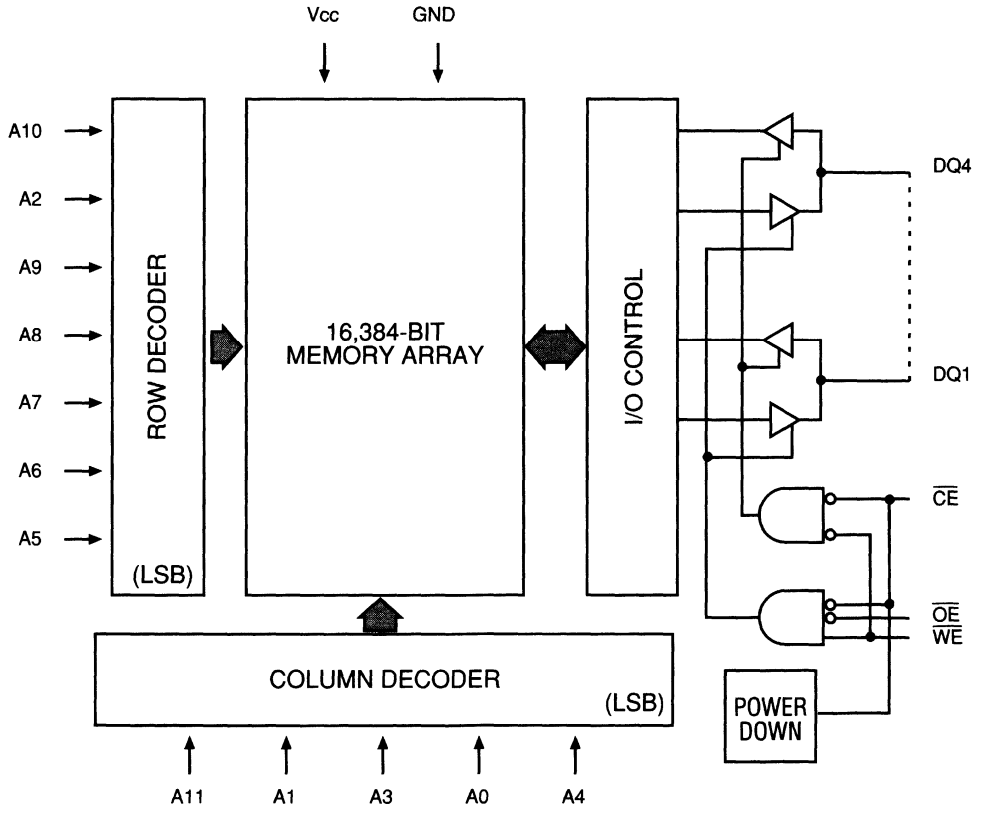
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8+	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

5 VOLT SRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	8		10		12		15		20		25		ns	
Address access time	t_{AA}		8		10		12		15		20		25	ns	
Chip Enable access time	t_{ACE}		7		8		10		12		15		20	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}†	2		2		2		3		5		5		ns	7, 15
		2		2		2		2		2		2			
Chip disable to output in High-Z	t_{HZCE}		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		8		10		12		15		20		25	ns	
Output Enable access time	t_{AOE}		3.5		4		5		6		7		8	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		3.5		4		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	8		10		12		15		20		25		ns	
Chip Enable to end of write	t_{CW}	6.5		8		10		12		15		20		ns	
Address valid to end of write	t_{AW}	6.5		8		10		12		15		20		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
WRITE pulse width	t_{WP1}	5.5		7		8		10		12		15		ns	
WRITE pulse width	t_{WP2}	8		9		10		14		18		20		ns	
Data setup time	t_{DS}	4.5		6		7		8		9		10		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	t_{HZWE}		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

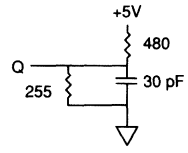


Fig. 1 OUTPUT LOAD EQUIVALENT

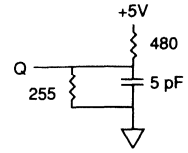


Fig. 2 OUTPUT LOAD EQUIVALENT

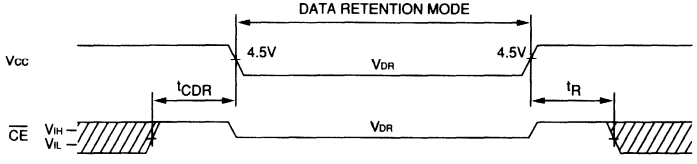
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

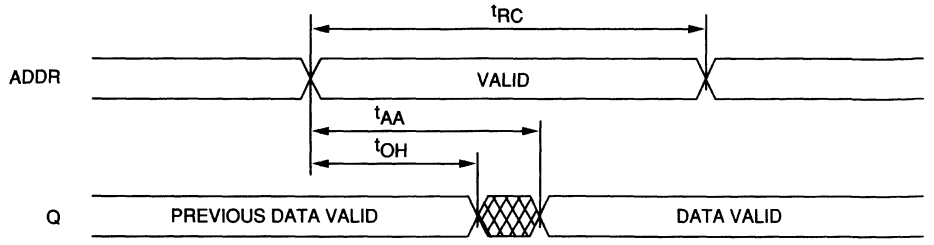
LOW Vcc DATA RETENTION WAVEFORM



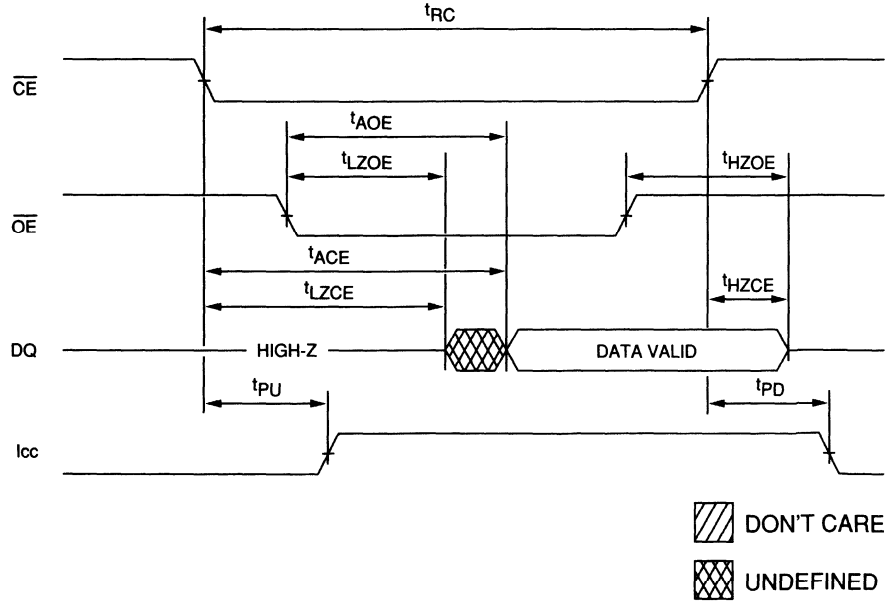
DON'T CARE

UNDEFINED

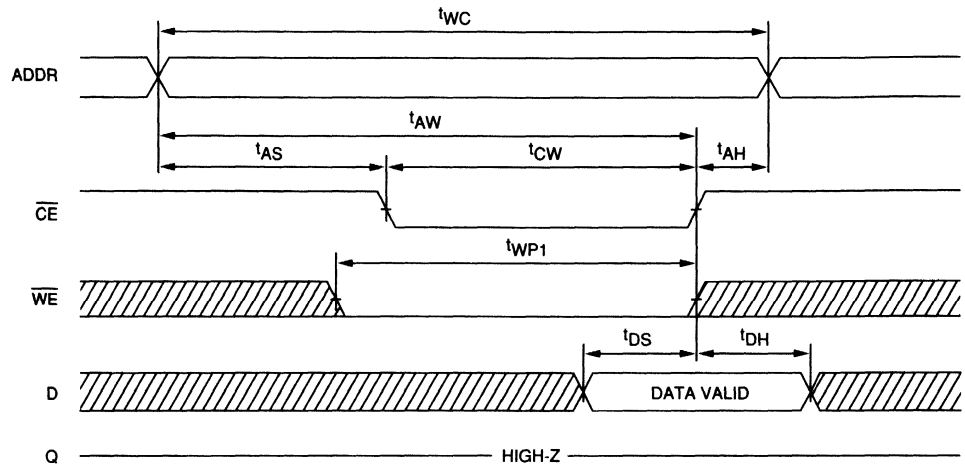
READ CYCLE NO. 1 [8, 9]



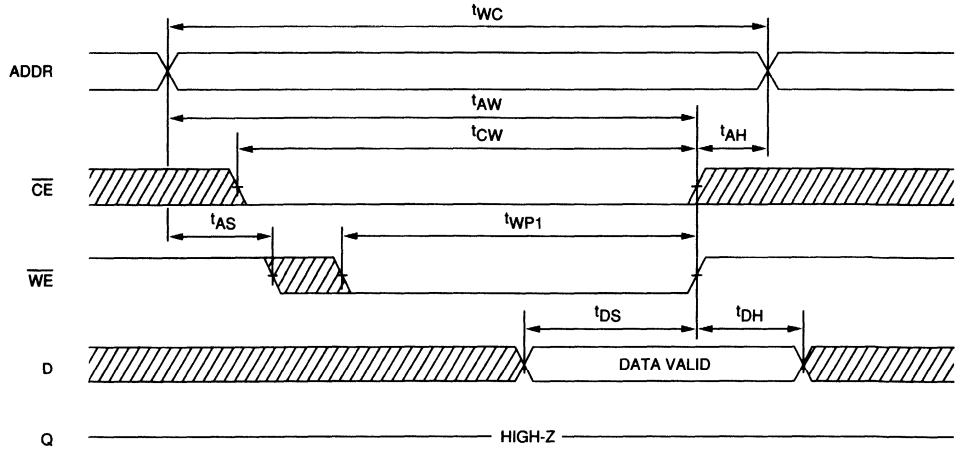
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

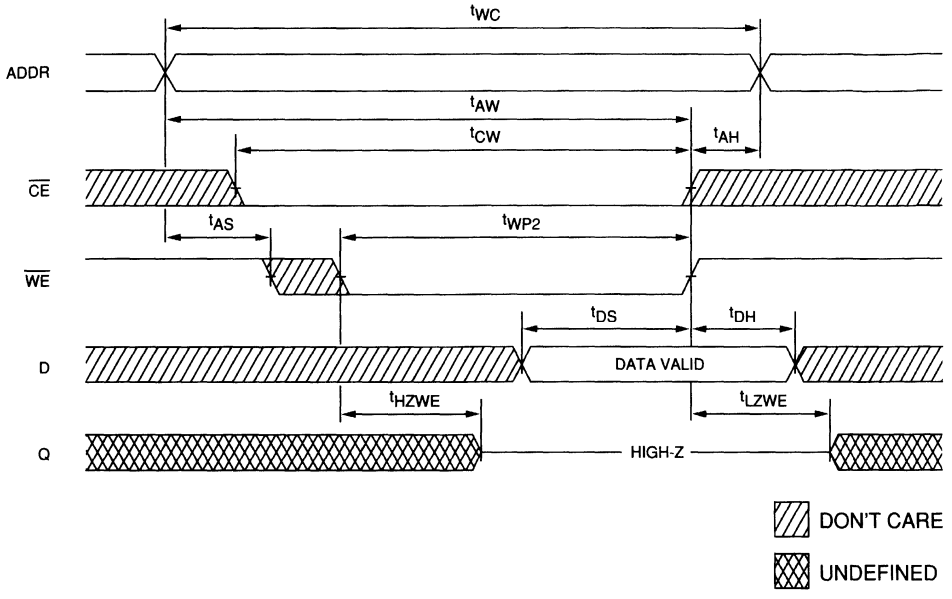


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

16K x 4 SRAM

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

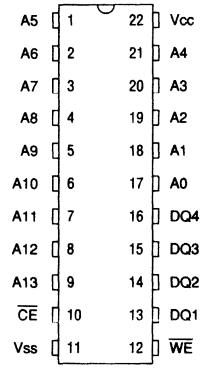
NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- Part Number Example: MT5C6404DJ-15 L XT

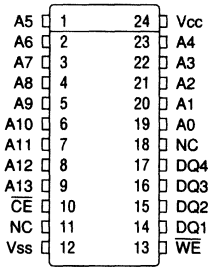
*Preliminary

PIN ASSIGNMENT (Top View)

22-Pin DIP
(SA-2)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

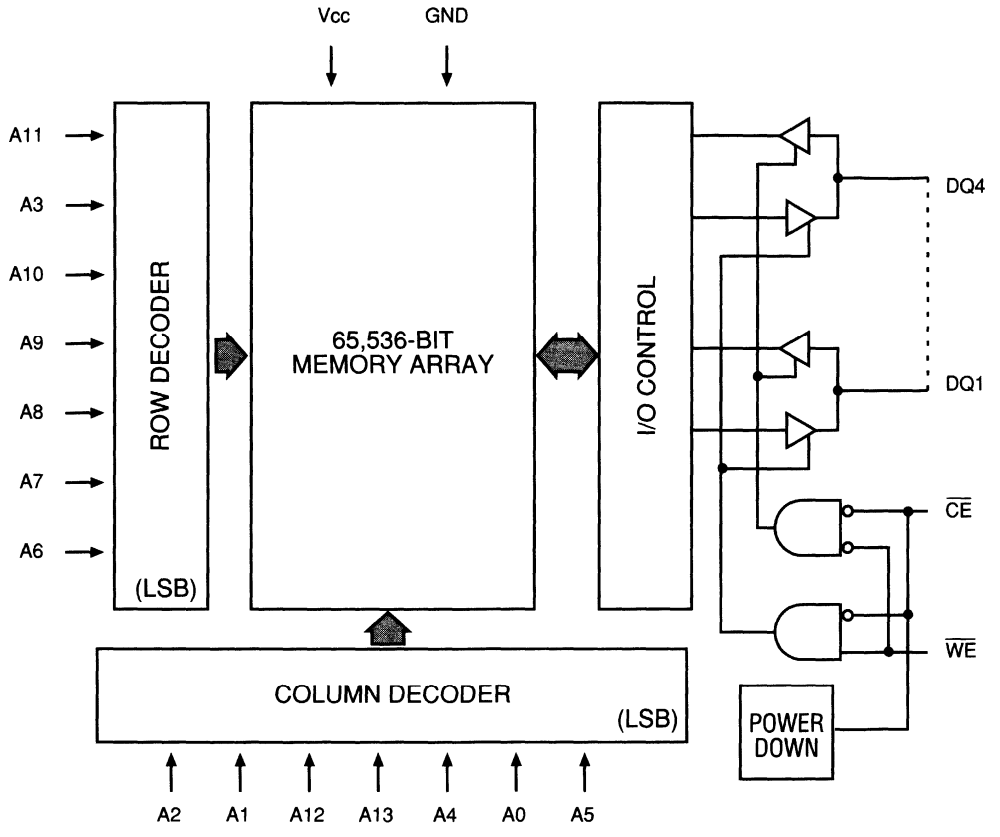
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8+	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	8		10		12		15		20		25		ns	
Address access time	^tAA		8		10		12		15		20		25	ns	
Chip Enable access time	^tACE		7		8		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE†	2		2		2		2		5		5		ns	7, 15
		2		2		2		2		2		2			
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25	ns	
WRITE Cycle															
WRITE cycle time	^tWC	8		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	6.5		8		10		12		15		20		ns	
Address valid to end of write	^tAW	6.5		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	5.5		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	4.5		6		7		8		9		10		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

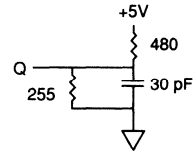


Fig. 1 OUTPUT LOAD EQUIVALENT

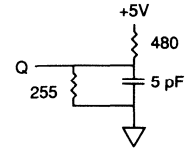


Fig. 2 OUTPUT LOAD EQUIVALENT

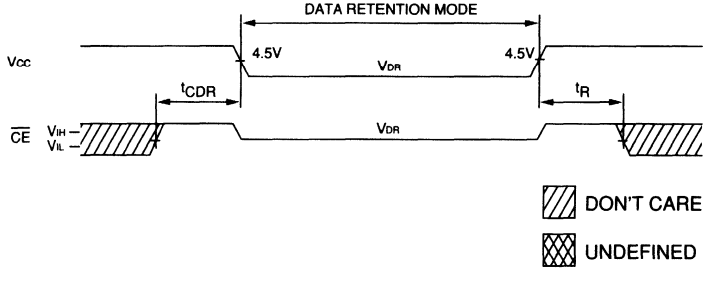
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

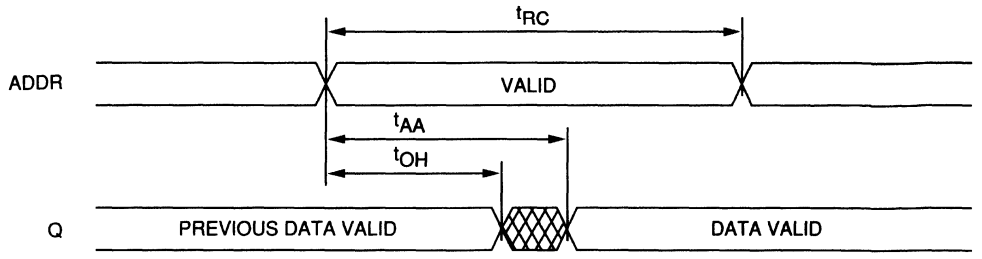
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

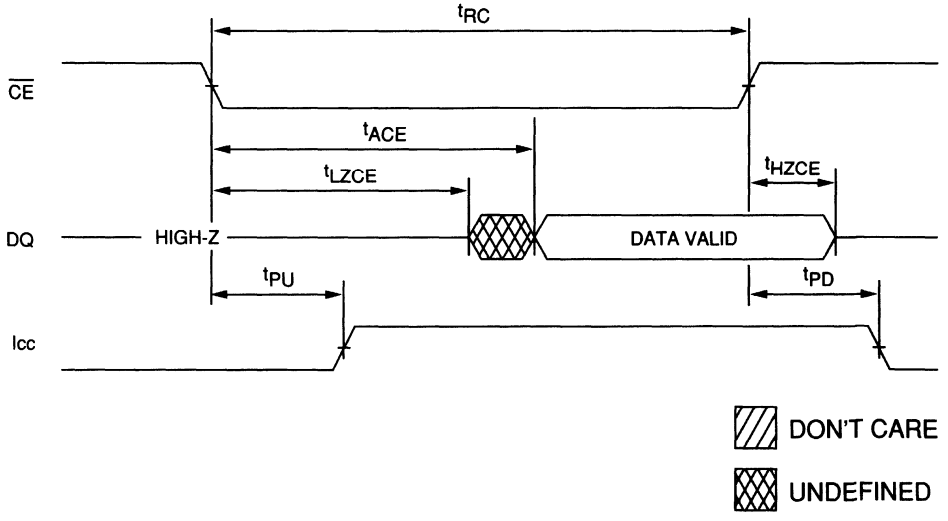
LOW Vcc DATA RETENTION WAVEFORM



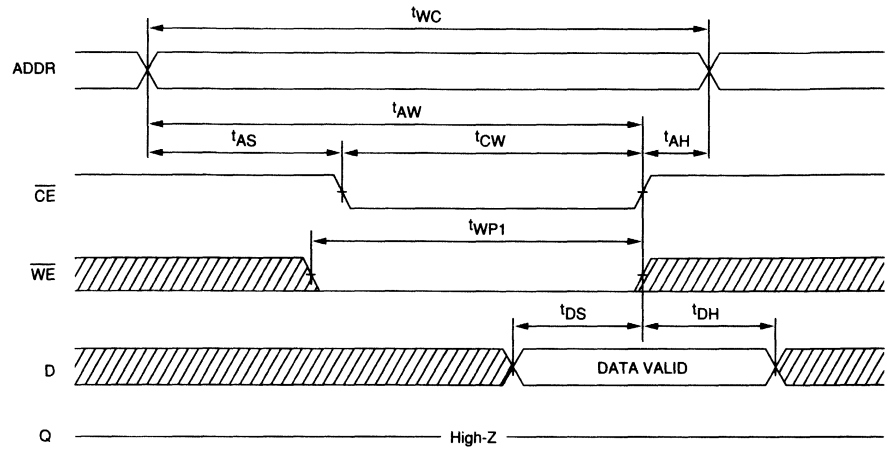
READ CYCLE NO. 1 [8, 9]



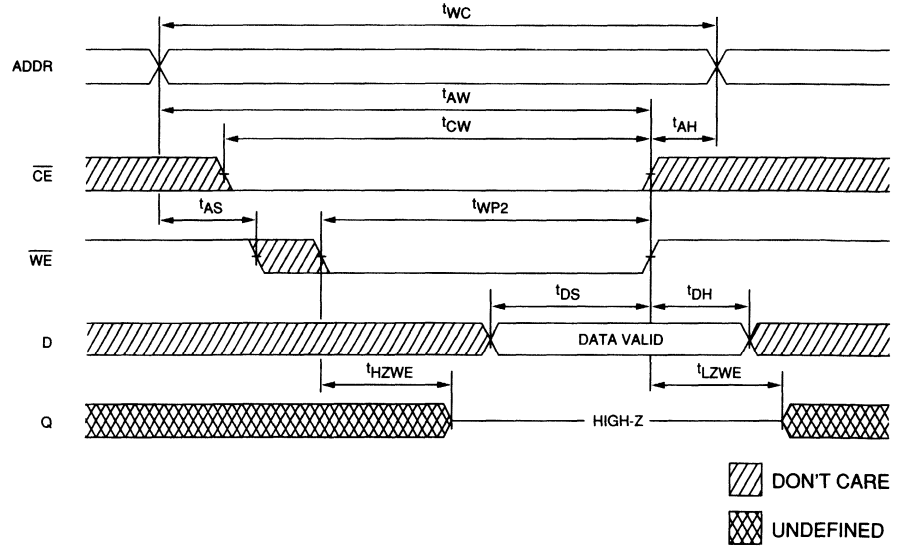
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

16K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS — MARKING

- Timing

8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention — L
- Temperature

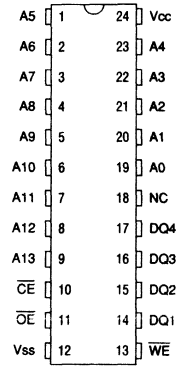
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C6405DJ-15 L IT

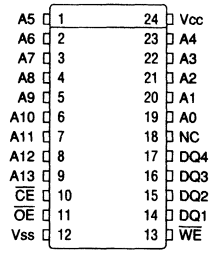
*Preliminary

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

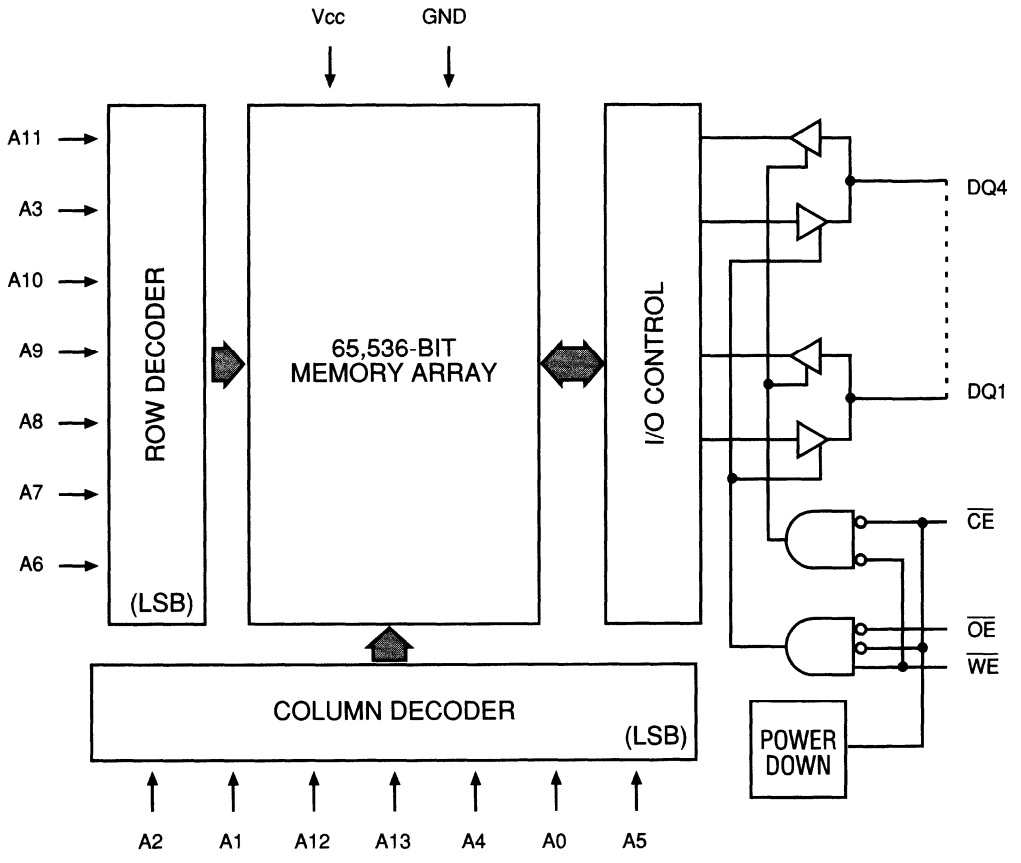
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8+	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	8		10		12		15		20		25		ns	
Address access time	^tAA		8		10		12		15		20		25	ns	
Chip Enable access time	^tACE		7		8		10		12		15		20	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE †	2		2		2		3		5		5		ns	7, 15
		2		2		2		2		2		2			
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25	ns	
Output Enable access time	^tAOE		3.5		4		5		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		3.5		4		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	8		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	6.5		8		10		12		15		20		ns	
Address valid to end of write	^tAW	6.5		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	5.5		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	4.5		6		7		8		9		10		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

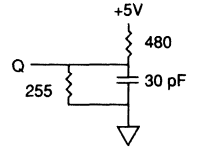


Fig. 1 OUTPUT LOAD EQUIVALENT

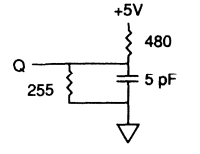


Fig. 2 OUTPUT LOAD EQUIVALENT

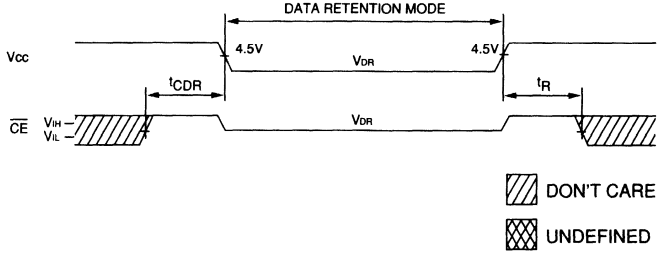
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

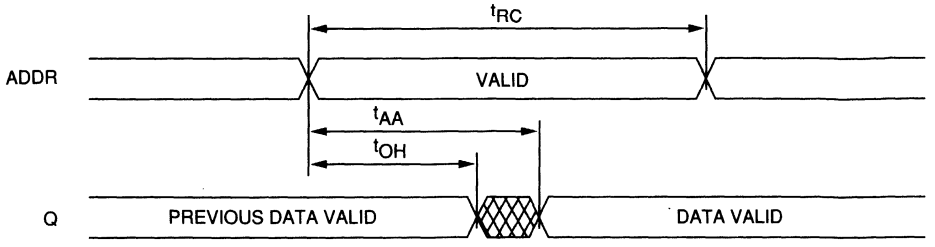
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

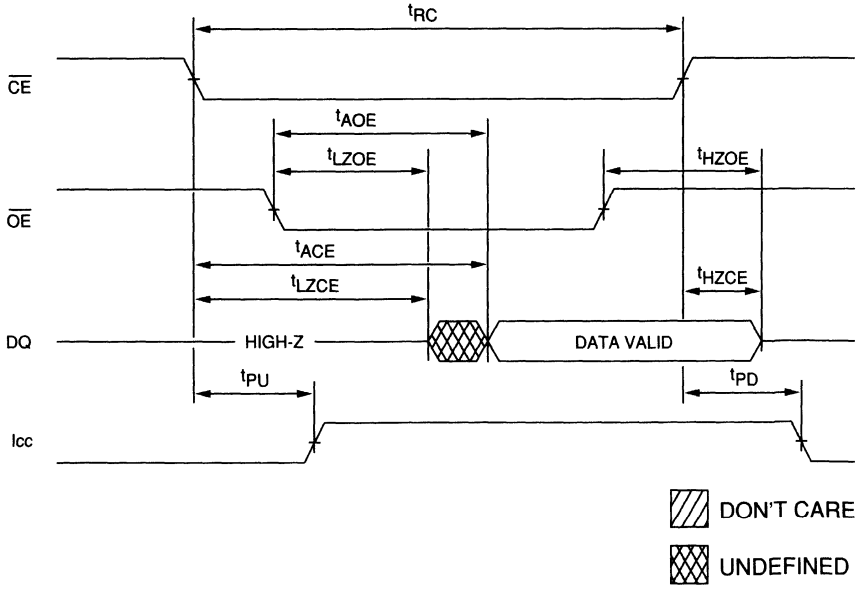
LOW Vcc DATA RETENTION WAVEFORM



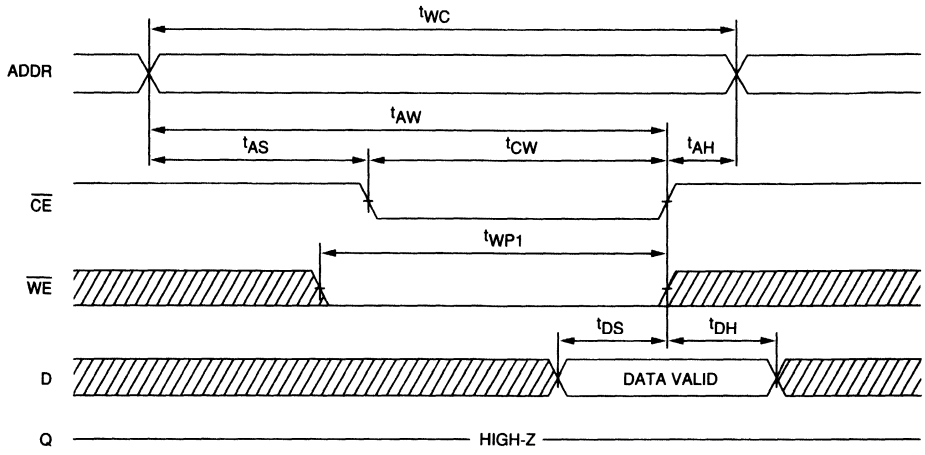
READ CYCLE NO. 1 [8, 9]



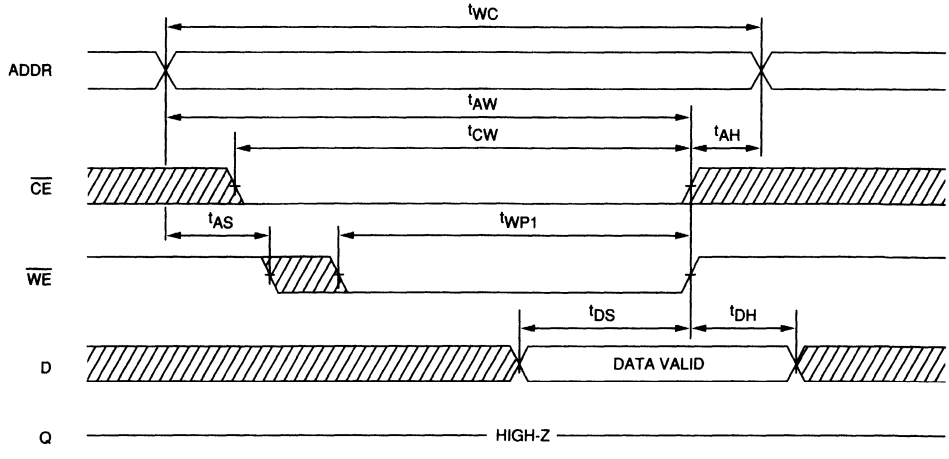
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)

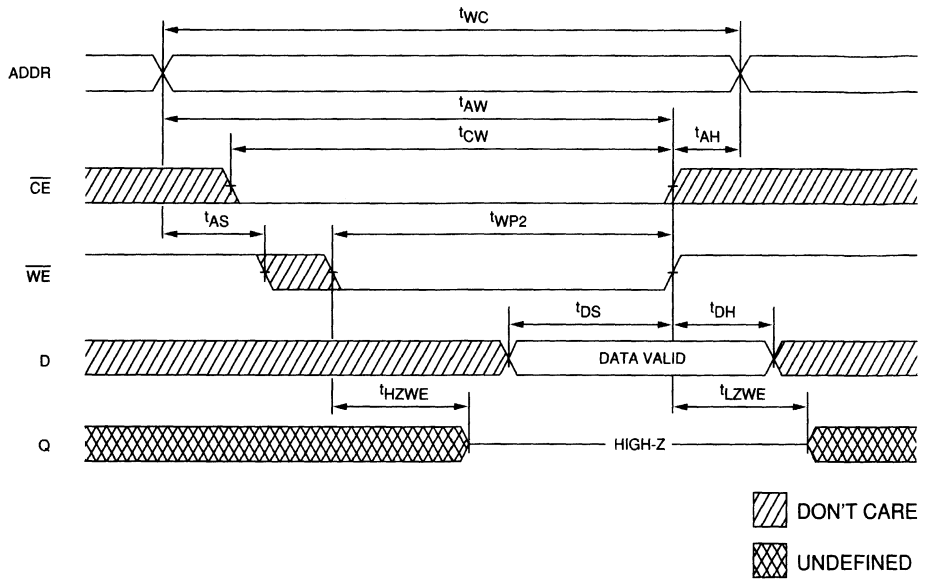


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

64K x 4 SRAM

FEATURES

- High speed: 10*, 12*, 15, 20, 25, and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
10ns access	-10*
12ns access	-12*
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic SOIC (300 mil)	SG

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

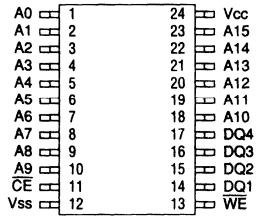
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C2564SG-35 LP XT

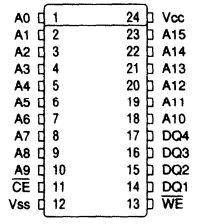
*Preliminary

PIN ASSIGNMENT (Top View)

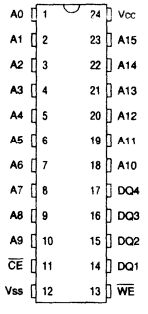
24-Pin SOIC (SF-1)



24-Pin SOJ (SD-1)



24-Pin DIP (SA-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

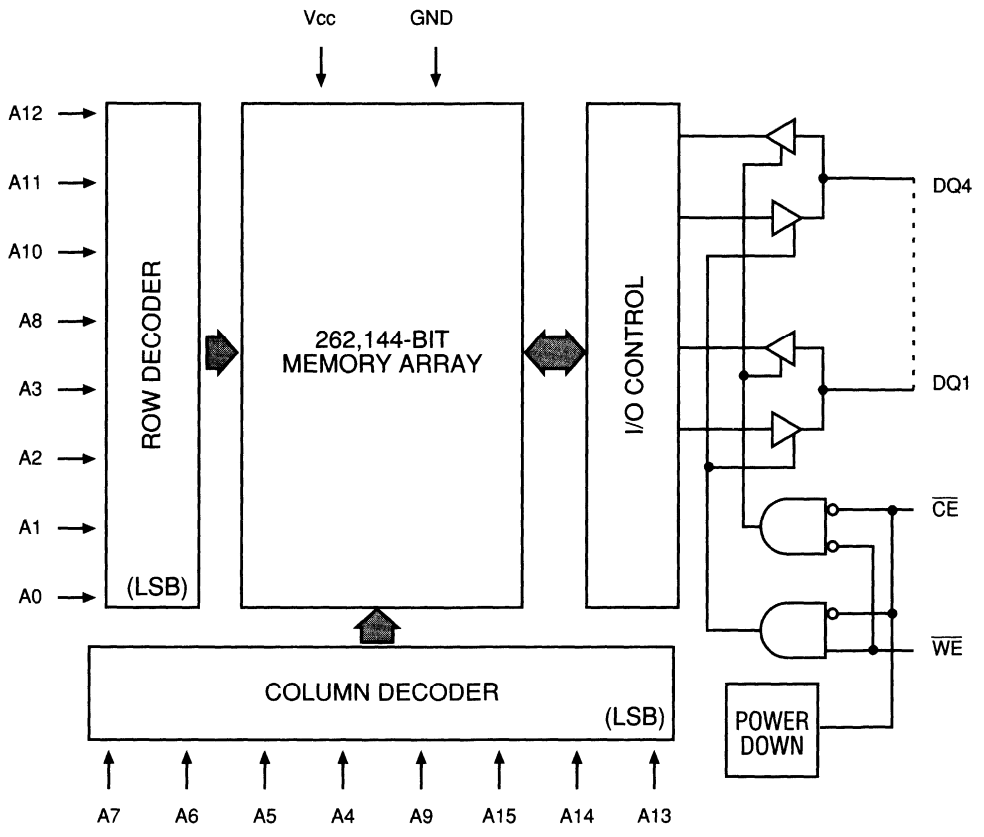
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10+†	-12+†	-15†	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	85	180	160	140	120	110	90	mA	3, 14
	"LP" VERSION	I_{CC}	65	-	-	-	110	100	80	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	11	45	40	30	30	25	25	mA	14
	"LP" VERSION	I_{SB1}	3	-	-	-	7	7	7	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	14

+Preliminary
† LP version not available with this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10*		-12*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	tRC	10		12		15		20		25		35		ns	
Address access time	tAA		10		12		15		20		25		35	ns	
Chip Enable access time	tACE		10		12		15		20		25		35	ns	
Output hold from address change	tOH	2		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	3		4		4		4		6		6		ns	7
Chip disable to output in High-Z	tHZCE		6		8		8		9		9		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		10		12		15		20		25		35	ns	
WRITE Cycle															
WRITE cycle time	tWC	10		12		15		20		25		30		ns	
Chip Enable to end of write	tCW	9		10		10		15		15		20		ns	
Address valid to end of write	tAW	9		10		10		15		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
WRITE pulse width	tWP1	9		10		10		15		15		20		ns	
WRITE pulse width	tWP2	11		12		12		15		15		20		ns	
Data setup time	tDS	6		7		7		10		10		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		4		4		4		5		5		ns	7
Write Enable to output in High-Z	tHZWE		6		7		7		10		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

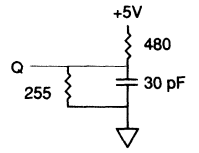


Fig. 1 OUTPUT LOAD EQUIVALENT

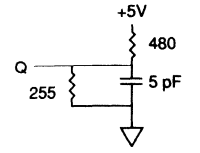


Fig. 2 OUTPUT LOAD EQUIVALENT

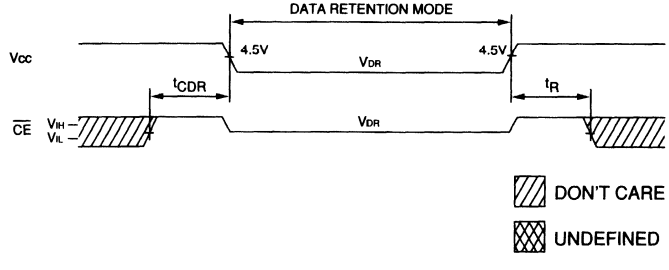
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

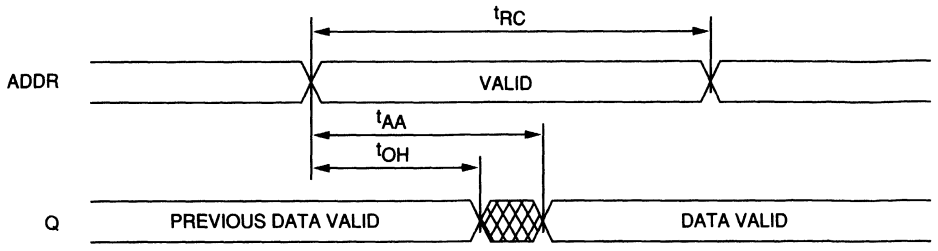
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	300	µA	
		Vcc = 3V	ICCDR		90	500	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

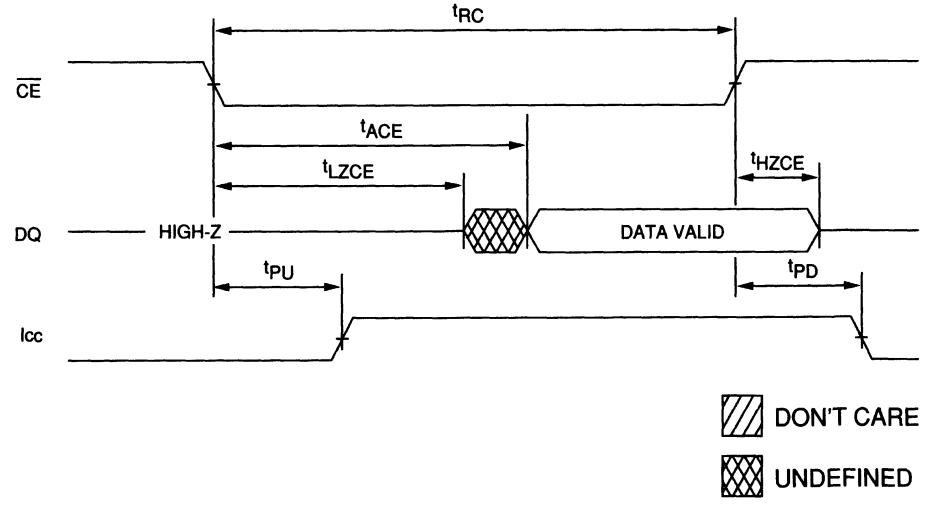
LOW Vcc DATA RETENTION WAVEFORM



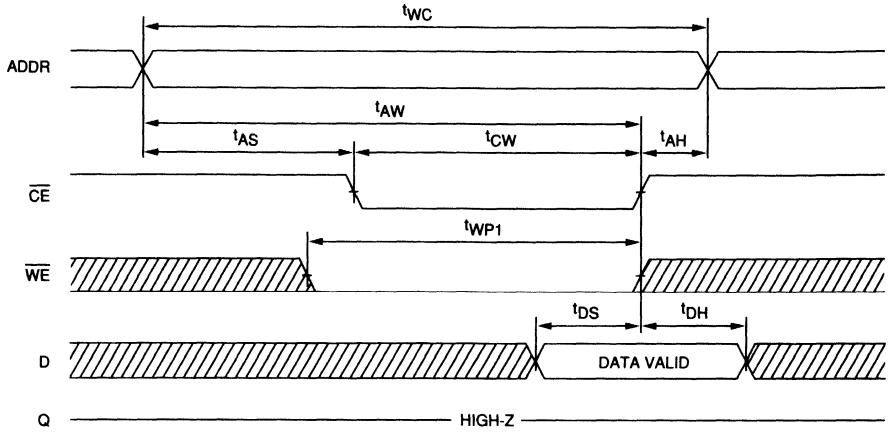
READ CYCLE NO. 1 [8, 9]



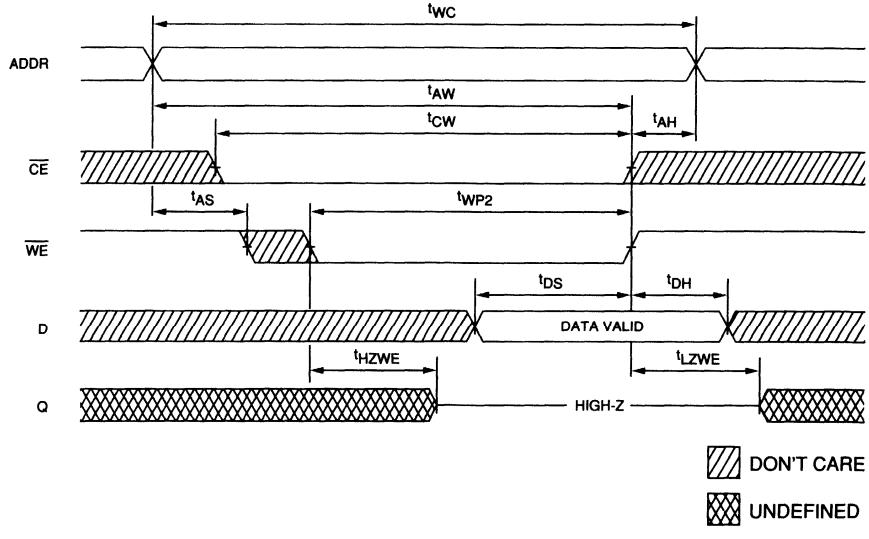
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 10*, 12*, 15, 20, 25, and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS — MARKING

- Timing

10ns access	-10*
12ns access	-12*
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention — L
- 2V data retention, low power — LP
- Temperature

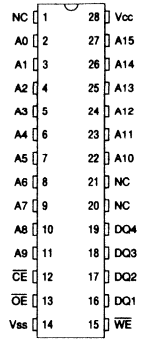
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C2565DJ-35 LP

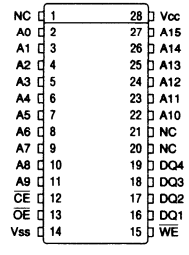
*Preliminary

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



28-Pin SOJ
(SD-2)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

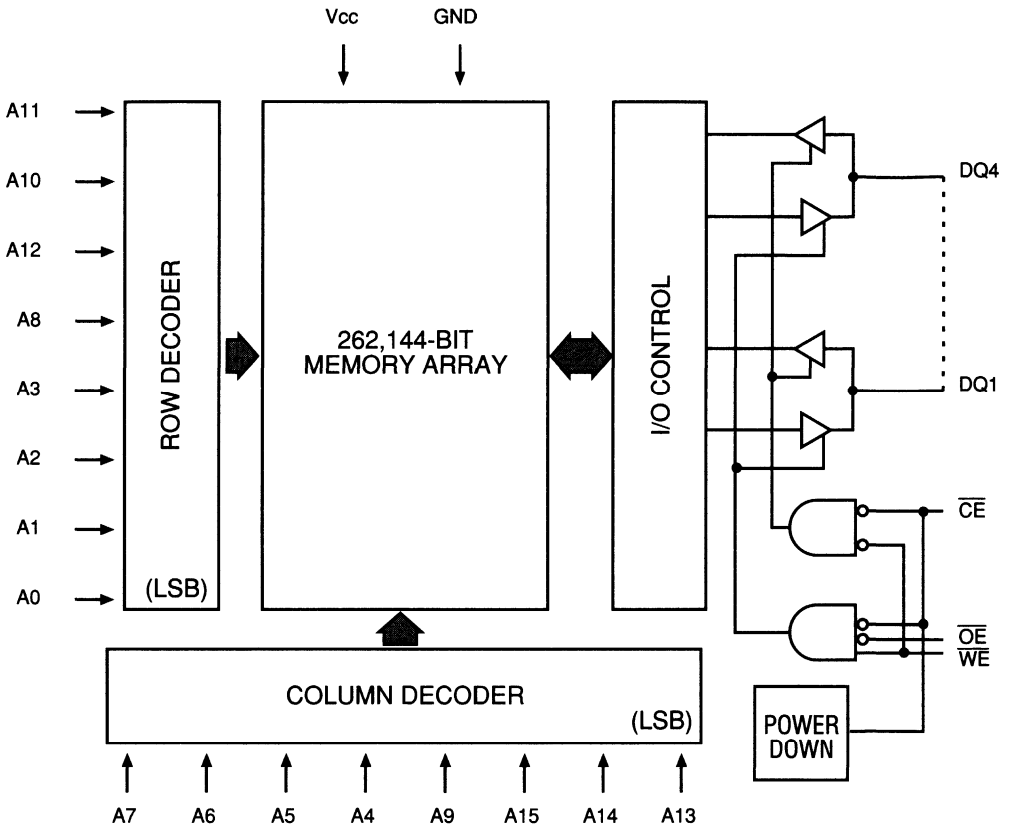
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10+†	-12+†	-15†	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	85	180	160	140	120	110	90	mA	3, 14
	"LP" VERSION	I_{CC}	65	-	-	-	110	100	80	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	11	45	40	30	30	25	25	mA	14
	"LP" VERSION	I_{SB1}	3	-	-	-	7	7	7	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	14

+Preliminary
† LP version not available with this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	7	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION		-10*		-12*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	tRC	10		12		15		20		25		35		ns	
Address access time	tAA		10		12		15		20		25		35	ns	
Chip Enable access time	tACE		10		12		15		20		25		35	ns	
Output hold from address change	tOH	2		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	3		4		4		4		6		6		ns	7
Chip disable to output in High-Z	tHZCE		6		8		8		9		9		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		10		12		15		20		25		35	ns	
Output Enable access time	tAOE		6		8		8		8		8		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	tHZOE		5		6		6		7		7		12	ns	6
WRITE Cycle															
WRITE cycle time	tWC	10		12		15		20		25		30		ns	
Chip Enable to end of write	tCW	9		10		10		15		15		20		ns	
Address valid to end of write	tAW	9		10		10		15		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
WRITE pulse width	tWP1	9		10		10		15		15		20		ns	
WRITE pulse width	tWP2	11		12		12		15		15		20		ns	
Data setup time	tDS	6		7		7		10		10		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		4		4		4		5		5		ns	7
Write Enable to output in High-Z	tHZWE		6		7		7		10		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

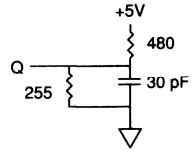


Fig. 1 OUTPUT LOAD EQUIVALENT

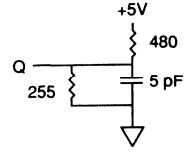


Fig. 2 OUTPUT LOAD EQUIVALENT

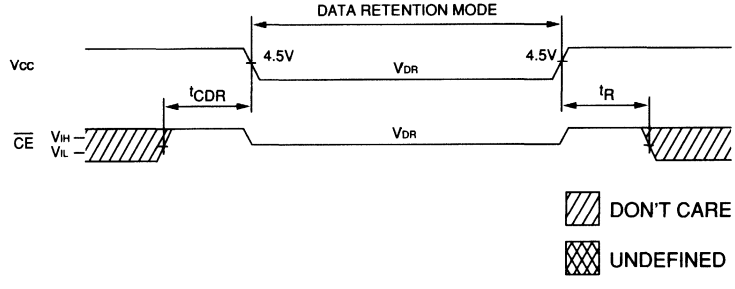
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

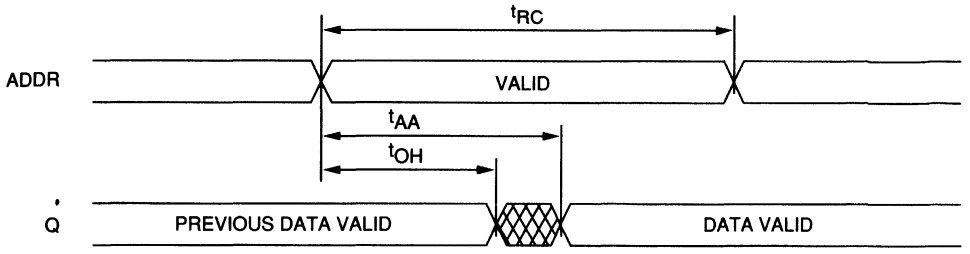
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	300	µA	
		Vcc = 3V	ICCDR		90	500	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

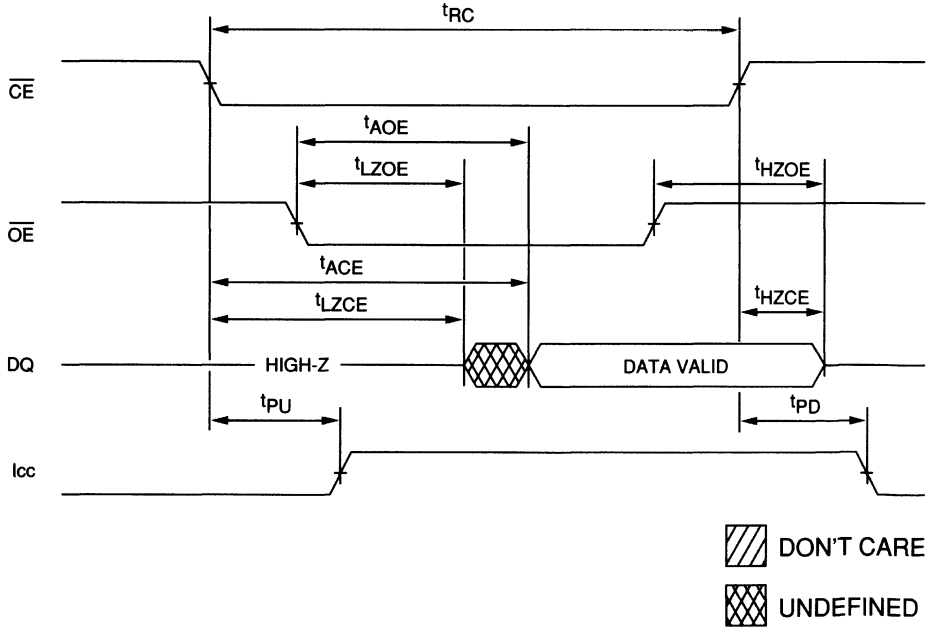
LOW Vcc DATA RETENTION WAVEFORM



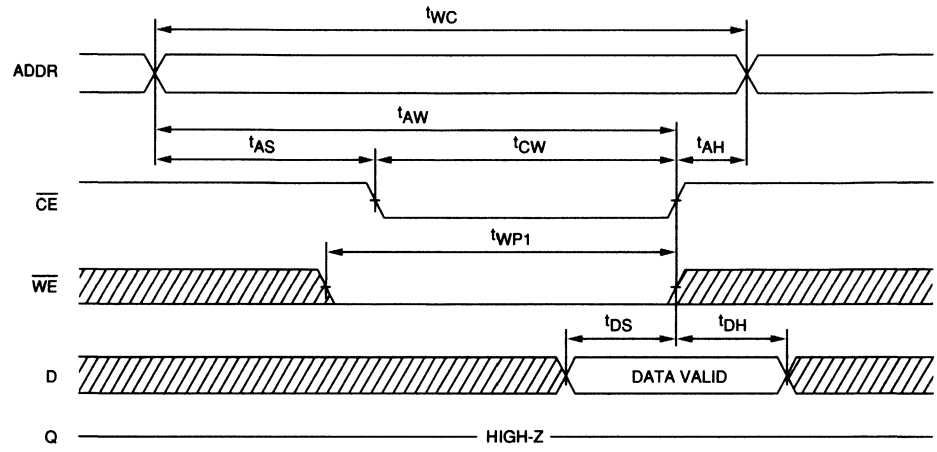
READ CYCLE NO. 1 [8, 9]



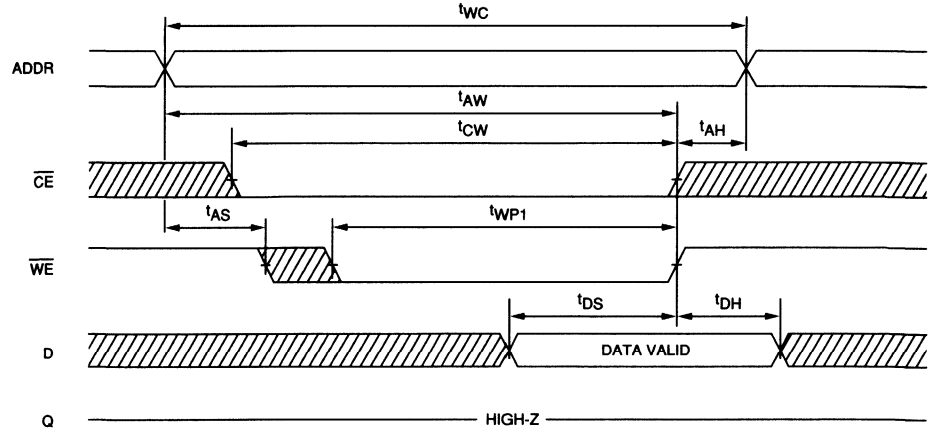
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)

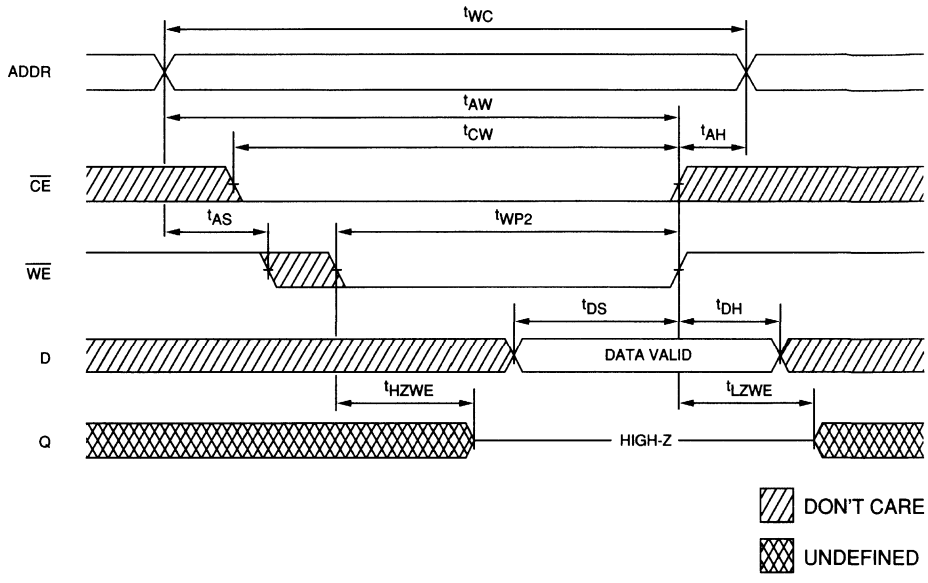


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12*, 15*, 17, 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS

	MARKING
• Timing	
12ns access	-12*
15ns access	-15*
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

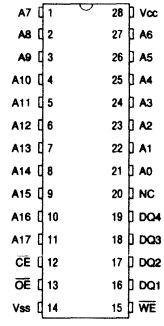
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C1005DJ-25 L IT

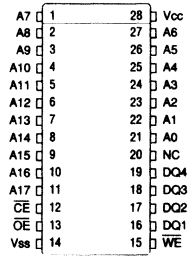
*Preliminary

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

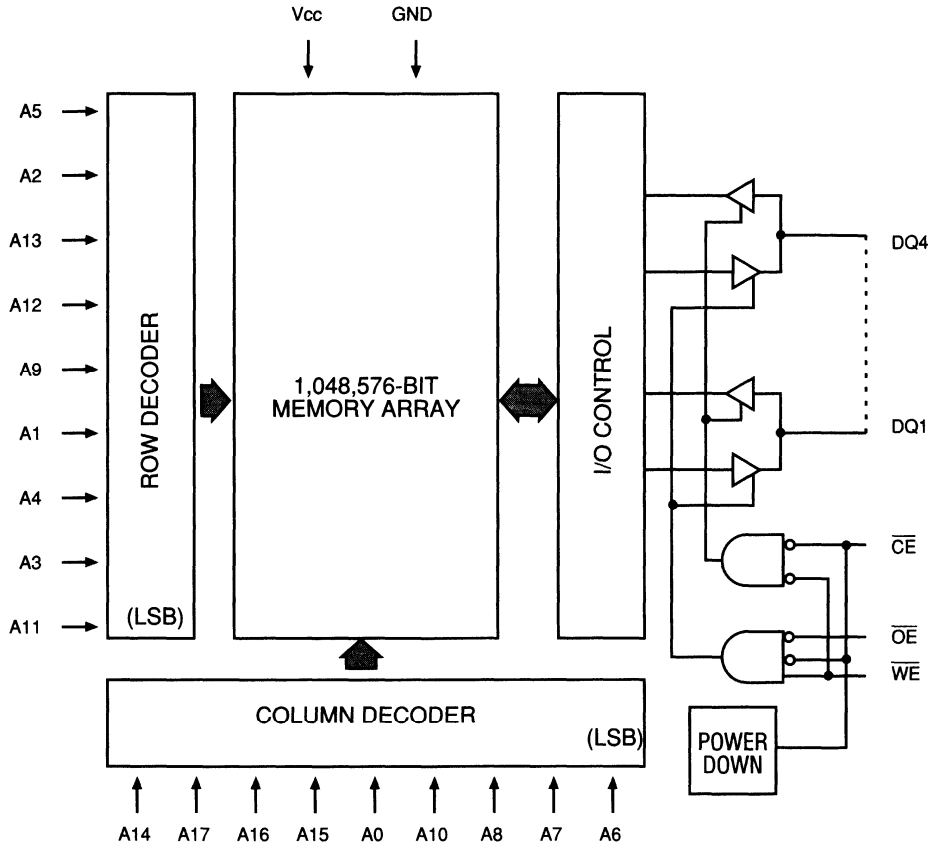
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A11 and A3) are encoded using a Gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12*	-15*	-17	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	95	190	165	155	140	125	115	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	17	45	40	40	35	30	25	25	mA	14
	"LP" Version Only	I_{SB1}	1.3	3	3	3	3	3	3	3	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	5	5	5	mA	14
	"L" and "LP" Versions Only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	14

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION		-12*		-15*		-17		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	tRC	12		15		17		20		25		35		45		ns	
Address access time	tAA		12		15		17		20		25		35		45	ns	
Chip Enable access time	tACE		12		15		17		20		25		35		45	ns	
Output hold from address change	tOH	3		3		3		3		5		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	3		5		5		5		5		5		5		ns	7
Chip disable to output in High-Z	tHZCE		5		6		7		8		10		15		18	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		12		15		17		20		25		35		45	ns	
Output Enable access time	tAOE		4		5		5		6		8		12		15	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		4		5		5		6		10		12		15	ns	6
WRITE Cycle																	
WRITE cycle time	tWC	12		15		17		20		25		35		45		ns	
Chip Enable to end of write	tCW	8		10		12		12		15		20		25		ns	
Address valid to end of write	tAW	8		10		12		12		15		20		25		ns	
Address setup time	tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	tWP1	8		9		12		12		15		20		25		ns	
WRITE pulse width	tWP2	10		12		8		15		15		20		25		ns	
Data setup time	tDS	6		7		7		8		10		15		20		ns	
Data hold time	tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	tHZWE		5		6		7		8		10		15		18	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

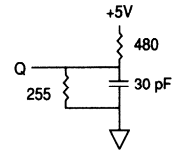


Fig. 1 OUTPUT LOAD EQUIVALENT

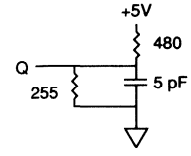


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

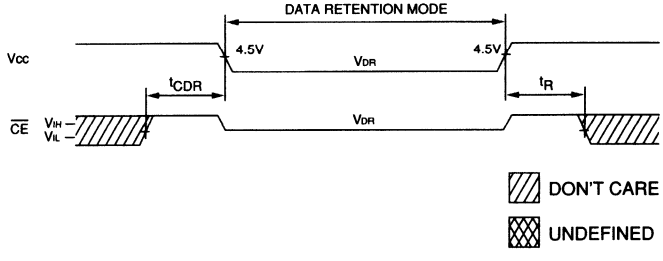
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

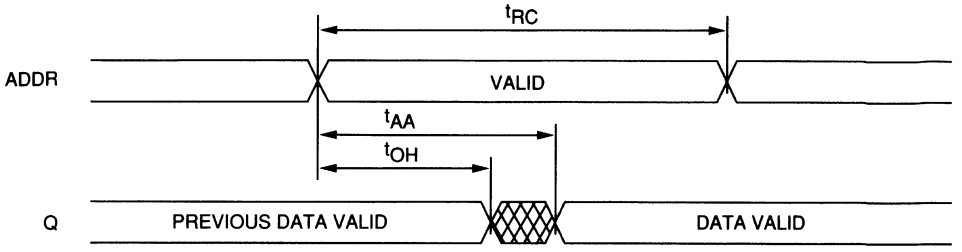
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		35	150	µA	
	VIN ≥ (Vcc -0.2V)	Vcc = 3V			60	400	µA	
	or ≤ 0.2V	Vcc = 3V*			30	100	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

*Preliminary

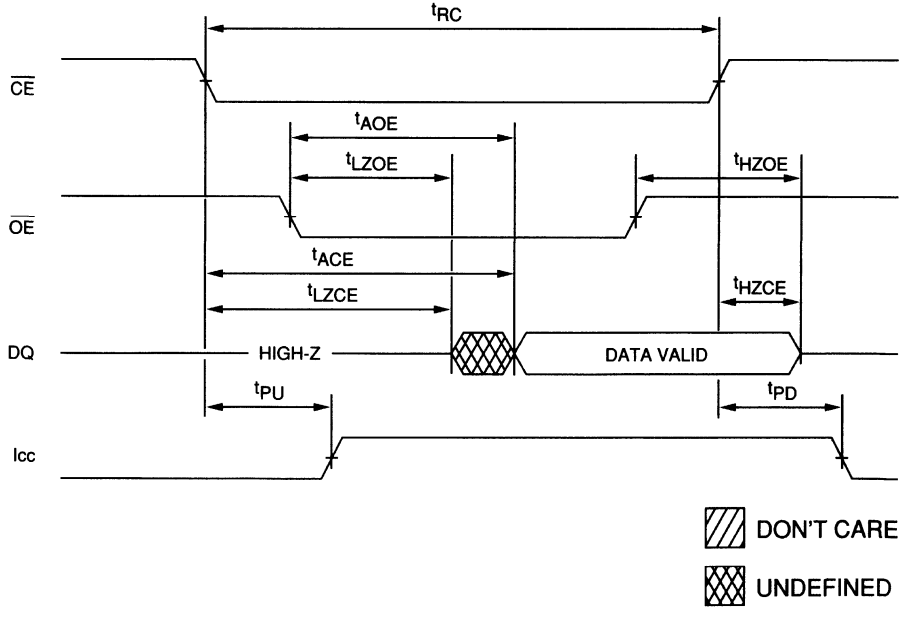
LOW Vcc DATA RETENTION WAVEFORM



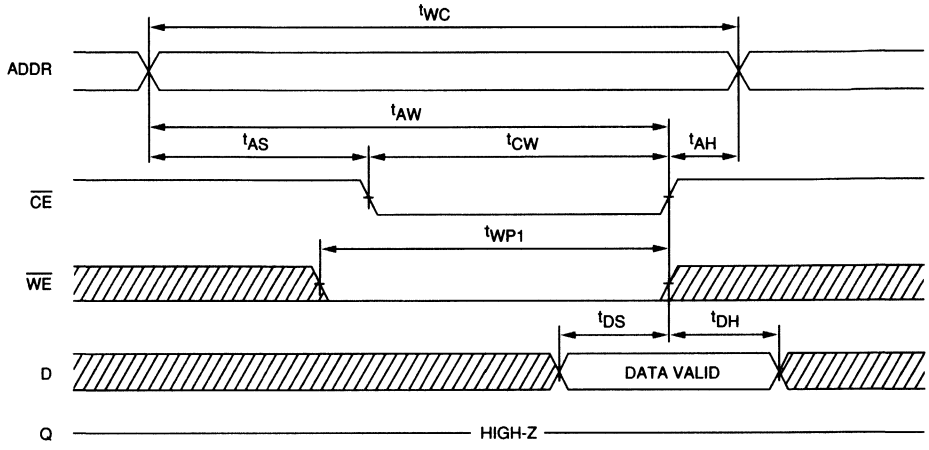
READ CYCLE NO. 1 [8, 9]



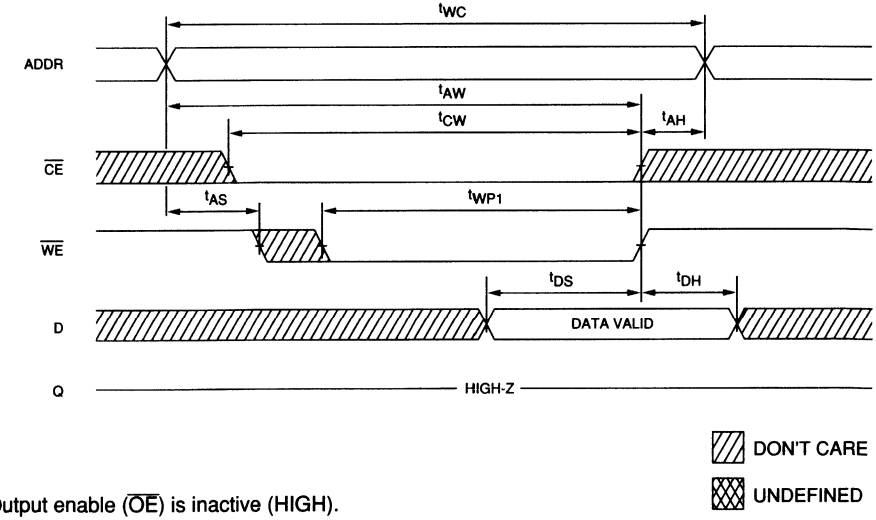
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

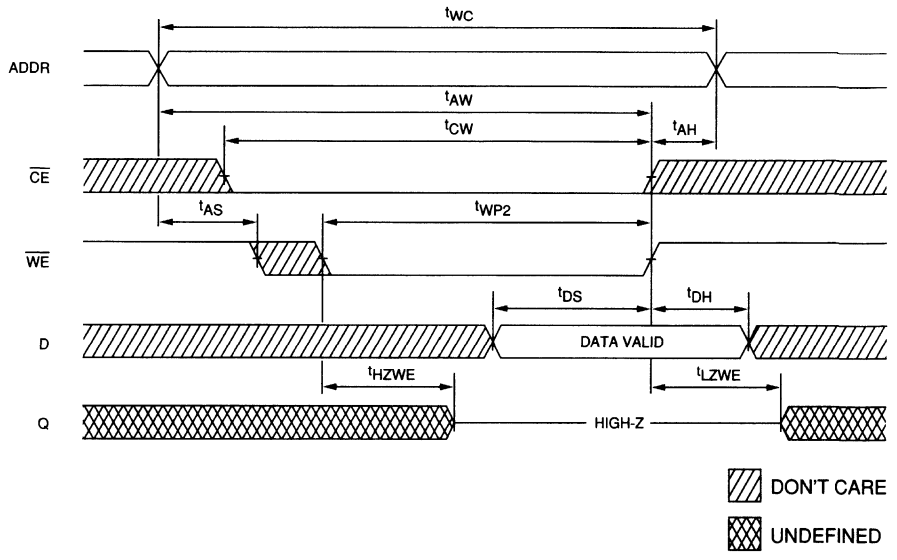


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

WITH SINGLE CHIP ENABLE, CENTER POWER AND GROUND PINS

FEATURES

- High speed: 12, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast $\overline{OE}$ access times: 6, 8, 10 and 12ns

OPTIONS MARKING

- Timing

12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

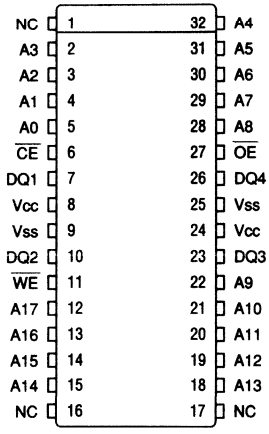
- Packages

32-pin SOJ (400 mil)	DJ

- Part Number Example: MT5C256K4A1DJ-12

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

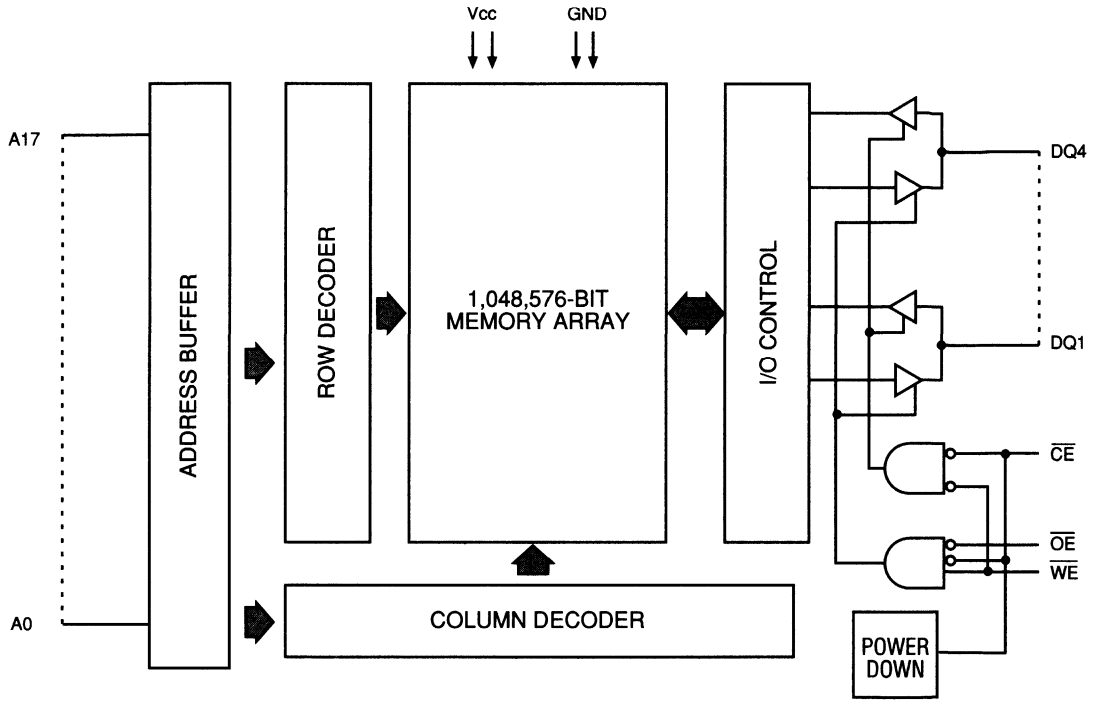
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 32, 31, 30, 29, 28, 22, 21, 20, 19, 18, 15, 14, 13, 12	A0-A17	Input	Address Inputs: These inputs determine which cell is addressed.
11	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
6	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
27	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
7, 10, 23, 26	DQ1-DQ4	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 5V ±10%
9, 25	Vss	Supply	Ground: GND
1, 16, 17	NC	-	No Connect: These signals are not internally connected.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply relative to Vss ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.7W
Short Circuit Output Current 50mA
Voltage on any pin relative to Vss ..... -1V to Vcc +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	150	300	260	220	200	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	25	50	45	40	35	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	7		9		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	7		9		10		12		ns	
WRITE pulse width	$^tWP2$	7		9		10		12		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

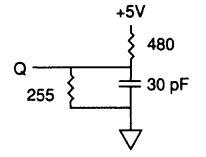


Fig. 1 OUTPUT LOAD EQUIVALENT

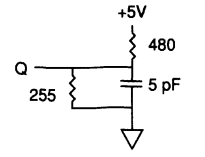
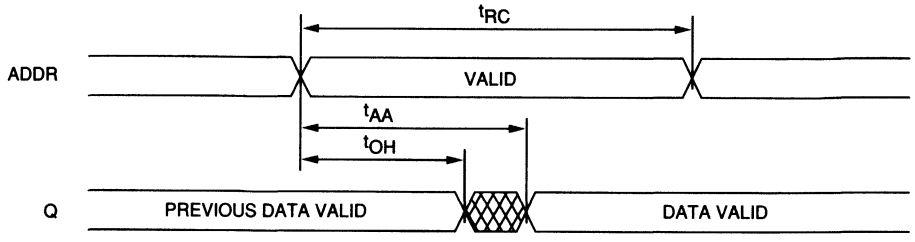


Fig. 2 OUTPUT LOAD EQUIVALENT

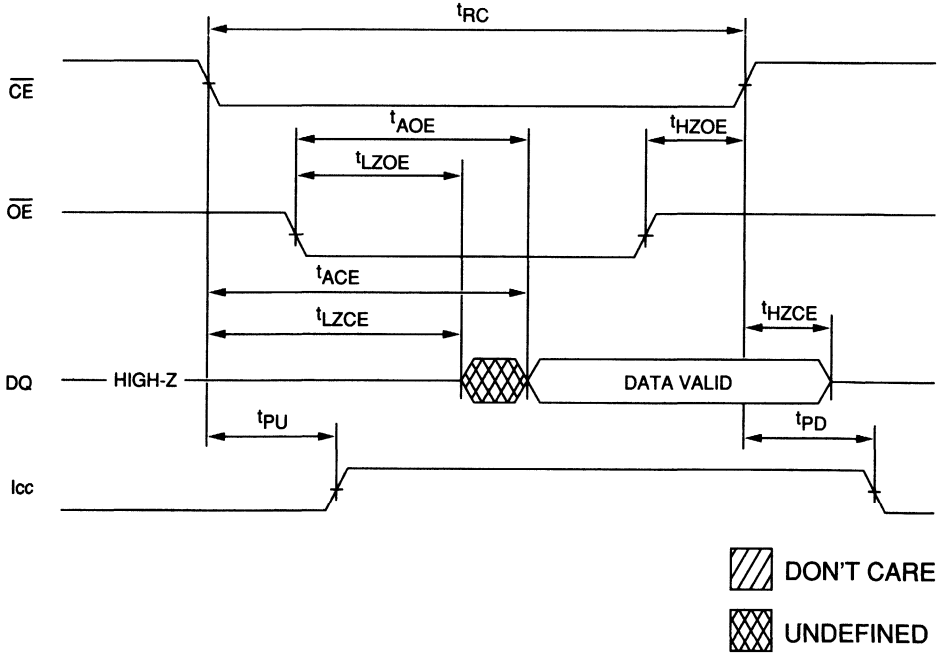
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}HZCE$, $^{t}HZOE$ and $^{t}HZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, and $^{t}HZWE$ is less than $^{t}LZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.

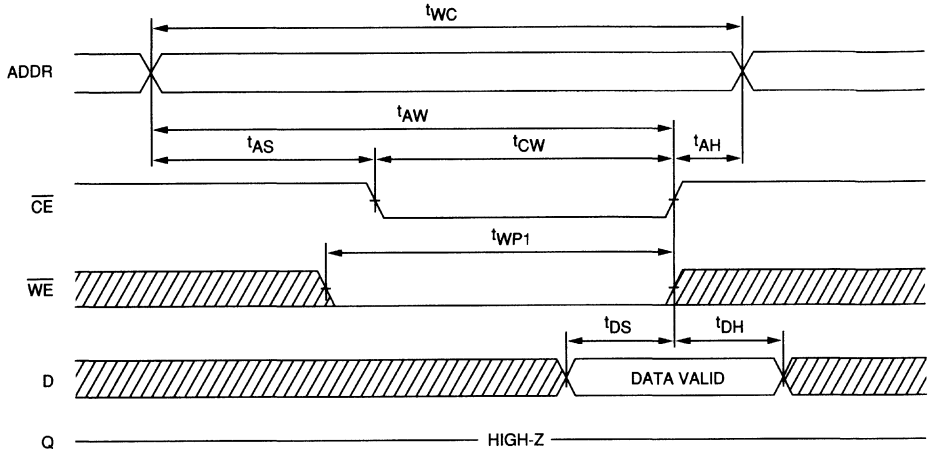
READ CYCLE NO. 1 [8, 9]



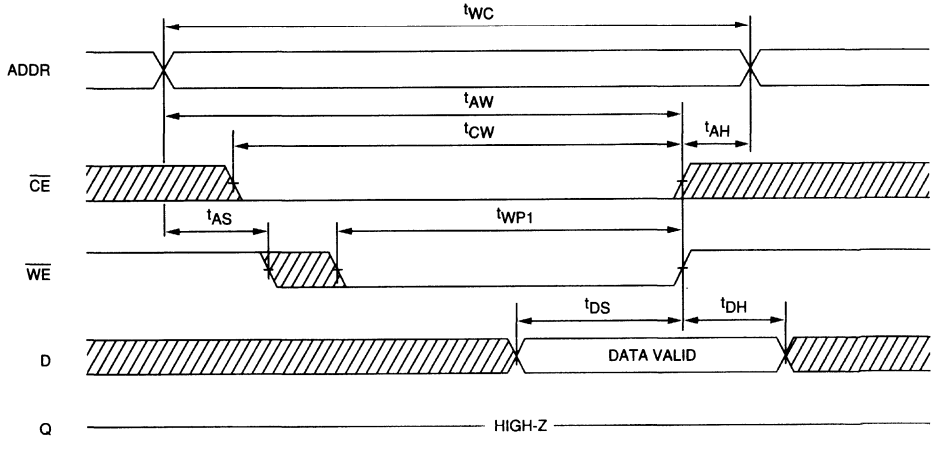
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

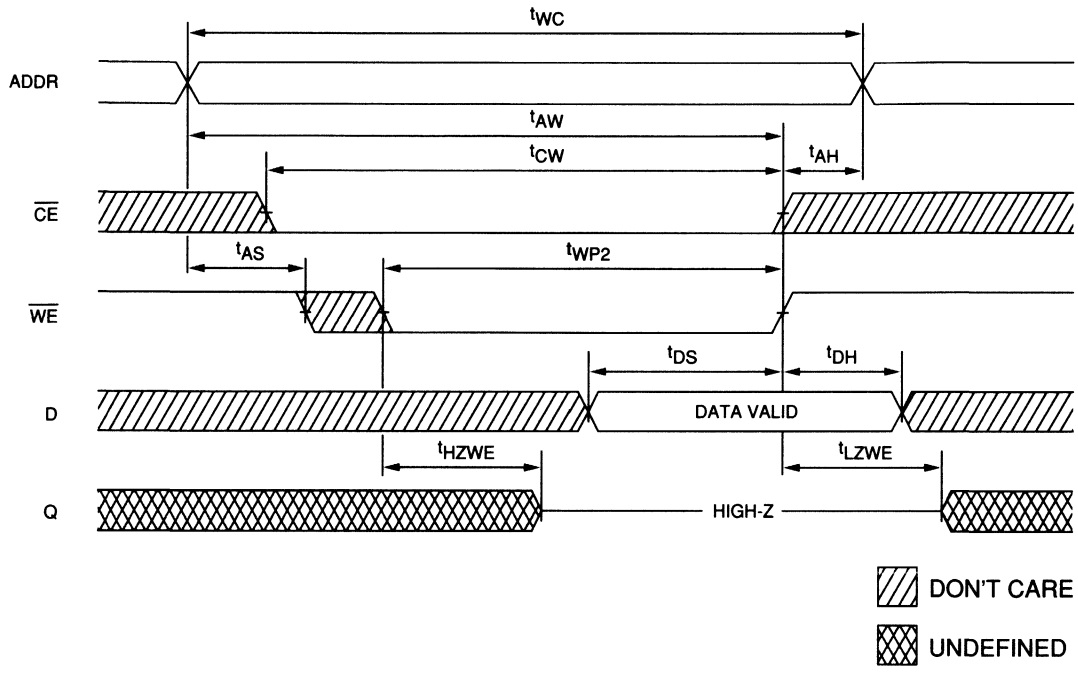


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON

MT5C256K4A1
REVOLUTIONARY PINOUT 256K x 4 SRAM

NEW 5 VOLT SRAM

SRAM

1 MEG x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, 35 and 55ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS

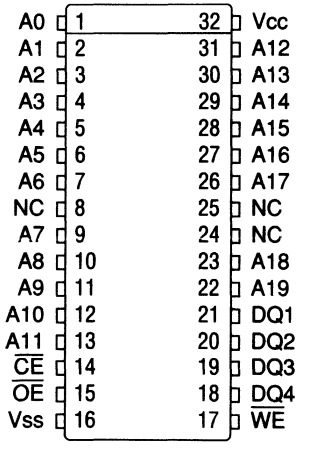
	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
55ns access	-55
• Packages	
Plastic SOJ (400 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- Part Number Example: MT5C1M4A1DJ-20 L IT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) in this configuration. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

SRAM

1 MEG x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 6ns

OPTIONS MARKING

- Timing

20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention L
- 2V data retention, low power LP

- Part Number Example: MT5C1M4B2DJ-35 LP

GENERAL DESCRIPTION

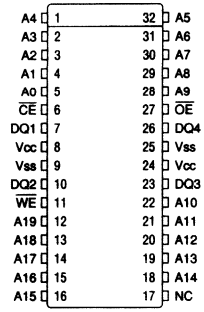
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this configuration. This enhancement can place the outputs in High-Z for additional flexibility in system design.

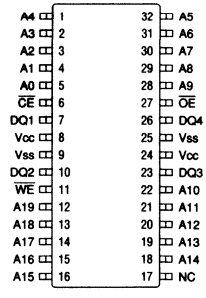
Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



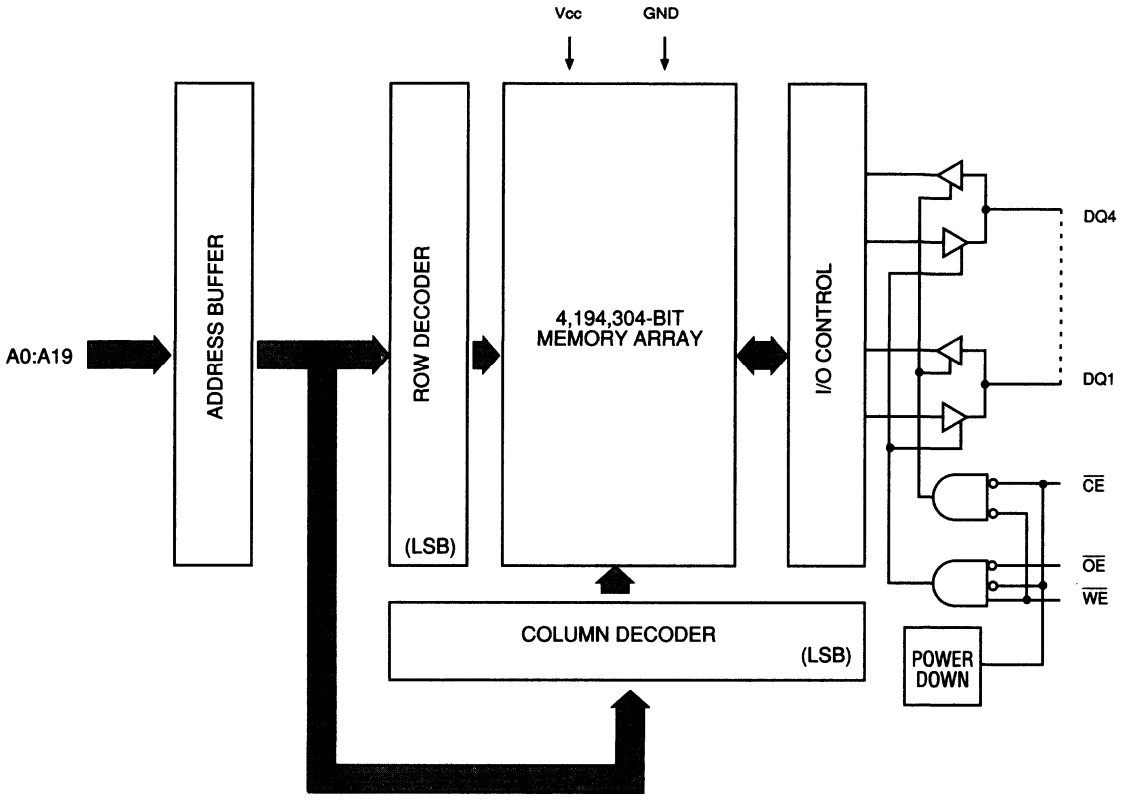
32-Pin TSOP
(SE-1)



The "LP" version provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE	CE	WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-2	2	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-2	2	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	140	120	115	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	35	30	25	mA	
	"LP" Version Only	I_{SB1}	2	2	2	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	2	2	2	mA	
	"L" and "LP" Versions Only	I_{SB2}	2	2	2	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		35		ns	
Address access time	^tAA		20		25		35	ns	
Chip Enable access time	^tACE		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		10		12	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		25		35		ns	
Chip Enable to end of write	^tCW	12		15		20		ns	
Address valid to end of write	^tAW	12		15		20		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		ns	
WRITE pulse width	$^tWP2$	15		15		20		ns	
Data setup time	^tDS	8		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

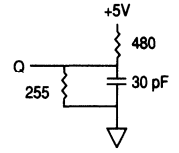


Fig. 1 OUTPUT LOAD EQUIVALENT

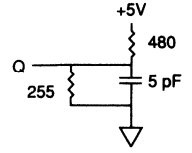


Fig. 2 OUTPUT LOAD EQUIVALENT

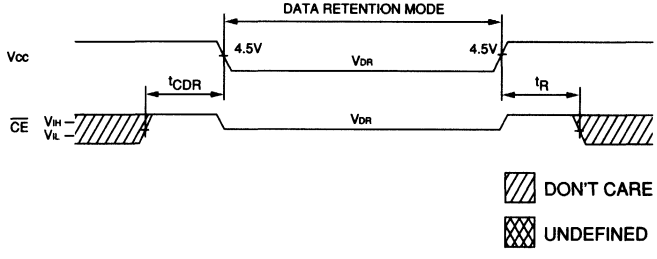
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.

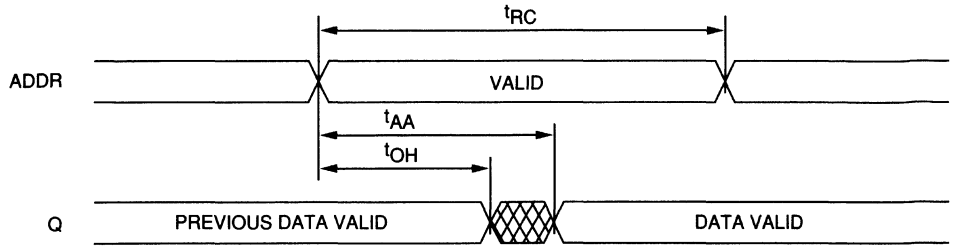
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		200	µA	
		Vcc = 3V			300	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		ns	4
Operation Recovery Time			^{t}R	^{t}RC		ns	4, 11

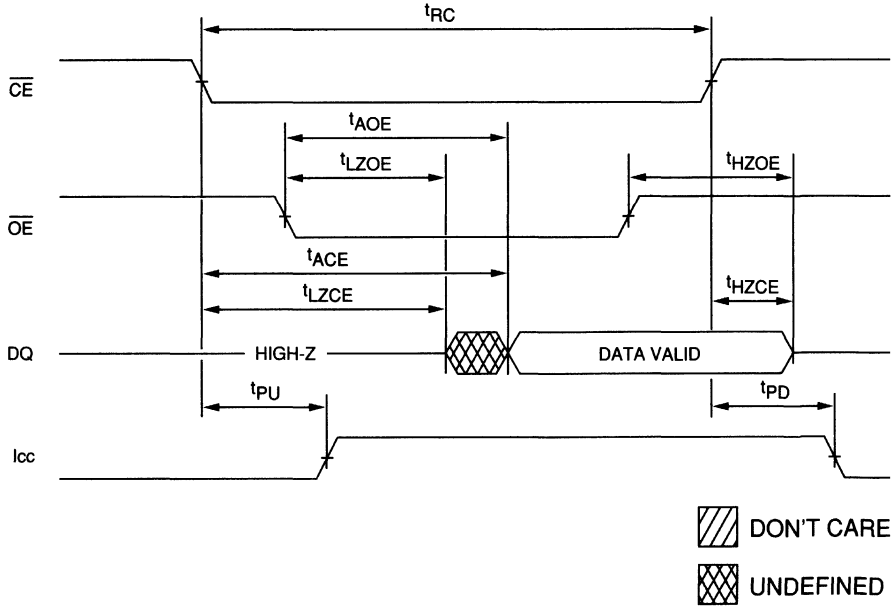
LOW Vcc DATA RETENTION WAVEFORM



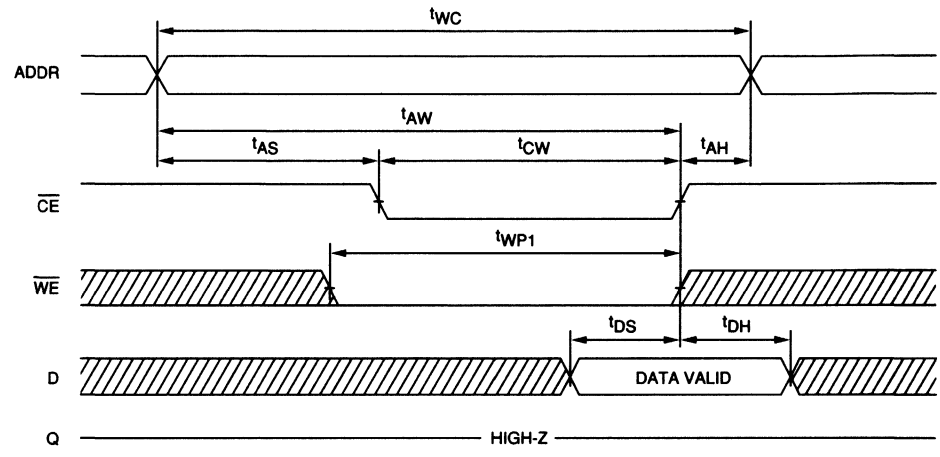
READ CYCLE NO. 1 [8, 9]



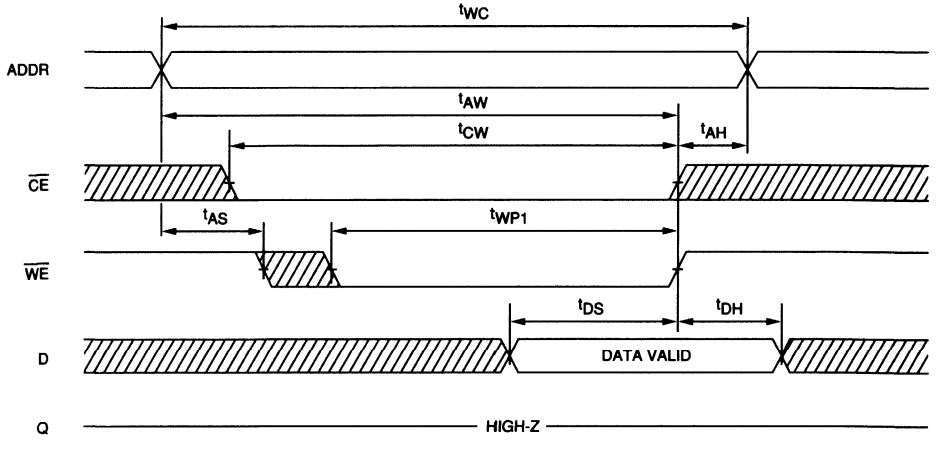
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

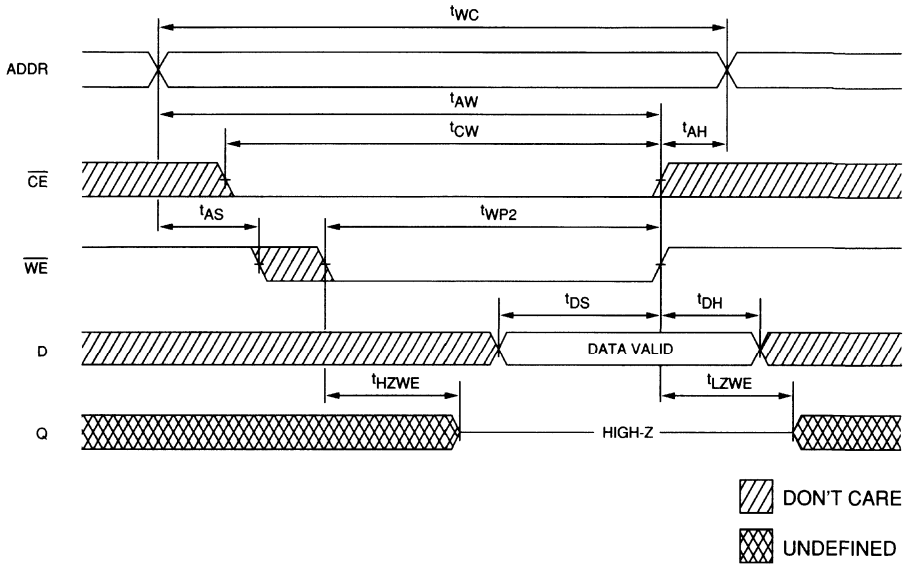


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

2K x 8 SRAM

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

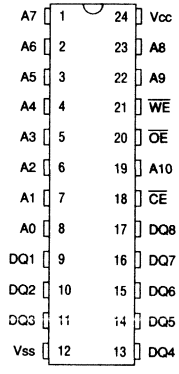
NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- Part Number Example: MT5C1608DJ-8 L IT

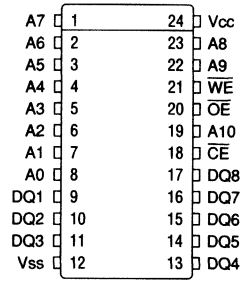
*Preliminary

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

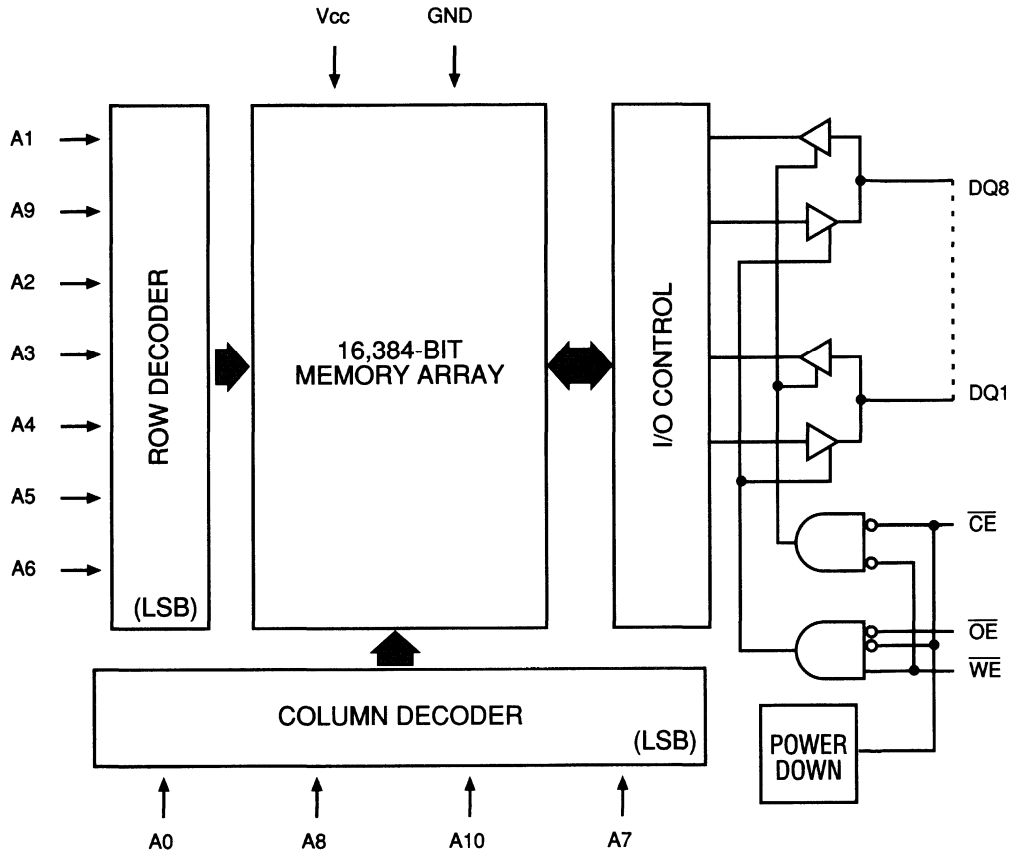
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8+	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

5 VOLT SRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	8		10		12		15		20		25		ns	
Address access time	t_{AA}		8		10		12		15		20		25	ns	
Chip Enable access time	t_{ACE}		7		8		10		12		15		20	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}†	2		2		2		2		2		2		ns	7, 15
Chip disable to output in High-Z	t_{HZCE}		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		8		10		12		15		20		25	ns	
Output Enable access time	t_{AOE}		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		4.5		5		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	8		10		12		15		20		25		ns	
Chip Enable to end of write	t_{CW}	6.5		8		10		12		15		20		ns	
Address valid to end of write	t_{AW}	6.5		8		10		12		15		20		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
WRITE pulse width	t_{WP1}	5.5		7		8		10		12		15		ns	
WRITE pulse width	t_{WP2}	8		9		10		14		18		20		ns	
Data setup time	t_{DS}	4.5		6		7		8		9		10		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	t_{HZWE}		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

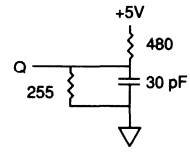


Fig. 1 OUTPUT LOAD EQUIVALENT

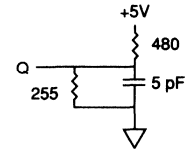


Fig. 2 OUTPUT LOAD EQUIVALENT

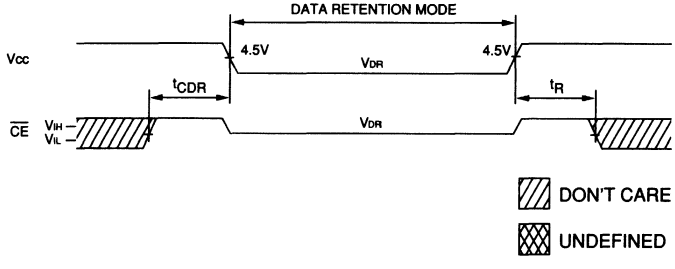
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

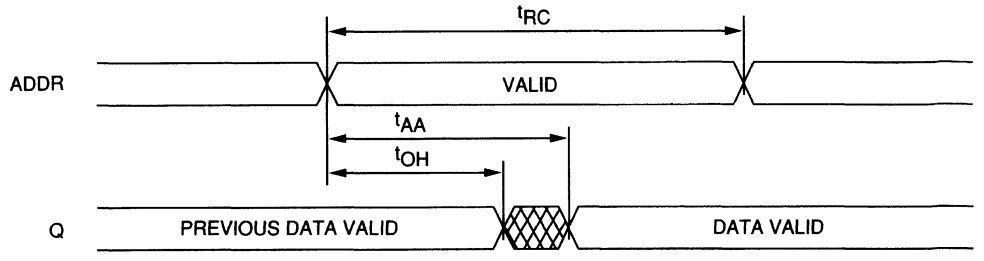
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

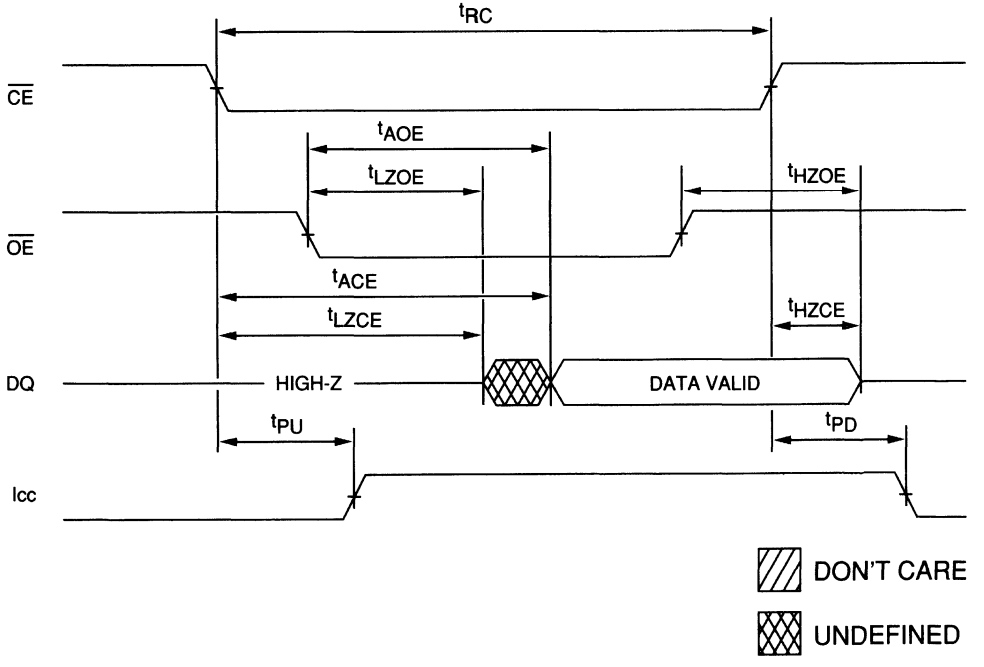
LOW Vcc DATA RETENTION WAVEFORM



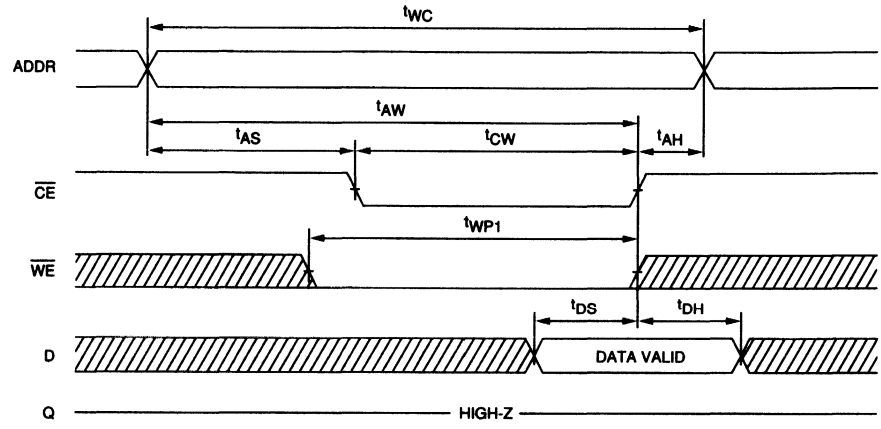
READ CYCLE NO. 1 [8, 9]



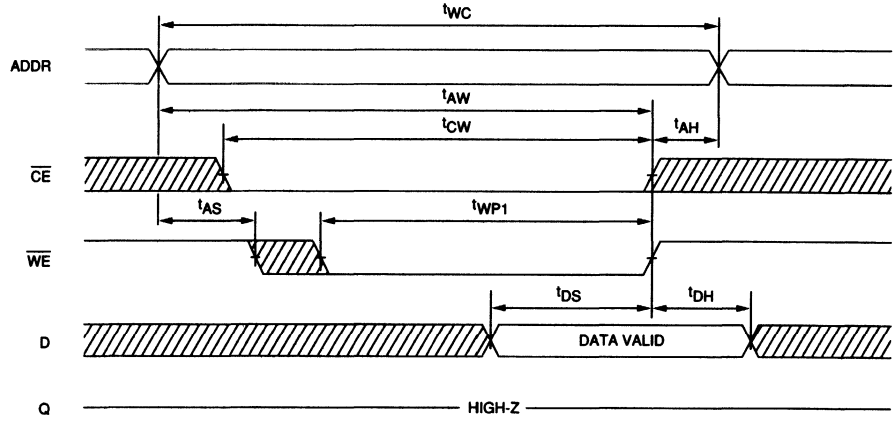
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

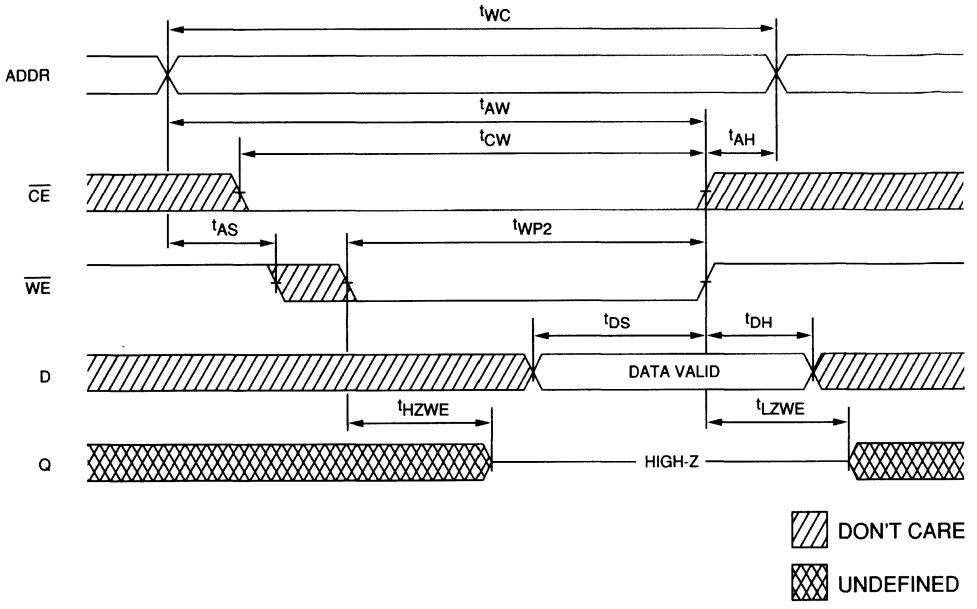


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

8K x 8 SRAM

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS — MARKING

- Timing

8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention — L
- Temperature

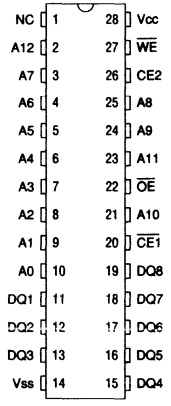
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C6408DJ-10 L AT

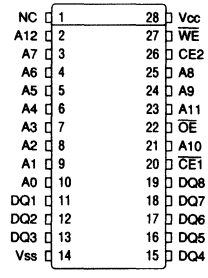
*Preliminary

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

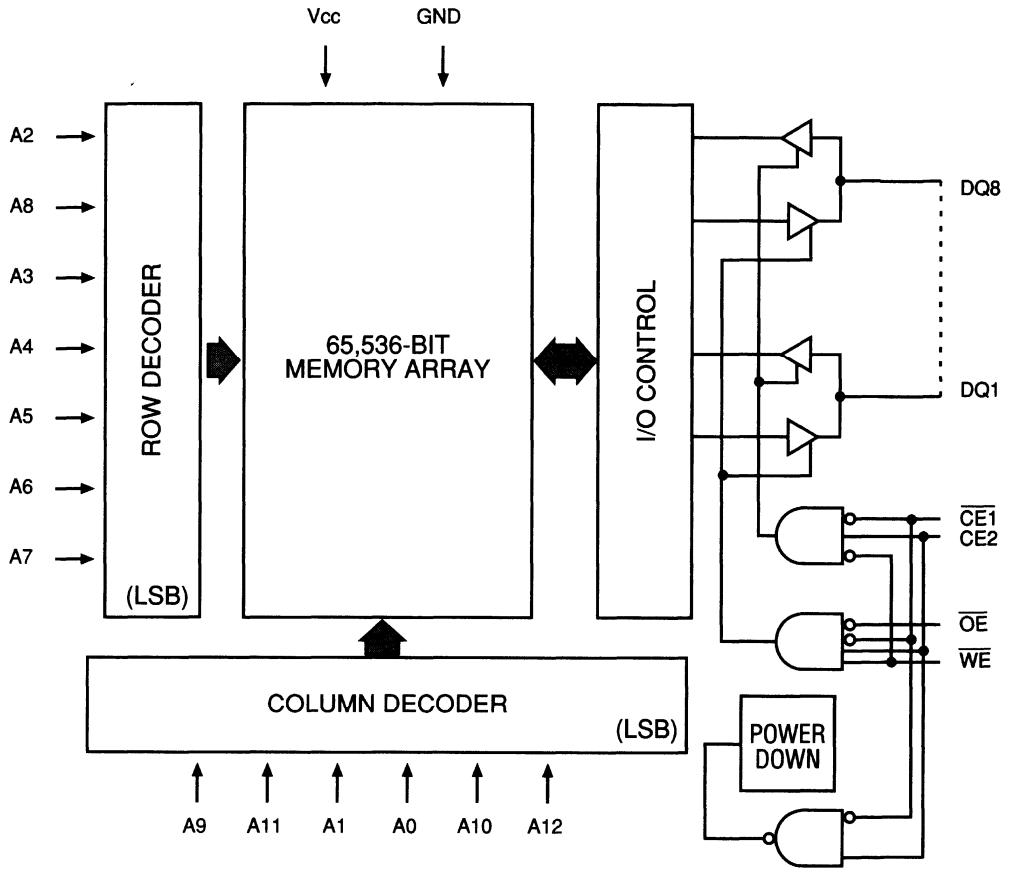
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers two chip enables and an output enable on the x8 organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	DQ	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
READ	L	H	H	H	HIGH-Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8+	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	60	50	45	40	35	35	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	5	mA	14

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	tRC	8		10		12		15		20		25		ns	
Address access time	tAA		8		10		12		15		20		25	ns	
Chip Enable access time	tACE		7		8		10		12		15		20	ns	
Output hold from address change	tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE†	2		2		2		2		2		2		ns	7, 16
Chip disable to output in High-Z	tHZCE		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		8		10		12		15		20		25	ns	
Output Enable access time	tAOE		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		4.5		5		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	tWC	8		10		12		15		20		25		ns	
Chip Enable to end of write	tCW	6.5		8		10		12		15		20		ns	
Address valid to end of write	tAW	6.5		8		10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
WRITE pulse width	tWP1	5.5		7		8		10		12		15		ns	
WRITE pulse width	tWP2	8		9		10		14		18		20		ns	
Data setup time	tDS	4.5		6		7		8		9		10		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	tHZWE		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 16 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

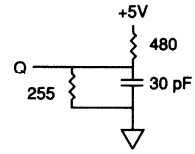


Fig. 1 OUTPUT LOAD EQUIVALENT

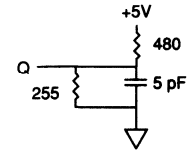


Fig. 2 OUTPUT LOAD EQUIVALENT

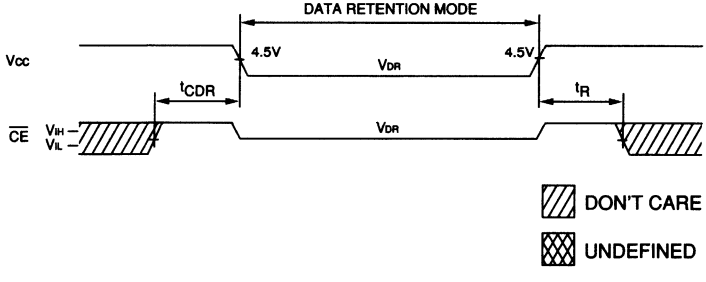
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 Timing is the same as $\overline{CE1}$ timing. The wave is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
15. Typical values are measured at 5V, 25°C and 20ns cycle time.
16. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

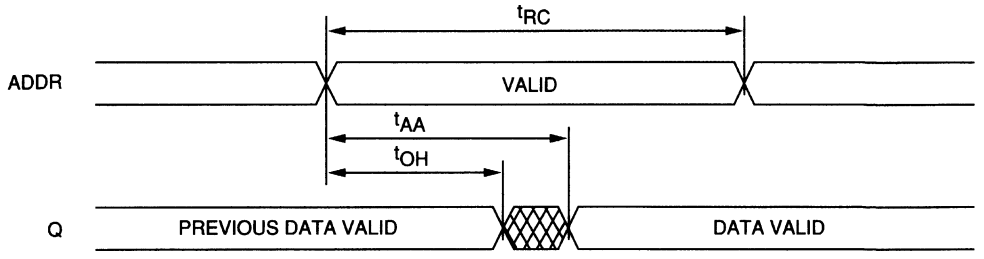
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

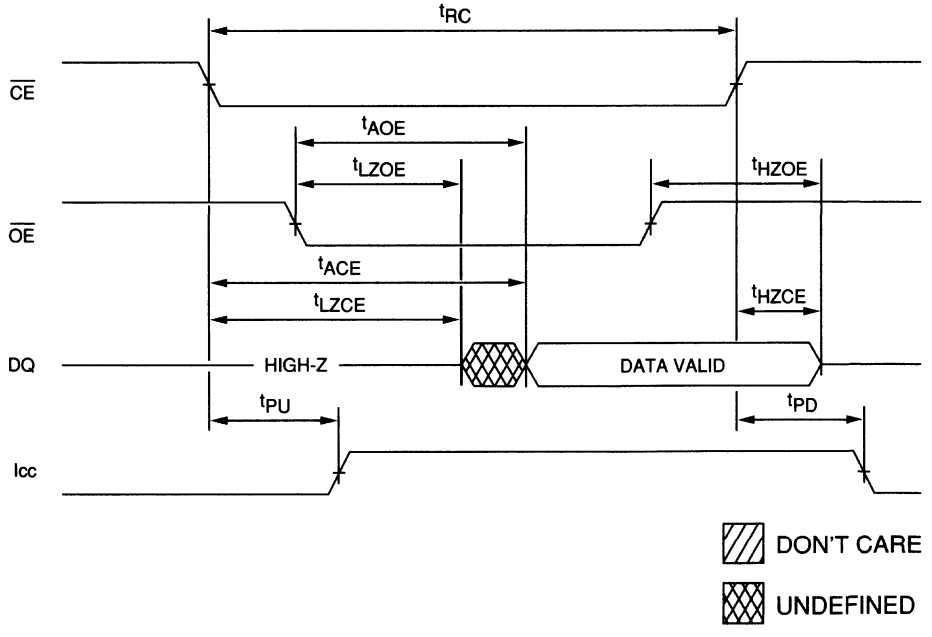
LOW Vcc DATA RETENTION WAVEFORM



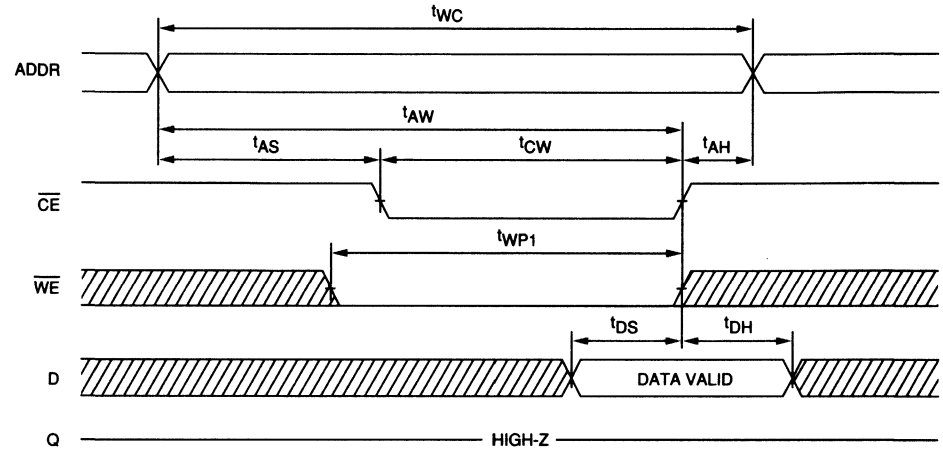
READ CYCLE NO. 1 [8, 9]



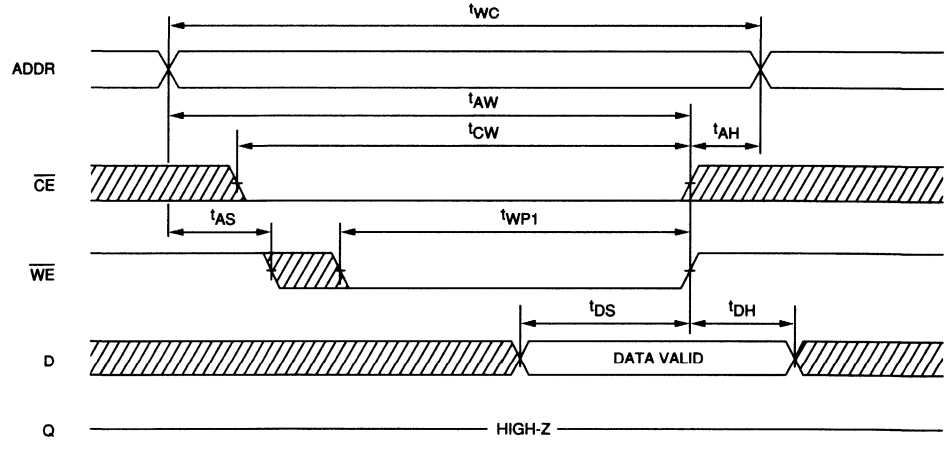
READ CYCLE NO. 2 [7, 8, 10, 12]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)

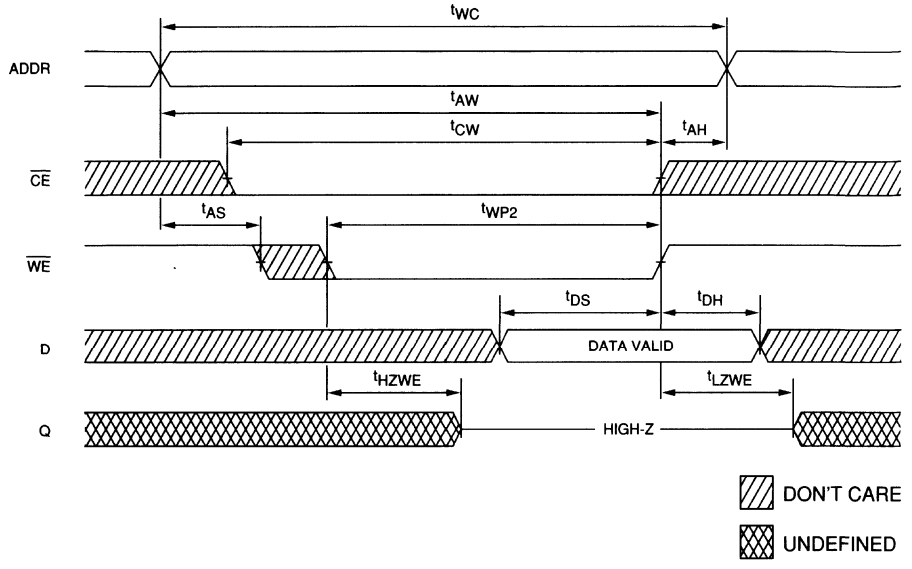


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

32K x 8 SRAM

FEATURES

- High speed: 10*, 12*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
10ns access	-10*
12ns access	-12*
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP	Z

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

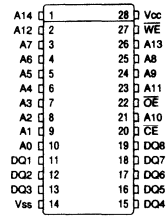
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C2568Z-20 LP IT

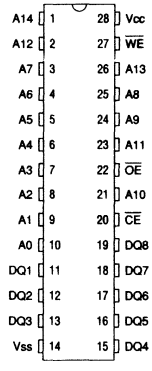
*Preliminary

PIN ASSIGNMENT (Top View)

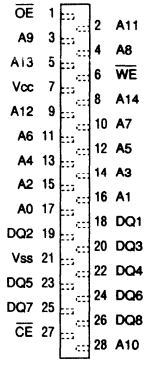
28-Pin SOJ (SD-2)



28-Pin DIP (SA-4)



28-Pin ZIP (SB-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

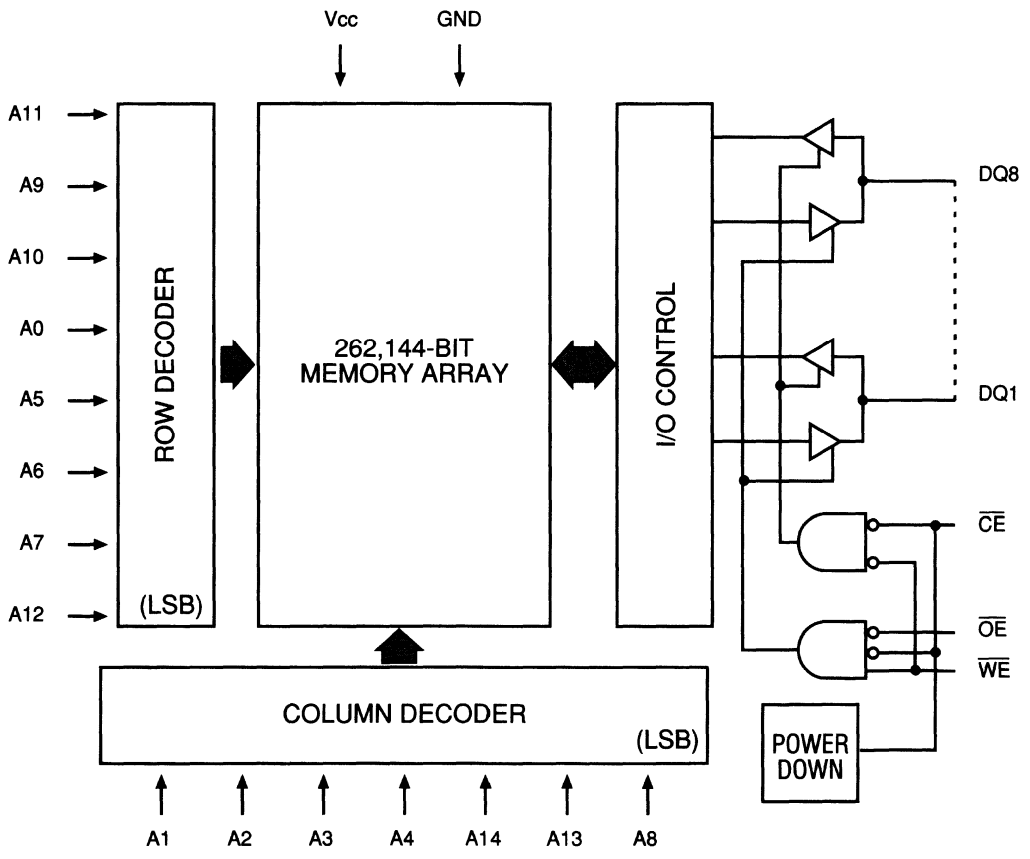
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10*†	-12*†	-15†	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	85	180	160	140	120	110	90	mA	3, 14
	"LP" VERSION	I_{CC}	65	-	-	-	110	100	80	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	11	45	40	30	30	25	25	mA	14
	"LP" VERSION	I_{SB1}	3	-	-	-	7	7	7	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	14

*Preliminary
† LP version not available in this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

5 VOLT SRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10*		-12*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	tRC	10		12		15		20		25		35		ns	
Address access time	tAA		10		12		15		20		25		35	ns	
Chip Enable access time	tACE		10		12		15		20		25		35	ns	
Output hold from address change	tOH	2		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	3		4		4		4		6		6		ns	7
Chip disable to output in High-Z	tHZCE		6		8		8		9		9		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		10		12		15		20		25		35	ns	
Output Enable access time	tAOE		6		8		8		8		8		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	tHZOE		5		6		6		7		7		12	ns	6
WRITE Cycle															
WRITE cycle time	tWC	10		12		15		20		25		30		ns	
Chip Enable to end of write	tCW	9		10		10		15		15		20		ns	
Address valid to end of write	tAW	9		10		10		15		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
WRITE pulse width	tWP1	9		10		10		15		15		20		ns	
WRITE pulse width	tWP2	11		12		12		15		15		20		ns	
Data setup time	tDS	6		7		7		10		10		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		4		4		4		5		5		ns	7
Write Enable to output in High-Z	tHZWE		6		7		7		10		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

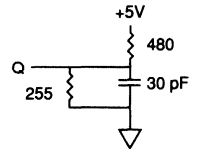


Fig. 1 OUTPUT LOAD EQUIVALENT

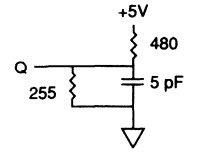


Fig. 2 OUTPUT LOAD EQUIVALENT

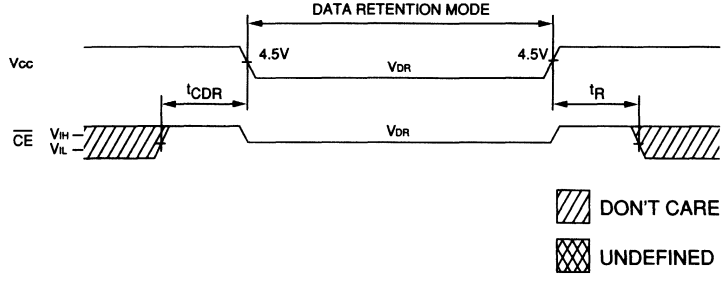
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

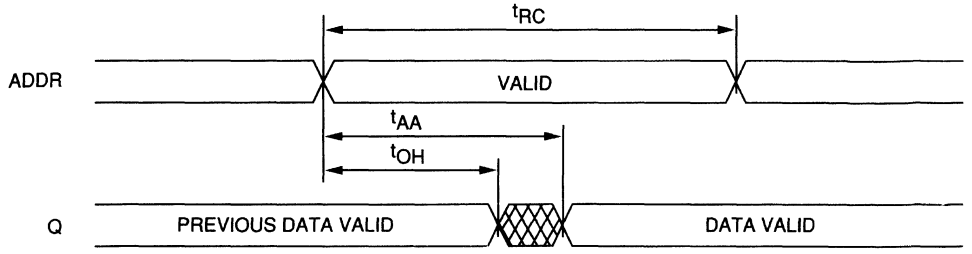
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	300	µA	
		Vcc = 3V	I_{CCDR}		90	500	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

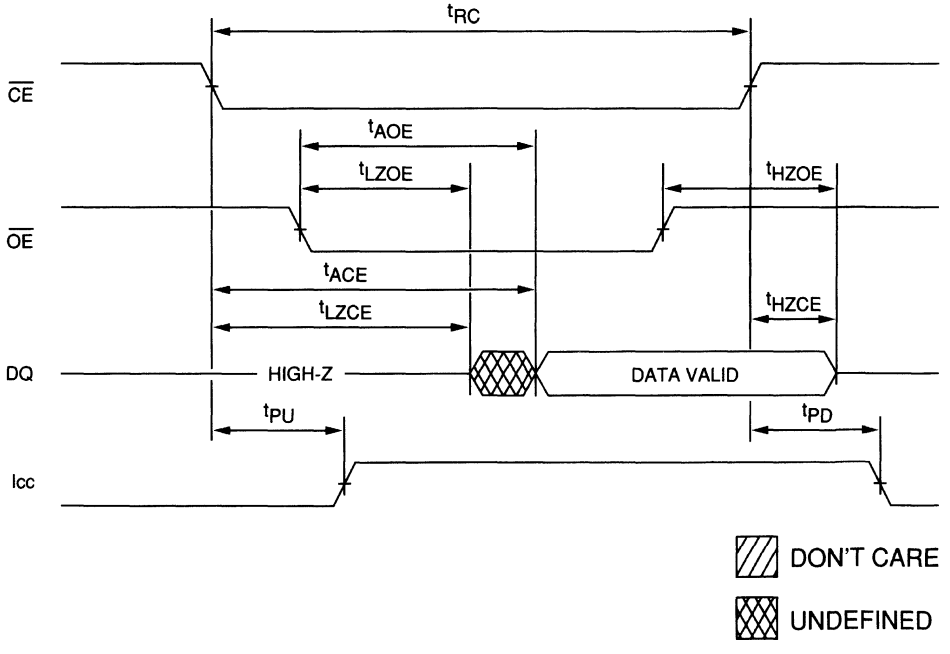
LOW Vcc DATA RETENTION WAVEFORM



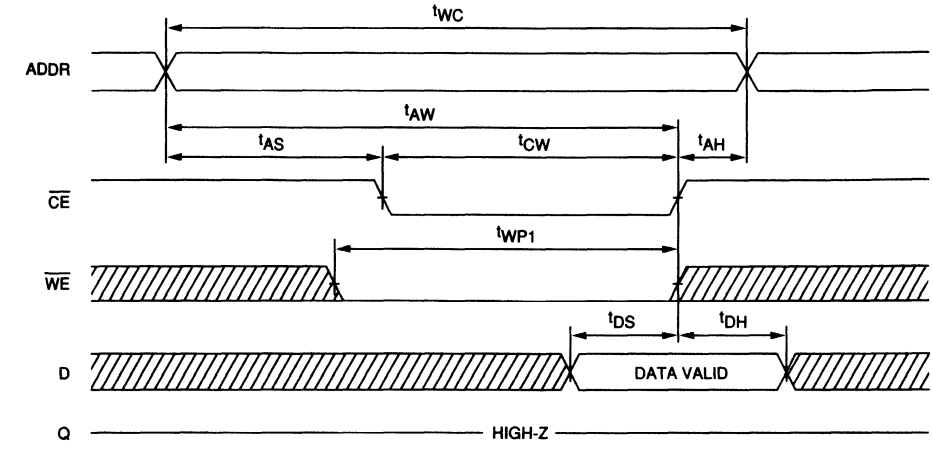
READ CYCLE NO. 1 [8, 9]



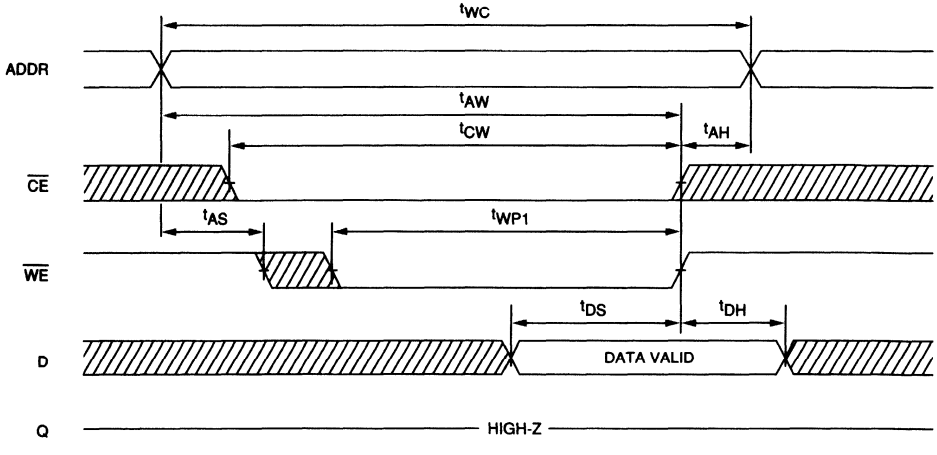
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

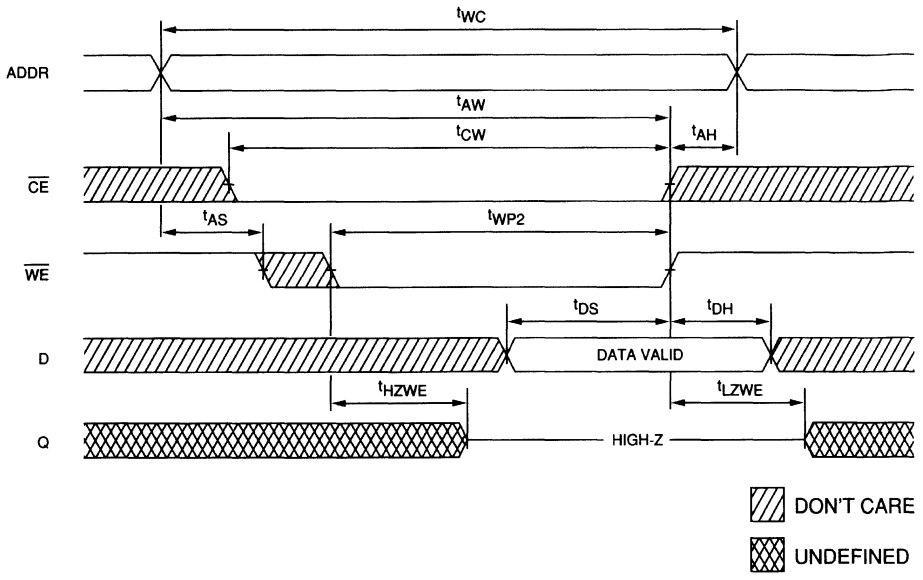


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12*, 15*, 17, 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS — MARKING

- Timing

12ns access	-12*
15ns access	-15*
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45

- Packages

Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention — L
- 2V data retention, low power — LP

- Temperature

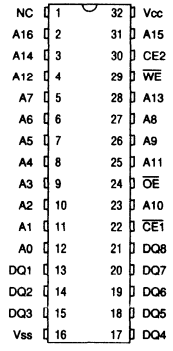
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C1008DJ-25 LP IT

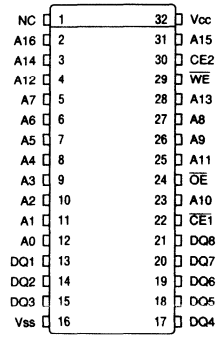
*Preliminary

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SA-7, SA-8)



32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

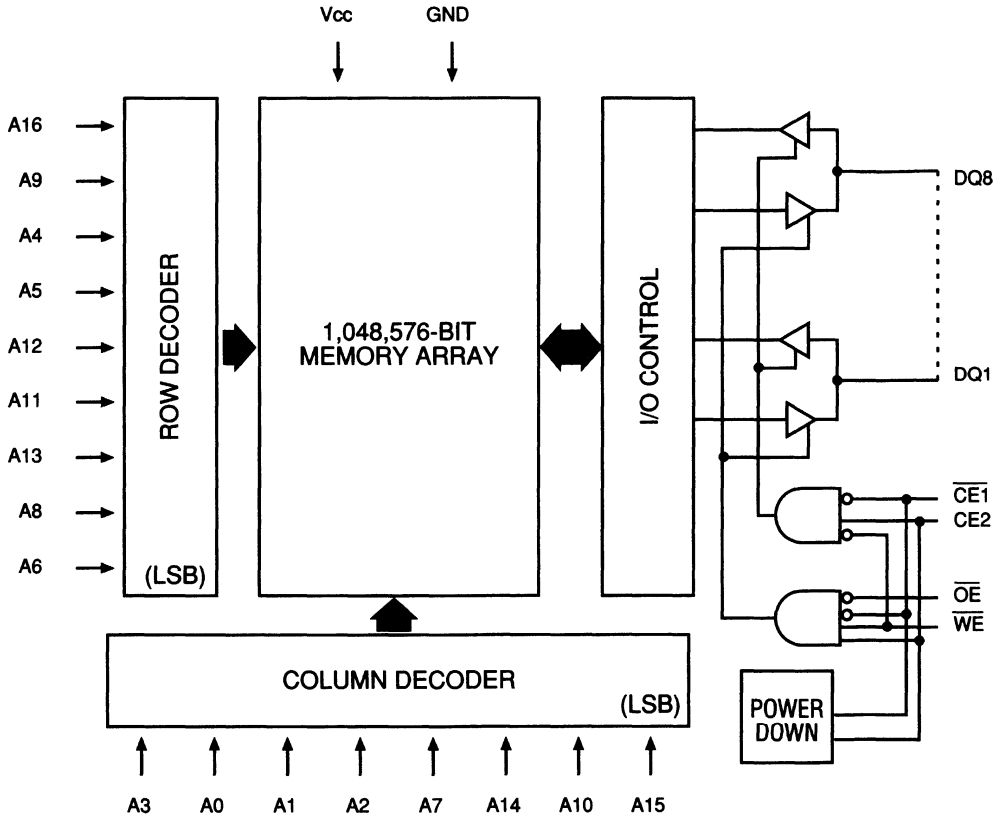
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and an output enable ($\overline{OE}$). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers reduced power standby modes when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70% reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12+	-15+	-17	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX; f = MAX = 1/ ^tRC; Outputs Open	I_{CC}	95	190	165	155	140	125	115	110	mA	3, 15
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX; f = MAX = 1/ ^tRC; Outputs Open	I_{SB1}	17	45	40	40	35	30	25	25	mA	15
	"LP" Version Only	I_{SB1}	1.3	3	3	3	3	3	3	3	mA	15
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX; $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	5	5	5	mA	15
	"L" and "LP" Versions Only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	15

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12*		-15*		-17		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^tRC	12		15		17		20		25		35		45		ns	
Address access time	^tAA		12		15		17		20		25		35		45	ns	
Chip Enable access time	^tACE		12		15		17		20		25		35		45	ns	
Output hold from address change	^tOH	3		3		3		3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		7		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		17		20		25		35		45	ns	
Output Enable access time	^tAOE		4		5		5		6		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		5		5		6		10		12		15	ns	6
WRITE Cycle																	
WRITE cycle time	^tWC	12		15		17		20		25		35		45		ns	
Chip Enable to end of write	^tCW	8		10		12		12		15		20		25		ns	
Address valid to end of write	^tAW	8		10		12		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		12		15		20		25		ns	
WRITE pulse width	$^tWP2$	10		12		13		15		15		20		25		ns	
Data setup time	^tDS	6		7		8		8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		15		18	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

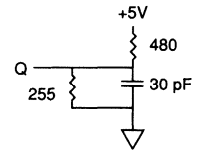


Fig. 1 OUTPUT LOAD EQUIVALENT

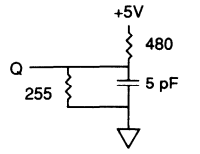


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

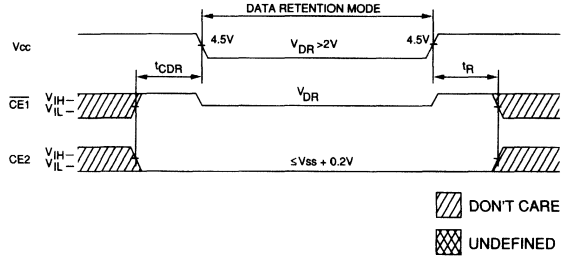
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave form is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
15. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

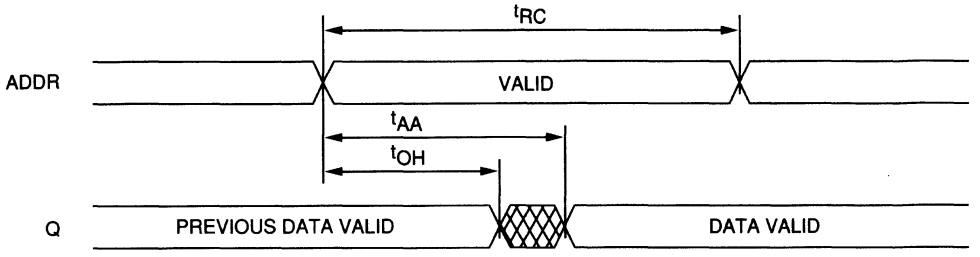
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	150	µA	
		Vcc = 3V			60	250	µA	
		Vcc = 3V*			30	100	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

*Preliminary

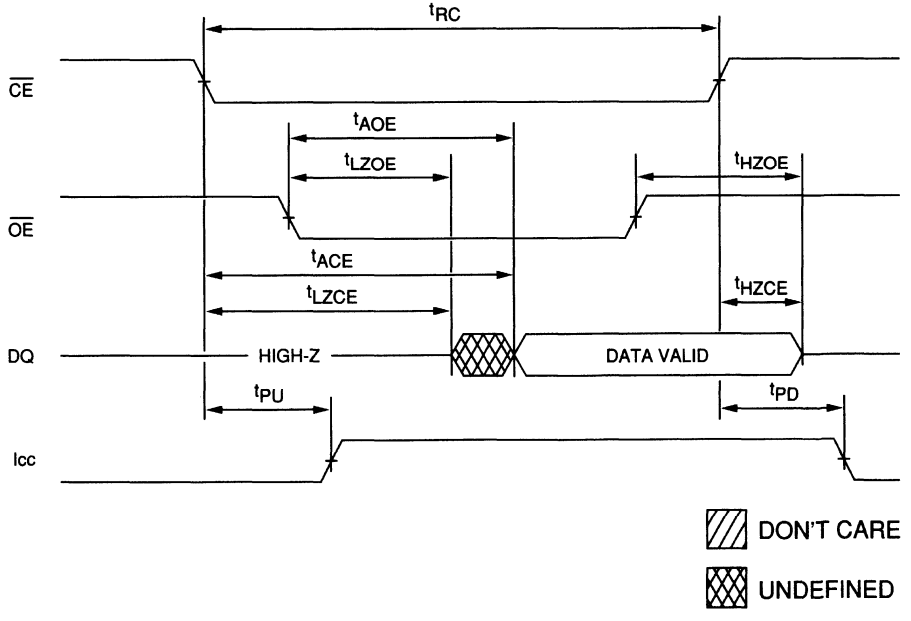
LOW Vcc DATA RETENTION WAVEFORM



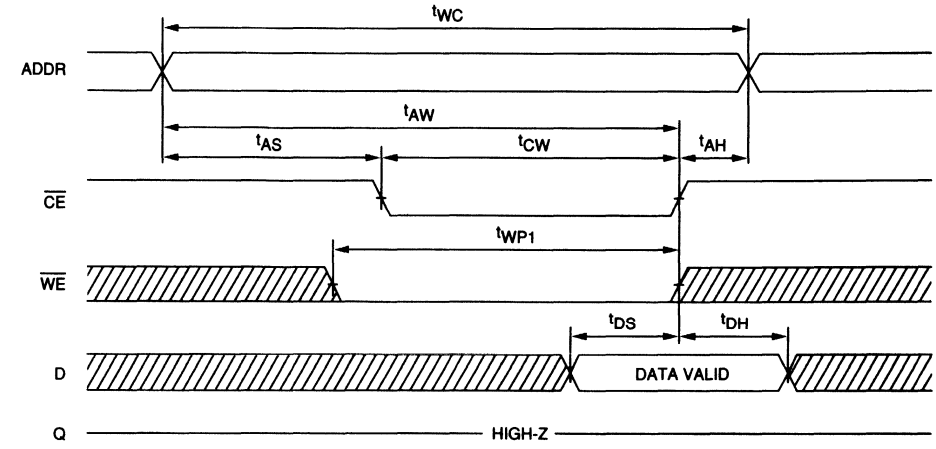
READ CYCLE NO. 1 [8, 9]



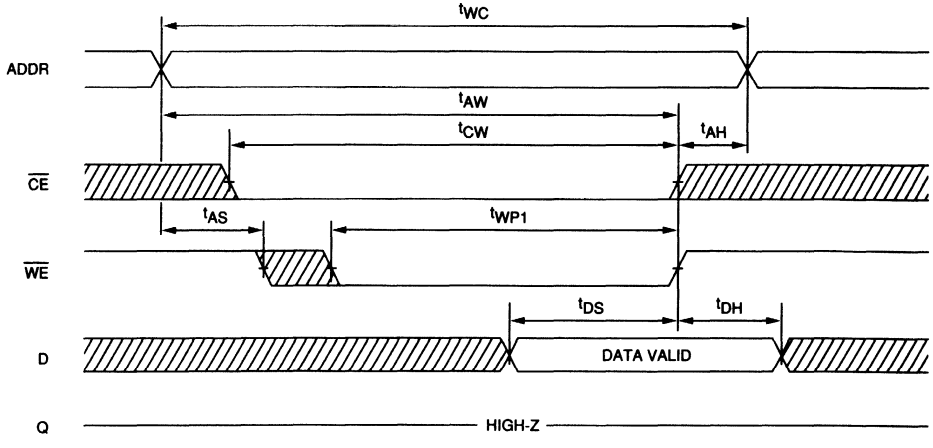
READ CYCLE NO. 2 [7, 8, 10, 12]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)

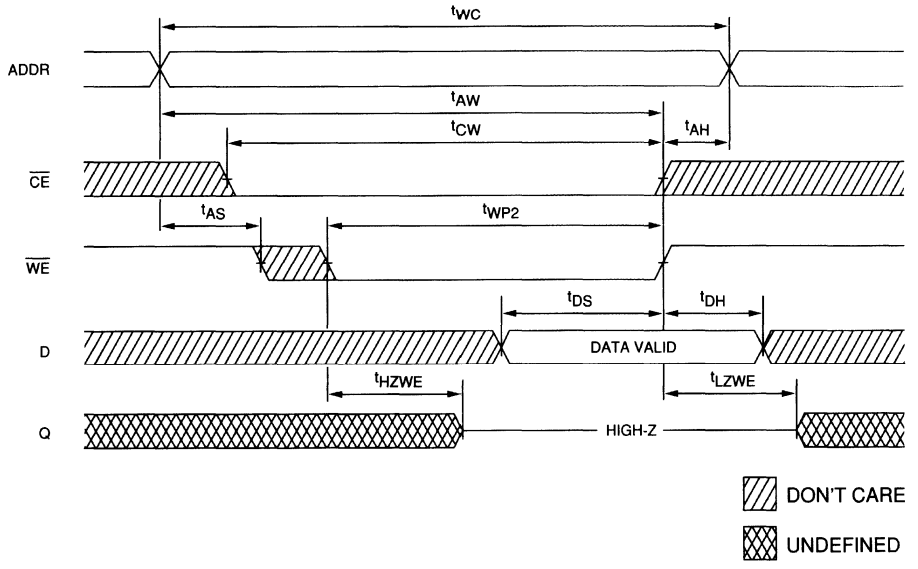


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON

MT5C128K8A1
REVOLUTIONARY PINOUT 128K x 8 SRAM

NEW ■ 5 VOLT SRAM

SRAM

128K x 8 SRAM

WITH SINGLE CHIP ENABLE,
CENTER POWER AND GROUND PINS

FEATURES

- High speed: 12, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast $\overline{OE}$ access times: 6, 8, 10 and 12ns

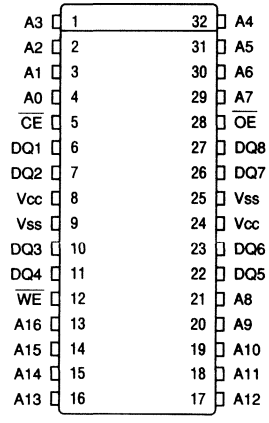
OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
32-pin SOJ (400 mil)	DJ

- Part Number Example: MT5C128K8A1TG-25

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

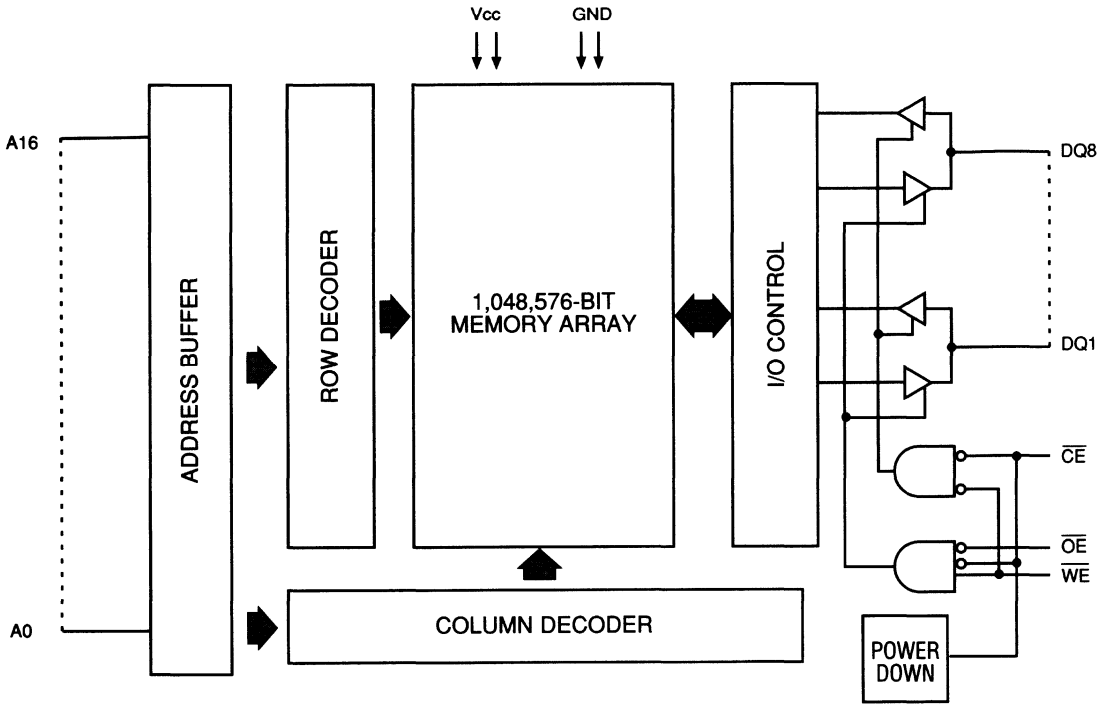
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the ouputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
4, 3, 2, 1, 32, 31, 30, 29, 21, 20, 19, 18, 17, 16, 15, 14, 13	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
12	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
5	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
28	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
6, 7, 10, 11, 22, 23, 26, 27	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	V_{CC}	Supply	Power Supply: 5V ±10%
9, 25	V_{SS}	Supply	Ground: GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.7W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	150	300	260	220	200	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	25	50	45	40	35	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	7		9		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	7		9		10		12		ns	
WRITE pulse width	$^tWP2$	7		9		10		12		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

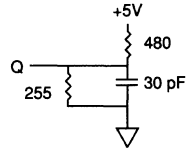


Fig. 1 OUTPUT LOAD EQUIVALENT

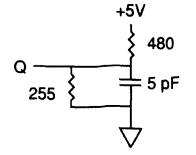
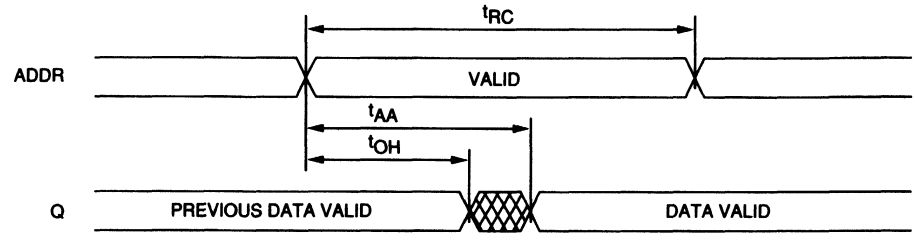


Fig. 2 OUTPUT LOAD EQUIVALENT

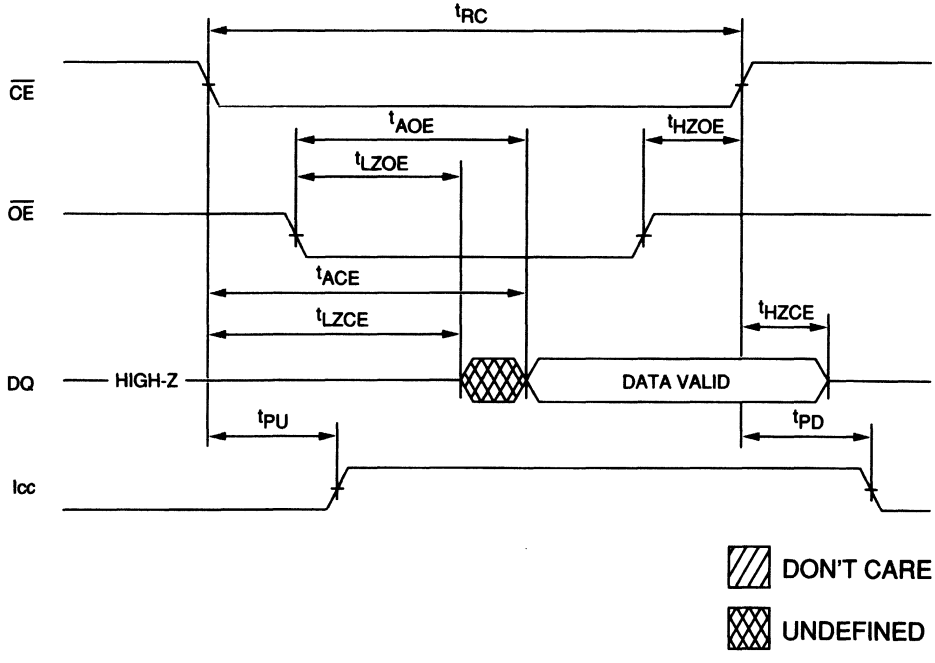
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}HZCE$, $^{t}HZOE$ and $^{t}HZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, and $^{t}HZWE$ is less than $^{t}LZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.

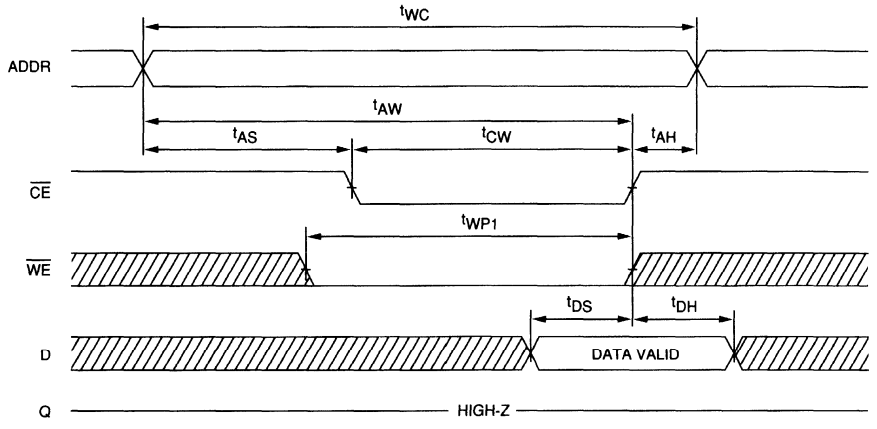
READ CYCLE NO. 1 [8, 9]



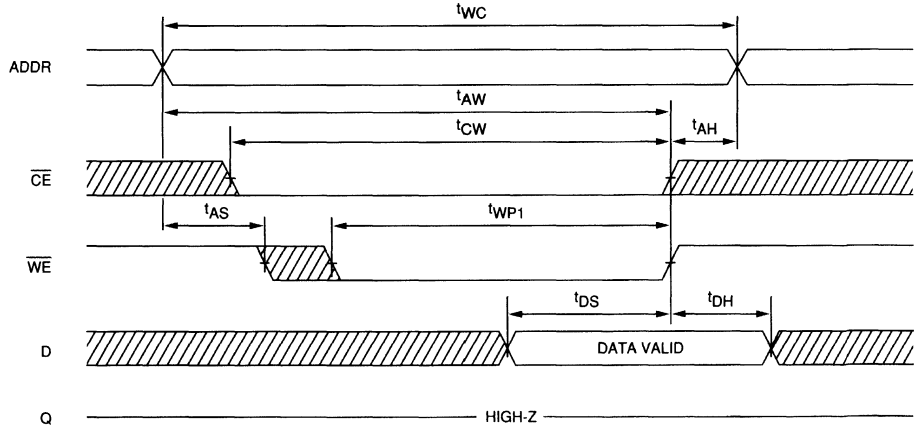
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

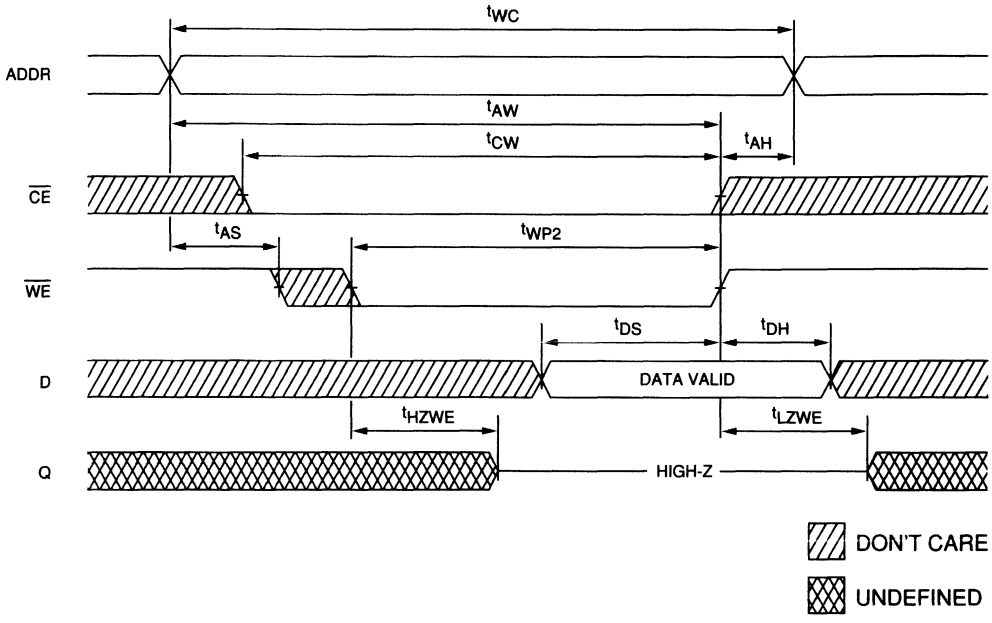


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON

MT5C128K8A1
REVOLUTIONARY PINOUT 128K x 8 SRAM

NEW ■ 5 VOLT SRAM

SRAM

512K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, 35 and 55ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS — MARKING

- Timing

20ns access	-20
25ns access	-25
35ns access	-35
55ns access	-55

- Packages

Plastic SOJ (400 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book.*

- 2V data retention — L

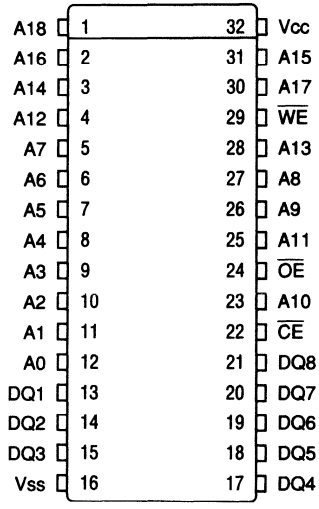
- Temperature

Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C512K8A1DJ-25 L IT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

NEW ■ 5 VOLT SRAM

SRAM

512K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 6ns

OPTIONS MARKING

- Timing

20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention L
- 2V data retention, low power LP

- Part Number Example: MT5C512K8B2DJ-20 LP

GENERAL DESCRIPTION

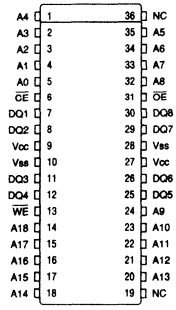
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and ouput enable ($\overline{OE}$) capabilities. This enhancement can place the outputs in High-Z for additional flexibility in system design.

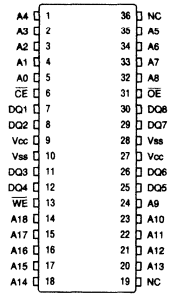
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

PIN ASSIGNMENT (Top View)

36-Pin SOJ
(SD-6)



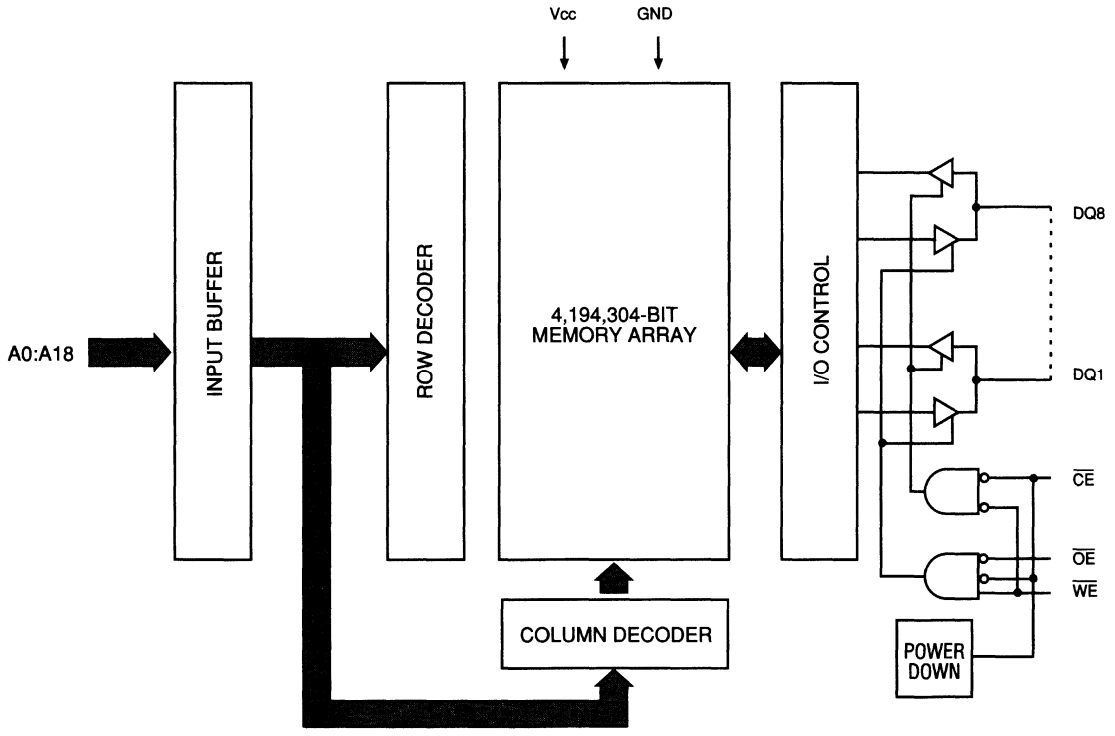
36-Pin TSOP
(SE-2)



The "LP" version provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-2	2	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-2	2	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	140	120	115	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	35	30	25	mA	
	"LP" Version Only	I_{SB1}	2	2	2	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	2	2	2	mA	
	"L" and "LP" Versions Only	I_{SB2}	2	2	2	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		35		ns	
Address access time	^tAA		20		25		35	ns	
Chip Enable access time	^tACE		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		10		12	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		25		35		ns	
Chip Enable to end of write	^tCW	12		15		20		ns	
Address valid to end of write	^tAW	12		15		20		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		ns	
WRITE pulse width	$^tWP2$	15		15		20		ns	
Data setup time	^tDS	8		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

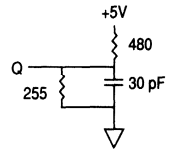


Fig. 1 OUTPUT LOAD EQUIVALENT

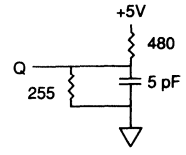


Fig. 2 OUTPUT LOAD EQUIVALENT

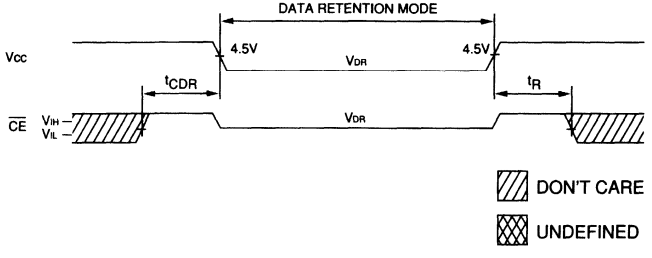
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.

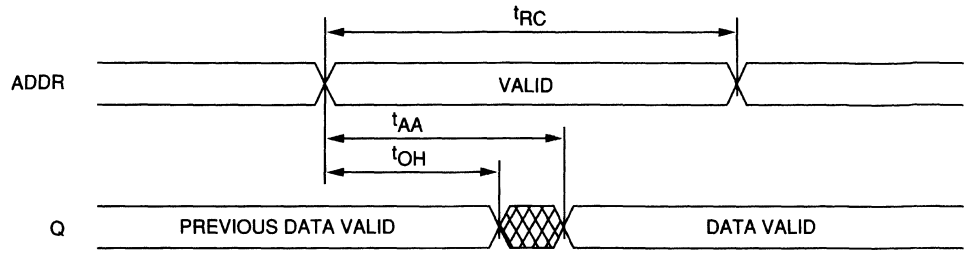
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		200	µA	
		Vcc = 3V			300	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		ns	4
Operation Recovery Time			^{t}R	^{t}RC		ns	4, 11

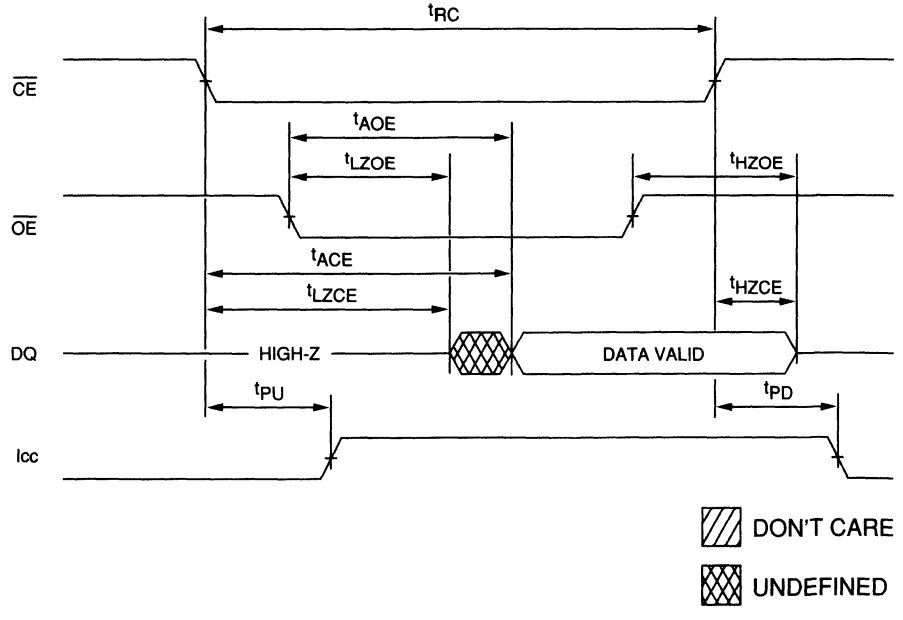
LOW Vcc DATA RETENTION WAVEFORM



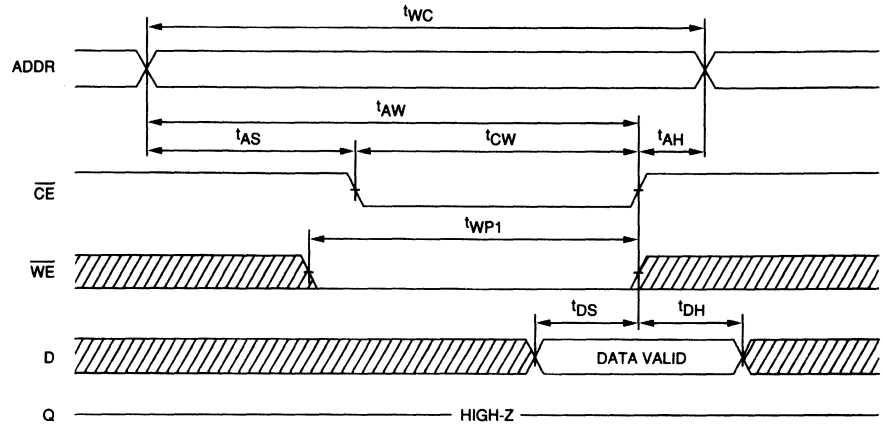
READ CYCLE NO. 1 [8, 9]



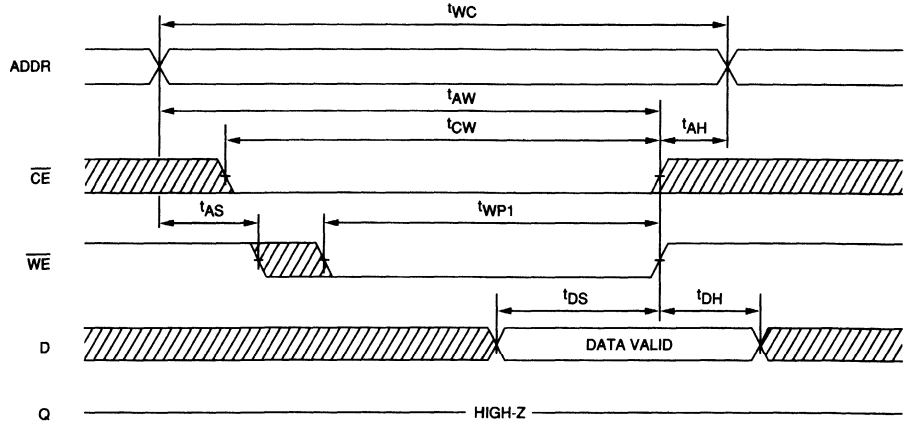
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

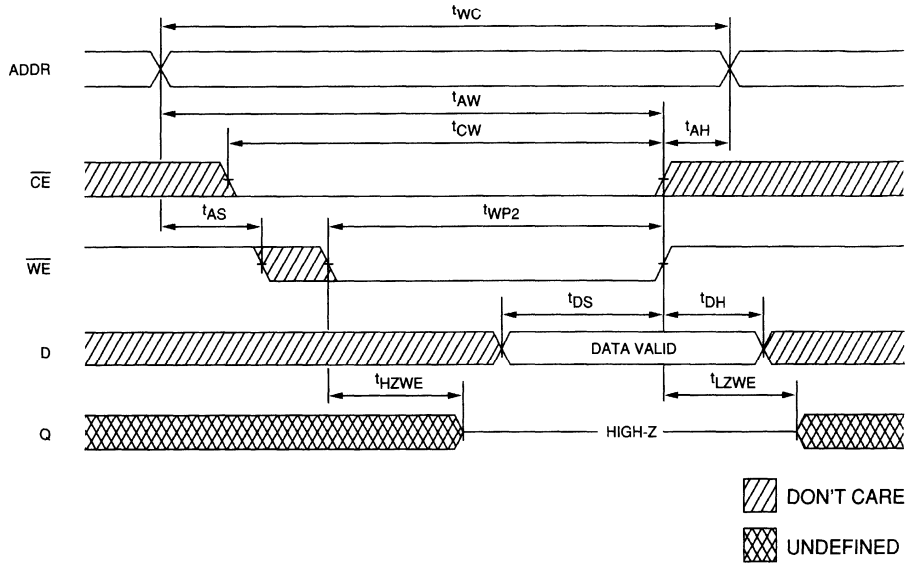


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

32K x 9 SRAM

FEATURES

- High speed: 15, 17, 20 and 25ns
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

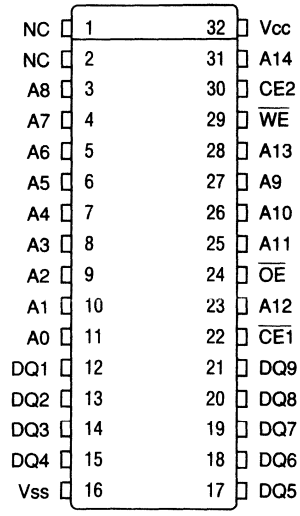
OPTIONS

MARKING

- Timing
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic SOJ (300 mil) — DJ
- 2V data retention — L
- Part Number Example: MT5C2889DJ-25 L

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-4)



GENERAL DESCRIPTION

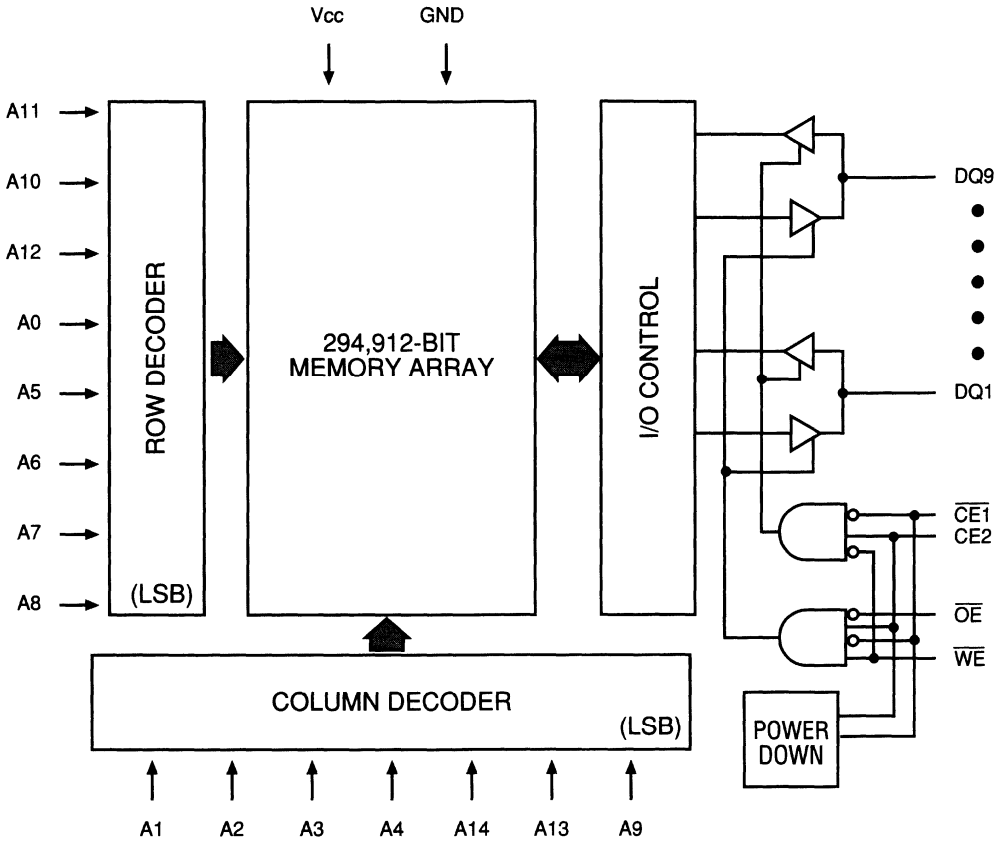
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. They are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and output enable ($\overline{OE}$) control signals. This enhancement can place the outputs in High-Z for additional flexibility in system design. The dual chip enables may be used to directly address multiple banks of SRAM without external logic.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW while CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH while $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C, V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-17	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE1}$ ≤ V_{IL}; CE2, ≥ V_{IH} f = MAX = 1/^tRC V_{CC} = MAX; Outputs Open	I_{CC}	90	145	130	120	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE1}$ ≥ V_{IH} or CE2 ≤ V_{IL} f = MAX = 1/^tRC V_{CC} = MAX; Outputs Open	I_{SB1}	13	35	35	30	30	mA	14
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.7	7	7	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	7	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ±10%)

DESCRIPTION		-15		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	15		17		20		25		ns	
Address access time	^tAA		15		17		20		25	ns	
Chip Enable access time	^tACE		15		17		20		25	ns	
Output hold from address change	^tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		4		4		4		ns	7
Chip disable to output in High-Z	^tHZCE		8		8		8		8	ns	6, 7
Chip Enable to power up time	^tPU	0		0		0		0		ns	
Chip disable to power down time	^tPD		15		17		20		25	ns	
Output Enable access time	^tAOE		8		8		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to out put in High-Z	^tHZOE		7		7		7		7	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		17		20		25		ns	
Chip Enable to end of write	^tCW	10		13		15		20		ns	
Address valid to end of write	^tAW	10		13		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	10		13		15		20		ns	
WRITE pulse width	$^tWP2$	12		13		15		20		ns	
Data setup time	^tDS	7		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		4		4		4		ns	7
Write Enable to output in High-Z	^tHZWE		7		8		10		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

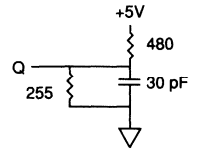


Fig. 1 OUTPUT LOAD EQUIVALENT

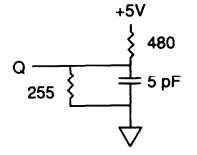


Fig. 2 OUTPUT LOAD EQUIVALENT

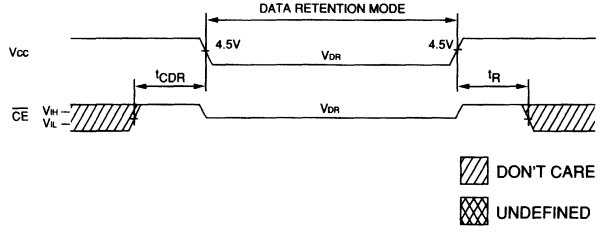
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is identical to $\overline{CE1}$ timing. The waveform is inverted.
13. Either $\overline{CE1}$, CE2 or $\overline{WE}$ can initiate or terminate WRITE cycles.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

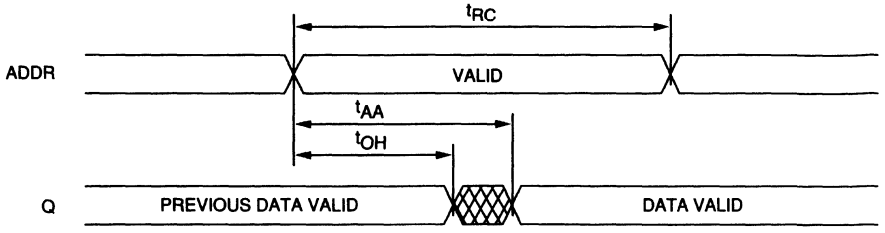
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		40	400	µA	
		Vcc = 3V			100	600	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

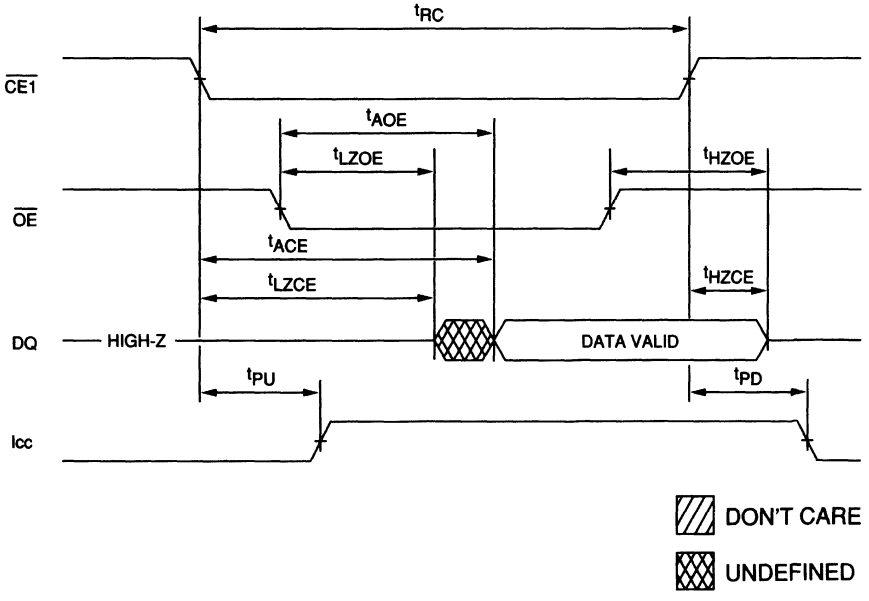
LOW Vcc DATA RETENTION WAVEFORM



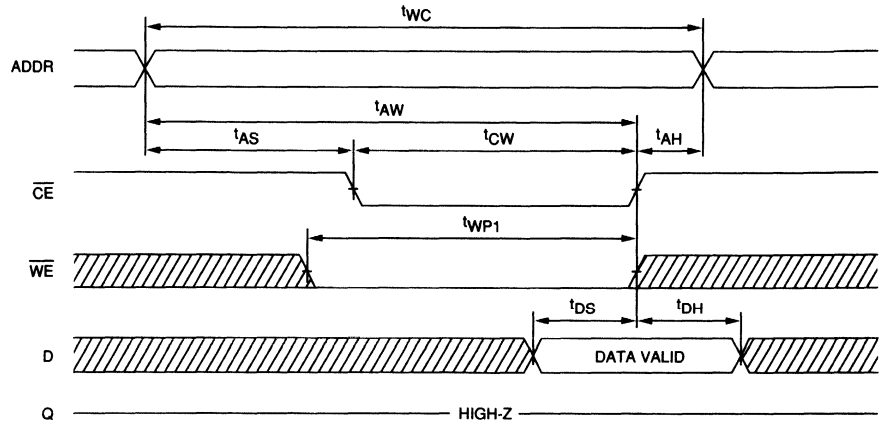
READ CYCLE NO. 1 [8, 9]



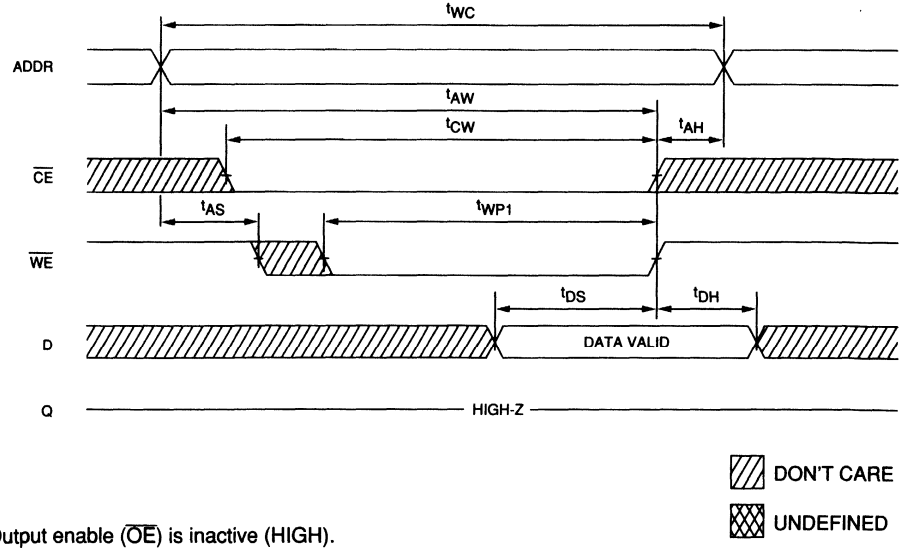
READ CYCLE NO. 2 [7, 8, 10, 12]



WRITE CYCLE NO. 1 [12, 13]
(Chip Enable Controlled)

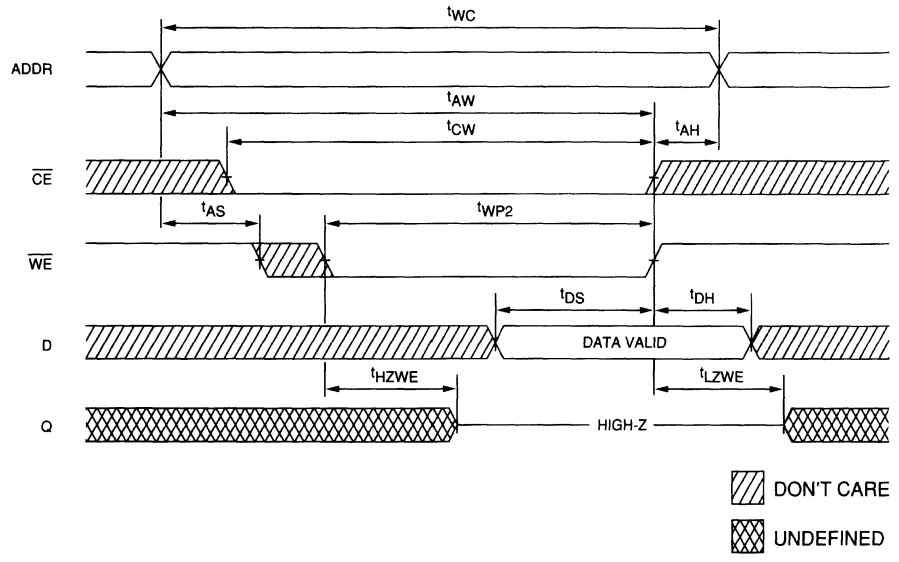


WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 9 SRAM

WITH SINGLE CHIP ENABLE

FEATURES

- High speed: 15*, 17, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL compatible
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Fast $\overline{OE}$ access time: 6ns

OPTIONS

	MARKING
• Timing	
15ns access	-15*
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic SOJ (400 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

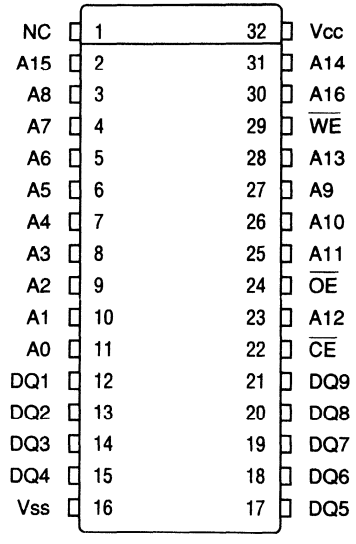
NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- Part Number Example: MT5C1189DJ-20 L IT

*Preliminary

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

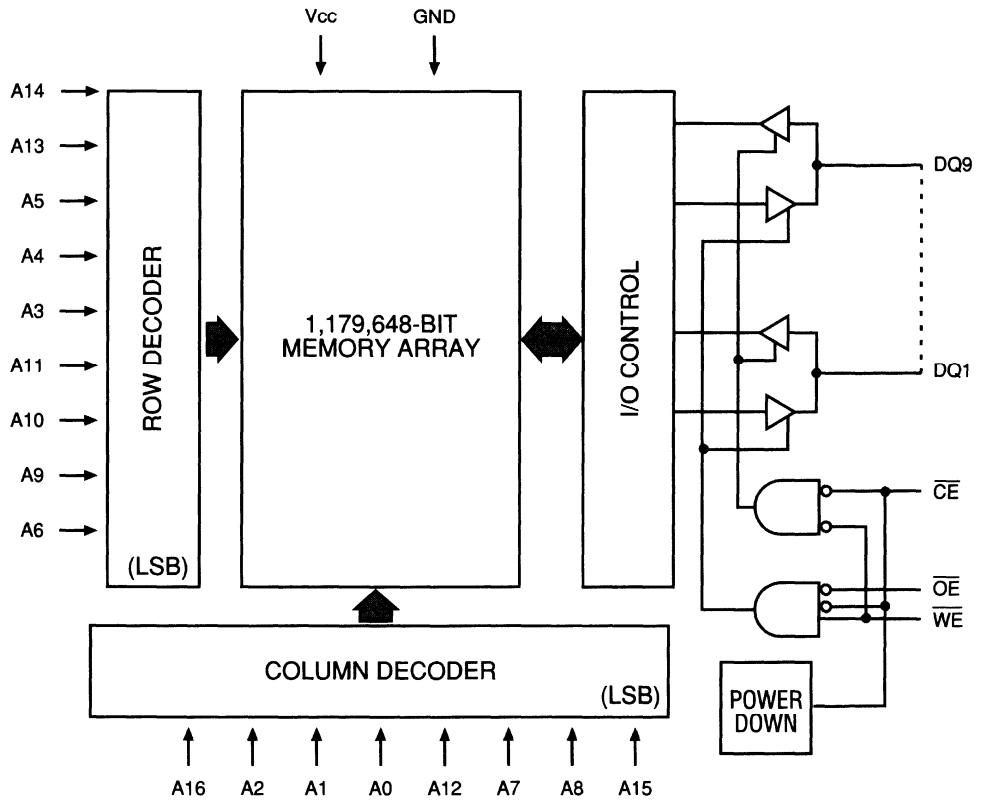
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capabilities. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to Vss ..... -1V to V_{CC}+1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15+	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	95	175	165	150	125	115	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	17	40	40	35	30	25	mA	14
	$\overline{CE}$ ≥ (Vcc -0.2V); Vcc = MAX All Other Inputs ≤ 0.2V or ≥ (Vcc -0.2V); f = 0Hz	I_{SB2}	0.4	5	5	5	5	5	mA	14
"L" version only	$\overline{CE}$ ≥ (Vcc -0.2V); Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0Hz	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	mA	

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15*		-17		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	15		17		20		25		35		ns	
Address access time	^tAA		15		17		20		25		35	ns	
Chip Enable access time	^tACE		15		17		20		25		35	ns	
Output hold from address change	^tOH	3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25		35	ns	
Output Enable access time	^tAOE		5		5		6		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		5		6		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	15		17		20		25		35		ns	
Chip Enable to end of write	^tCW	11		12		12		15		20		ns	
Address valid to end of write	^tAW	11		12		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	11		12		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		15		20		ns	
Data setup time	^tDS	7		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		5		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

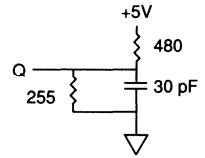


Fig. 1 OUTPUT LOAD EQUIVALENT

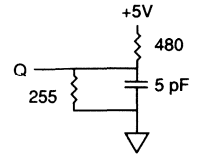


Fig. 2 OUTPUT LOAD EQUIVALENT

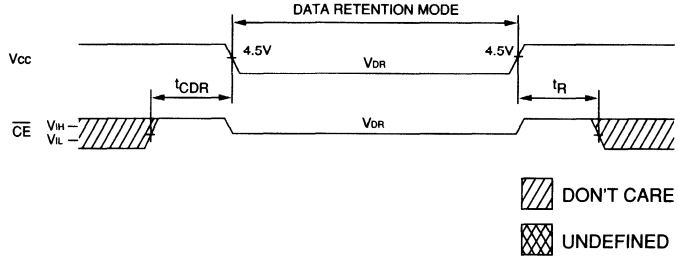
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}HZCE$, $^{t}HZOE$ and $^{t}HZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, and $^{t}HZWE$ is less than $^{t}LZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 25ns cycle time.

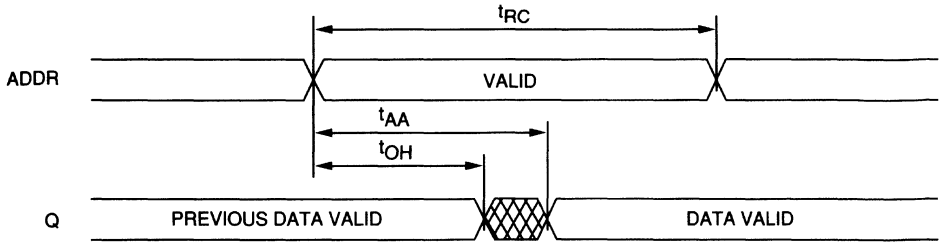
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	200	µA	
		Vcc = 3V			70	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

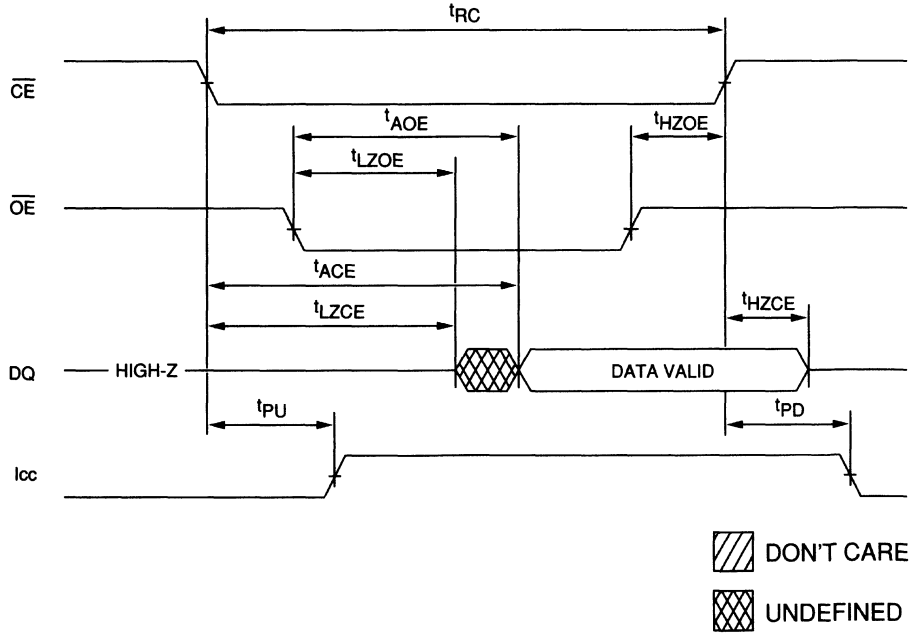
LOW Vcc DATA RETENTION WAVEFORM



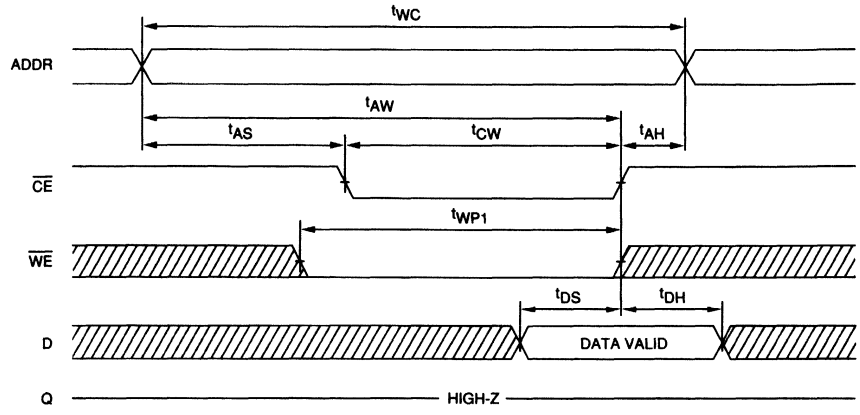
READ CYCLE NO. 1 [8, 9]



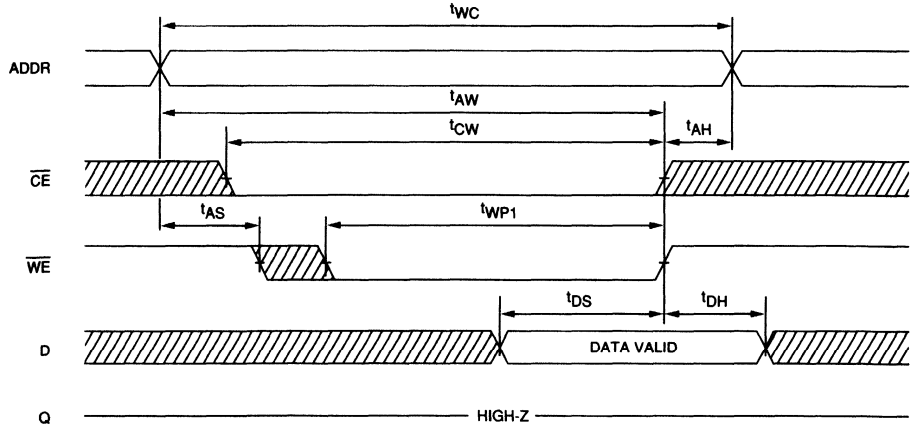
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

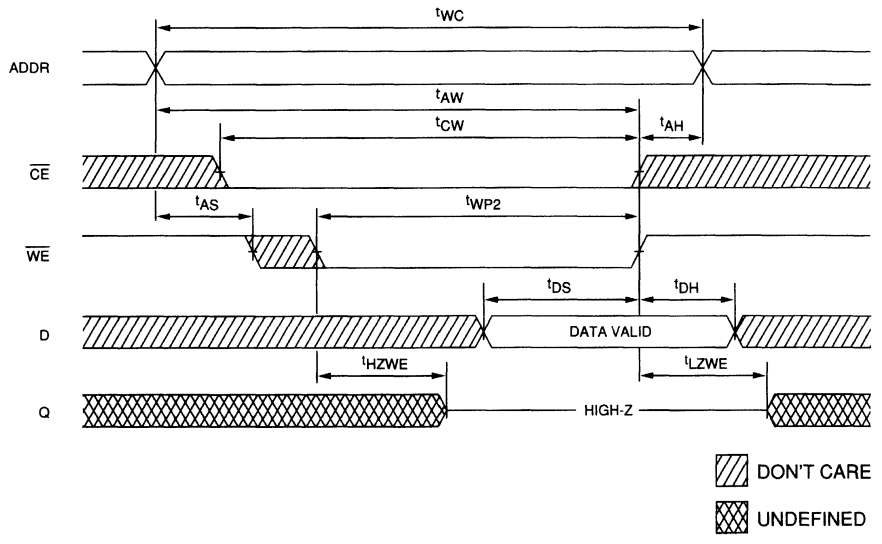


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

64K x 16 SRAM

WITH OUTPUT ENABLE

FEATURES

- Fast access times: 12, 15, 20 and 25ns
- Fast output enable access time: 6, 8, 10 and 12ns
- Multiple center power and ground pins for improved noise immunity
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Individual byte controls for both READ and WRITE cycles
- All inputs and outputs are TTL compatible

OPTIONS — MARKING

- Timing

12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

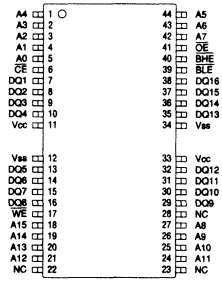
44-pin SOJ (400 mil)	DJ
44-pin TSOP (400 mil)	TG

- Part Number Example: MT5C64K16A1TG-12

PIN ASSIGNMENT (Top View)

44-Pin SOJ
(SD-7)

44-Pin TSOP
(SE-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

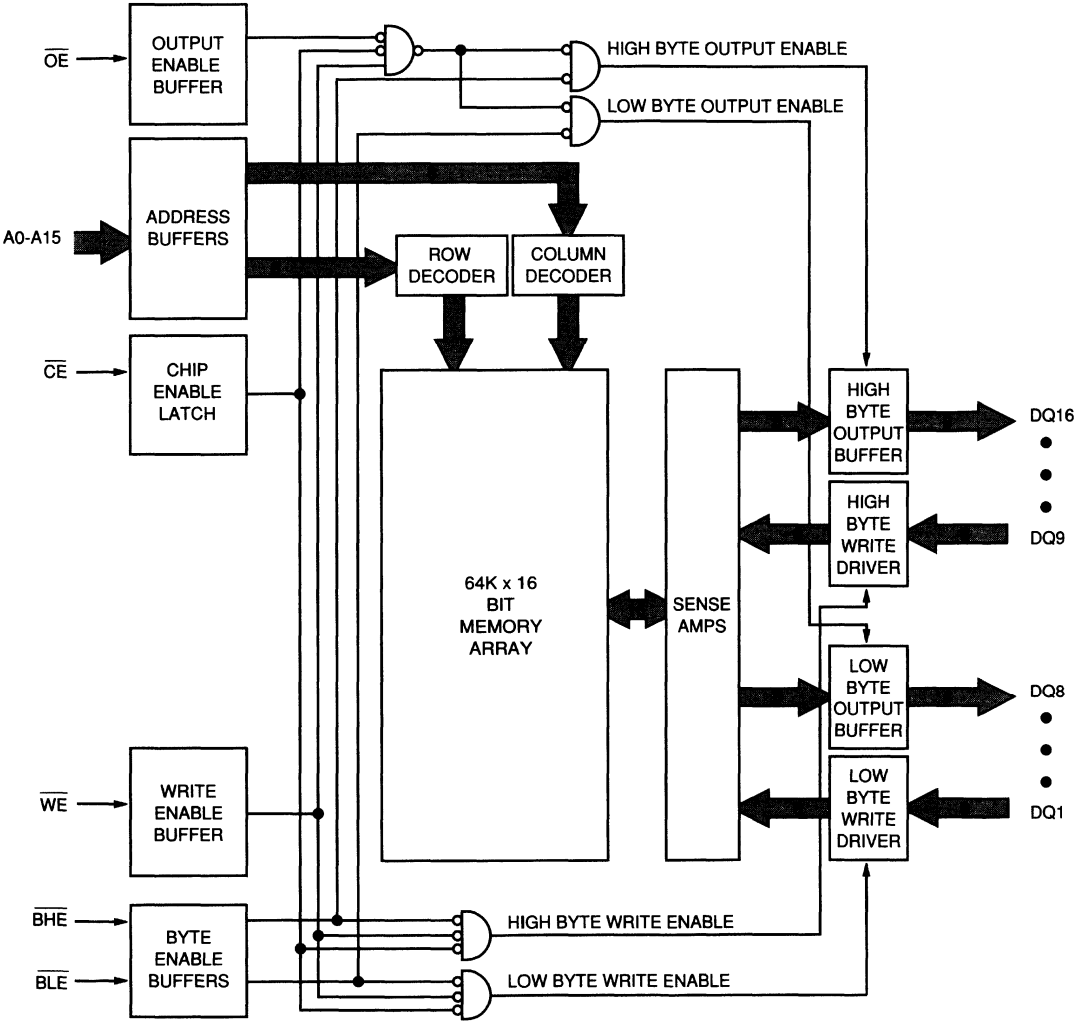
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and ouput enable ($\overline{OE}$) capabilities. This enhancement can place the output pin higher for additional flexibility in sytem design.

The MT5C64K16A1 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW chip enable, separate upper and lower byte enables and a fast output enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls DQ1-DQ8, the lower bits. $\overline{BHE}$ controls DQ9-DQ16, the upper bits.

The MT5C64K16A1 operates from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 1, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19, 18	A0-A15	Input	Address Inputs: These inputs determine which cell is accessed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte, D1-D8. When $\overline{BHE}$ is LOW, data is written or read to the upper byte, D9-D16.
6	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip automatically goes into standby power mode.
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
22, 23, 28	NC	-	No Connect: These signals are not internally connected.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16.
11, 33	Vcc	Supply	Power Supply: +5V ±10%
12, 34	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH -Z	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to 7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.7W
Short Circuit Output Current 50mA
Voltage at any pin relative toV_{SS} ..... -1V to V_{CC}+1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	150	300	260	220	200	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	25	50	45	40	35	mA	
	$\overline{CE}$ ≥ V_{CC} - 0.2V V_{CC} = MAX; V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	6, 7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6, 7
Byte Enable access time	^tABE		6		8		10		12	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		0		ns	6, 7
Byte disable to output in High-Z	^tHZBE		6		6		8		8	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	7		9		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
Write pulse width	^tWP	7		9		10		12		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		ns	6, 7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7
Byte Enable to end of write	^tBW	7		9		12		14		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

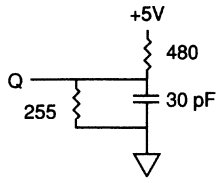


Fig. 1 OUTPUT LOAD EQUIVALENT

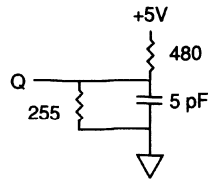
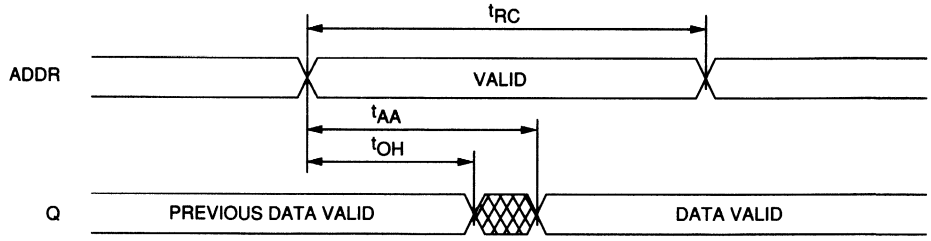


Fig. 2 OUTPUT LOAD EQUIVALENT

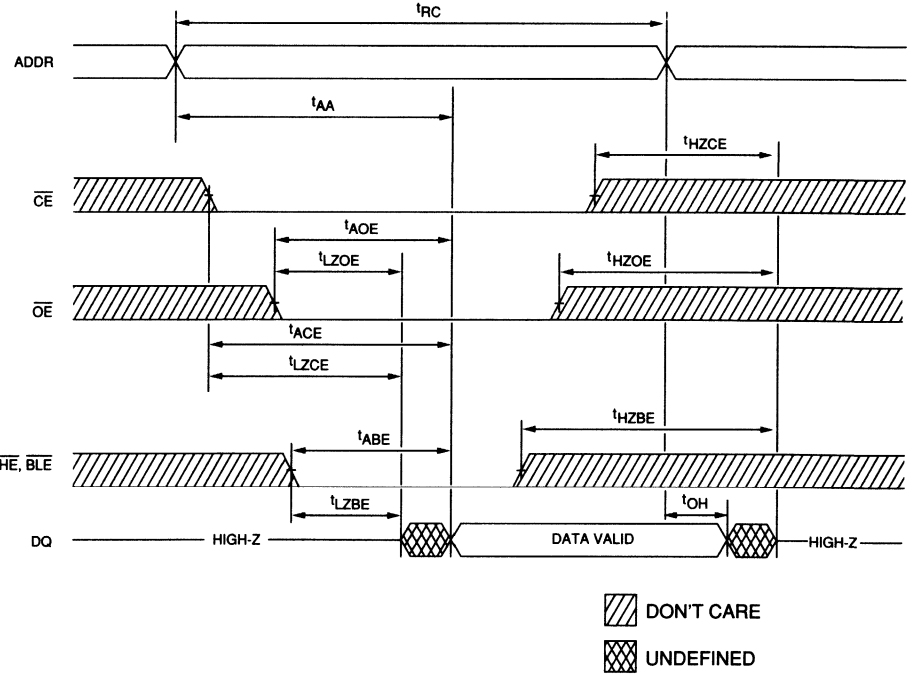
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, $^{t}HZOE$ is less than $^{t}LZOE$, and $^{t}HZBE$ is less than $^{t}LZBE$.
8. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
9. $\overline{WE}$ is HIGH for READ cycle.
10. Device is continuously selected. Chip enable is held in its active state.
11. Address valid prior to, or coincident with, the latest occurring chip enable.
12. $\overline{BHE}$ and $\overline{BLE}$ are held in their active state (LOW).
13. The output will be in the High-Z state if output enable is HIGH.

READ CYCLE NO. 1 [9, 10, 12]

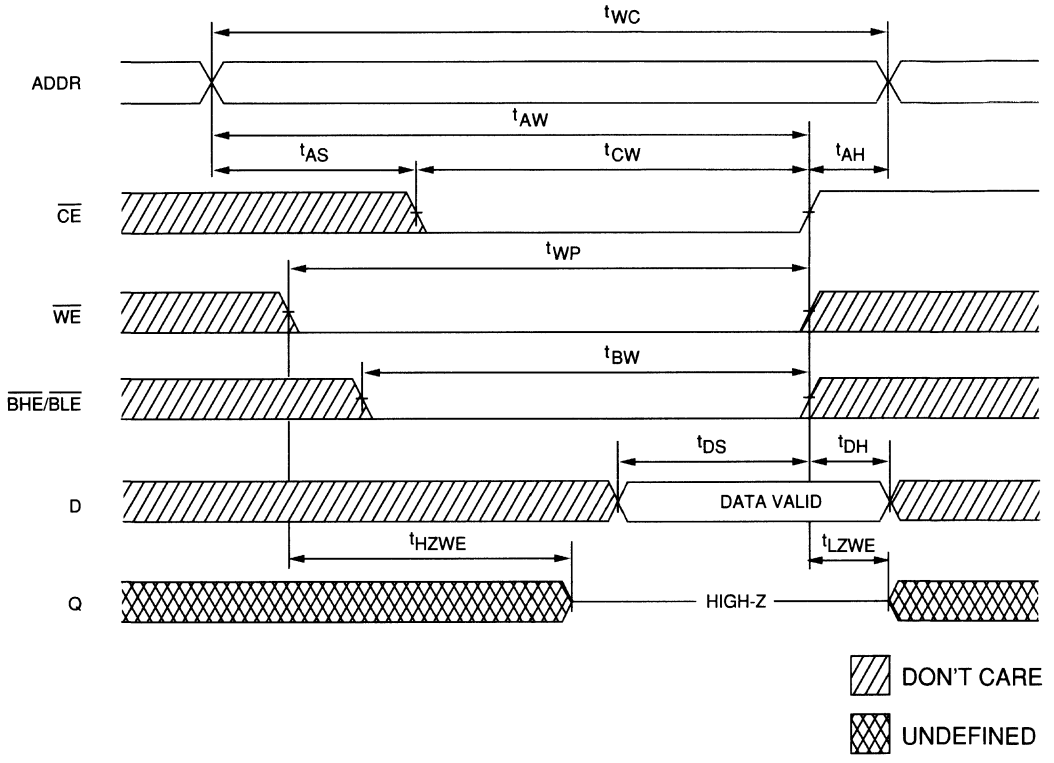


READ CYCLE NO. 2 [7, 9]

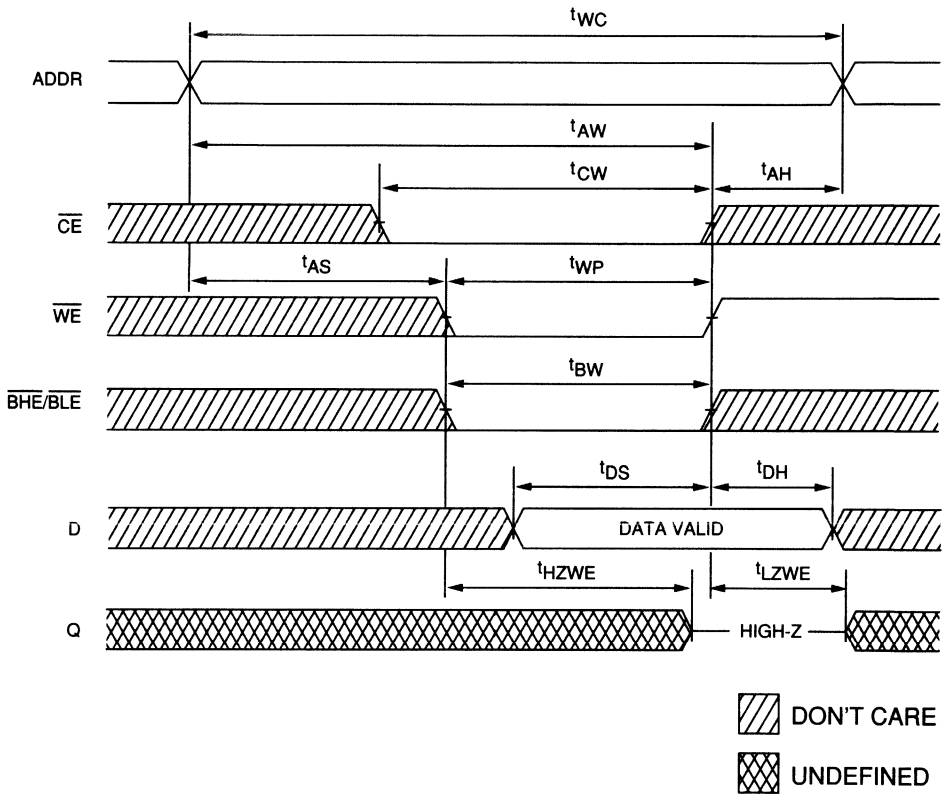


WRITE CYCLE NO. 1 [8, 13]

Chip Enable Controlled

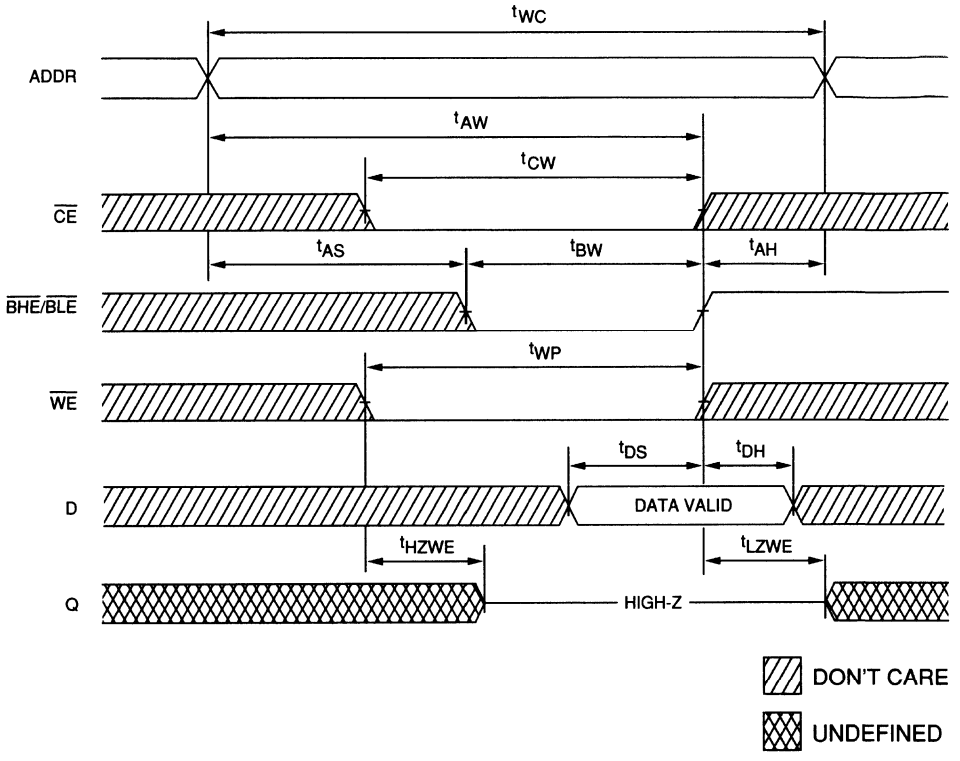


WRITE CYCLE NO. 2 [8, 13]
Write Enable Controlled



WRITE CYCLE NO. 3 [7, 8, 13]

Byte Enable Controlled



SRAM

256K x 16 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Separate upper and lower byte control ($\overline{BHE}$, $\overline{BLE}$)
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 6ns

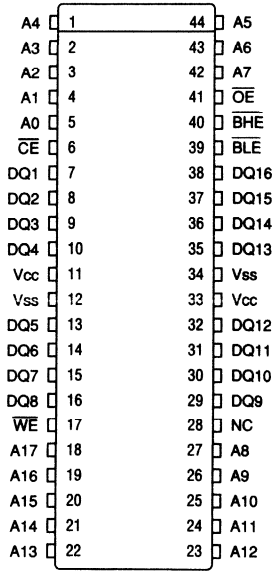
OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ

  NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.
- 2V data retention — L
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C256K16B2DJ-12 L IT

PIN ASSIGNMENT (Top View)

44-Pin SOJ
(SD-7)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for very high performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{OE}$ and $\overline{CE}$ go LOW. The high and low bytes of both the READ and WRITE operations are controlled by $\overline{BHE}$ and $\overline{BLE}$ respectively.

The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to Vss ..... -1V to Vcc+1V
IT ..... -40°C to +85°C
AT ..... -40°C to +125°C
XT ..... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX								
DESCRIPTION	CONDITIONS	SYMBOL	-8†	-10	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	180	165	150	130	120	110	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	65	60	55	45	40	35	35	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	5	mA	

† These are preliminary specifications.

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or ≤ -0.2V	V_{CC} = 2V	I_{CCDR}	95	300	µA	
		V_{CC} = 3V		125	550	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5††	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

†† The MT5C1601 device has an input capacitance maximum of 7pF.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^tRC	8		10		12		15		20		25		35		ns	
Address access time	^tAA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		7		8		10		12		15		20		30	ns	
Output hold from address change	^tOH	2		2		2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		1		1		1		ns	7
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25		35	ns	
Output Enable access time (x8)	^tAOE		4.5		5		6		7		8		8		15	ns	
Output Enable access time (x4)	^tAOE		3.5		4		5		6		7		8		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z (x8)	^tHZOE		4.5		5		5		6		7		8		8	ns	6
Output disable to output in High-Z (x4)	^tHZOE		3.5		4		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^tWC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	6.5		8		10		12		15		20		25		ns	
Address valid to end of write	^tAW	6.5		8		10		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	5.5		7		8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		25		ns	
Data setup time	^tDS	4.5		6		7		8		9		10		12		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8		8	ns	6, 7

*These specifications are preliminary.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to Vcc ..... -1V to Vcc+1V
IT ..... -40°C to +85°C
AT ..... -40°C to +125°C
XT ..... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-8†	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	180	165	150	130	120	110	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	65	60	55	45	40	35	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	mA	

† These are preliminary specifications.

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or ≤ -0.2V	V_{CC} = 2V	I_{CCDR}	95	300	µA	
		V_{CC} = 3V		125	550	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5††	pF	4
Output Capacitance	V_{CC} = 5V	C_O	7	pF	4

†† The MT5C6401 device has an input capacitance maximum of 7pF.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	8		10		12		15		20		25		ns	
Address access time	^tAA		8		10		12		15		20		25	ns	
Chip Enable access time	^tACE		7		8		10		12		15		20	ns	
Output hold from address change	^tOH	2		2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	1		1		1		1		1		1		ns	7
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25	ns	
Output Enable access time (x8)	^tAOE		4.5		5		6		7		8		8	ns	
Output Enable access time (x4)	^tAOE		3.5		4		5		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z (x8)	^tHZOE		4.5		5		5		6		7		8	ns	6
Output disable to output in High-Z (x4)	^tHZOE		3.5		4		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	8		10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	6.5		8		10		12		15		20		ns	
Address valid to end of write	^tAW	6.5		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	5.5		7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		ns	
Data setup time	^tDS	4		6		7		8		9		10		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		1		1		1		ns	7
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1V
IT ..... -40°C to +85°C
AT ..... -40°C to +125°C
XT ..... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	180	160	130	120	100	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	45	35	30	30	30	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	8	8	8	8	8	mA	

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ -0.2V	V_{CC} = 2V	I_{CCDR}	35	600	µA	
		V_{CC} = 3V		90	1000	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-12*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	2		3		3		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		8		8		10		10		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to out put in High-Z	^tHZOE		6		7		7		7		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		20		30		ns	
Chip Enable to end of write	^tCW	10		12		15		18		20		ns	
Address valid to end of write	^tAW	10		12		15		18		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	10		12		15		18		20		ns	
WRITE pulse width	$^tWP2$	12		12		15		18		20		ns	
Data setup time	^tDS	8		9		10		12		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		3		4		4		ns	7
Write Enable to output in High-Z	^tHZWE		8		8		10		10		15	ns	6, 7

*Preliminary

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to Vcc ..... -1V to Vcc+1V
IT ..... -40°C to +85°C
AT ..... -40°C to +125°C
XT ..... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	95	150	135	125	120	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	17	45	40	35	32	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	14
"L" version only	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or $\le$ -0.2V	V_{CC} = 2V	I_{CCDR}	35	1,000	µA	
		V_{CC} = 3V		70	1,500	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	t_{RC}	20		25		35		45		ns	
Address access time	t_{AA}		20		25		35		45	ns	
Chip Enable access time	t_{ACE}		20		25		35		45	ns	
Output hold from address change	t_{OH}	3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		3		3		ns	7
Chip disable to output in High-Z	t_{HZCE}		8		10		15		18	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		20		25		35		45	ns	
Output Enable access time	t_{AOE}		6		8		12		15	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		6		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	t_{WC}	20		25		35		45		ns	
Chip Enable to end of write	t_{CW}	12		15		20		25		ns	
Address valid to end of write	t_{AW}	12		15		20		25		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP1}	12		15		20		25		ns	
WRITE pulse width	t_{WP2}	15		15		20		25		ns	
Data setup time	t_{DS}	8		10		15		20		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	3		3		3		3		ns	7
Write Enable to output in High-Z	t_{HZWE}		8		10		15		18	ns	6, 7

MICRON

3.3V SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Time (ns)	Access Package and Number of Pins					Page
				PDIP	SOJ	ZIP	SOIC	TSOP	
256K x 1	$\overline{CE}$ only with separate I/O	MT5LC2561	15, 20, 25, 35	24	24	-	-	-	2-1
1 Meg x 1	$\overline{CE}$ only with separate I/O	MT5LC1001	20, 25, 35, 45	28	28	-	-	-	2-9
64K x 4	$\overline{CE}$ only	MT5LC2564	15, 20, 25, 35	24	24	-	24	-	2-17
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC2565	15, 20, 25, 35	28	28	-	-	-	2-25
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1005	20, 25, 35, 45	28	28	-	-	-	2-33
256K x 4	$\overline{CE}$ and center pin power and ground	MT5LC256K4D4	20, 25	-	32	-	-	32	2-41
1 Meg x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1M4C3	20, 25, 35, 55	-	32	-	-	-	2-51
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5LC1M4D4	20, 25, 35	-	32	-	-	32	2-53
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC2568	15, 20, 25, 35	28	28	28	-	-	2-61
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5LC1008	20, 25, 35, 45	32	32	-	-	-	2-69
128K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5LC128K8D4	20, 25	-	32	-	-	32	2-77
512K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC512K8C3	20, 25, 35, 55	-	32	-	-	-	2-87
512K x 8	$\overline{CE}$, $\overline{OE}$ and center pin power and ground	MT5LC512K8D4	20, 25, 35	-	36	-	-	36	2-89
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5LC64K16D4	20, 25	-	44	-	-	44	2-97
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and center pin power and ground	MT5LC256K16D4	20, 25, 35	-	44	-	-	-	2-107

NOTE: 1. Automotive, industrial and extended temperature specifications begin on page 1-189.
2. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

NEW 3.3 VOLT SRAM

SRAM

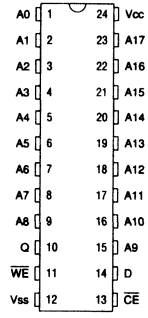
256K x 1 SRAM
LOW VOLTAGE

FEATURES
- High speed: 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

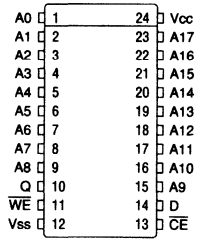
OPTIONS / MARKING
- Timing
  - 15ns access: -15
  - 20ns access: -20
  - 25ns access: -25
  - 35ns access: -35
- Packages
  - Plastic DIP (300 mil): None
  - Plastic SOJ (300 mil): DJ
- 2V data retention: L
- 2V data retention, low power: LP
- Temperature
  - Industrial (-40°C to +85°C): IT
  - Automotive (-40°C to +125°C): AT
  - Extended (-55°C to +125°C): XT
- Part Number Example: MT5LC2561DJ-20 LP IT

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

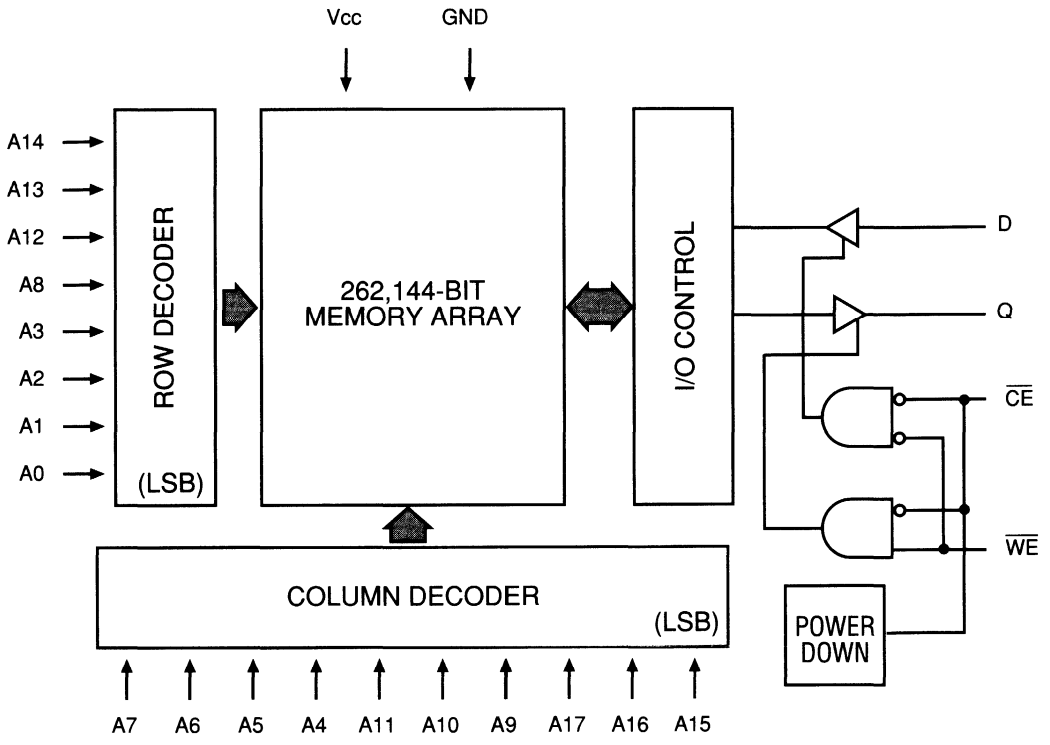
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed-systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	Vcc-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX Outputs Open f = MAX = 1/tRC	Icc	STD	55	50	45	40	mA	3, 14, 15
			LP	50	45	40	35	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX Outputs Open f = MAX = 1/tRC	I_{SB1}	STD	15	12	8	6	mA	14, 15
			LP	500	500	500	500	µA	14, 15
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD	300	300	300	300	µA	14, 15
			LP	300	300	300	300	µA	14, 15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	6	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	15		20		25		35		ns	
Address access time	^tAA		15		20		25		35	ns	
Chip Enable access time	^tACE		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		6		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		9		9		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25		35	ns	
WRITE Cycle											
WRITE cycle time	^tWC	15		20		25		35		ns	
Chip Enable to end of write	^tCW	10		15		15		20		ns	
Address valid to end of write	^tAW	10		15		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	10		15		15		20		ns	
Data setup time	^tDS	8		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

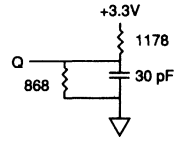


Fig. 1 OUTPUT LOAD EQUIVALENT

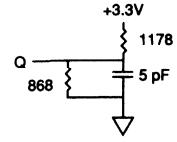


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

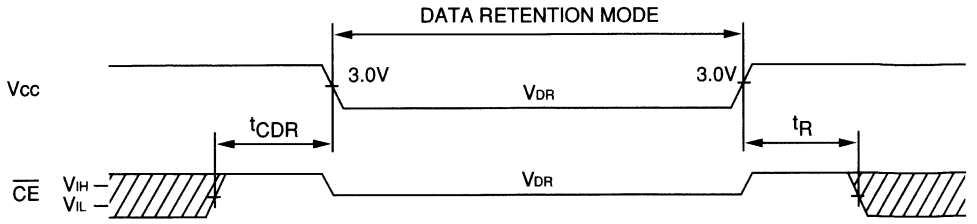
1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
15. Vcc = MAX.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

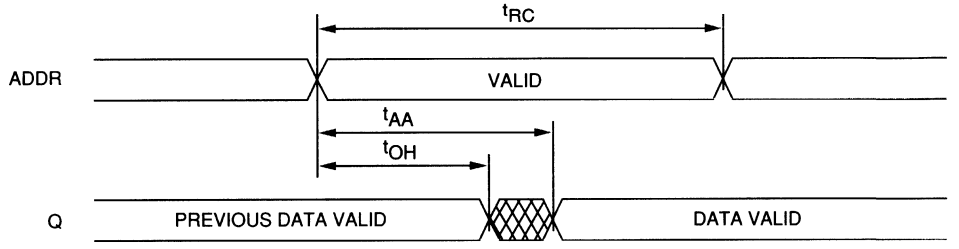
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ Vcc -0.2V Other Inputs: VIN ≥ Vcc -0.2V or VIN ≤ Vss+0.2V Vcc = 2V	ICCDR		TBD	50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

NEW 3.3 VOLT SRAM

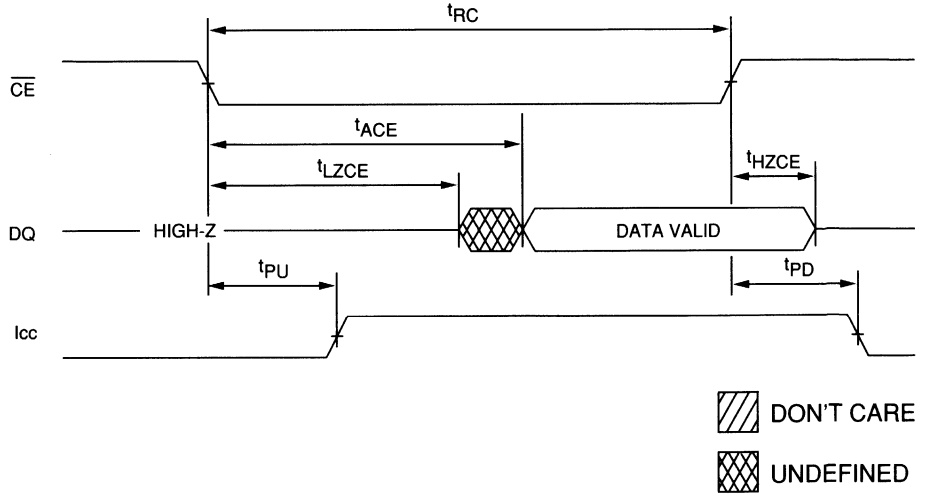
LOW Vcc DATA RETENTION WAVEFORM



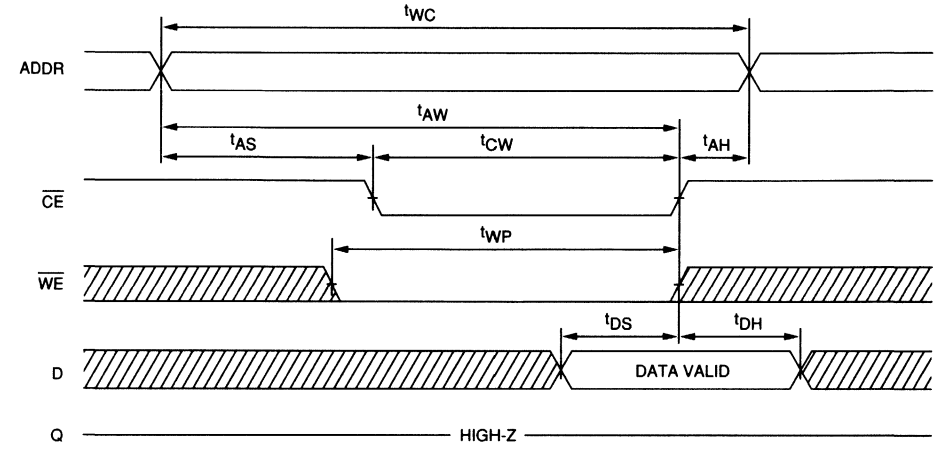
READ CYCLE NO. 1 [8, 9]



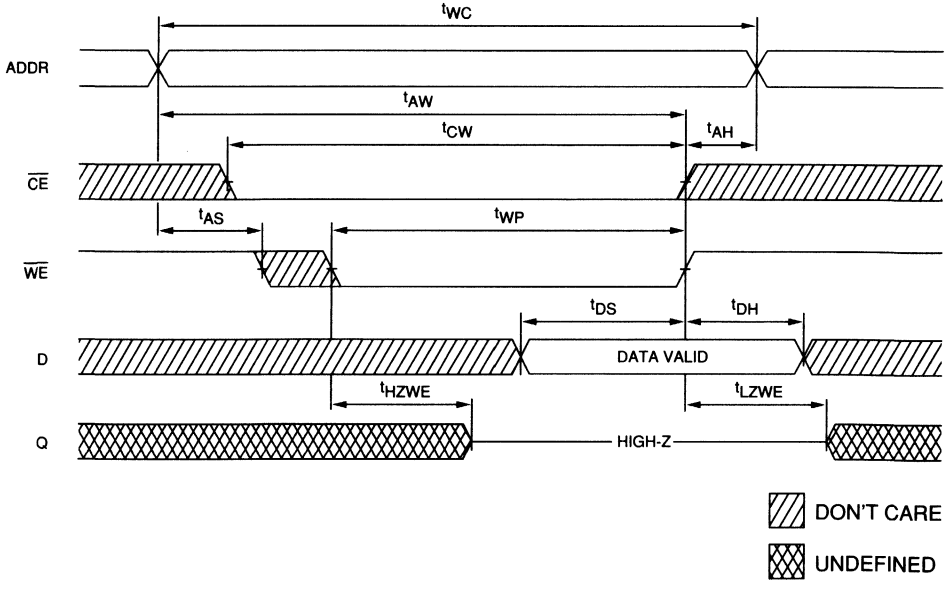
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NEW 3.3 VOLT SRAM

SRAM

1 MEG x 1 SRAM

LOW VOLTAGE

FEATURES

- High speed: 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3 power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

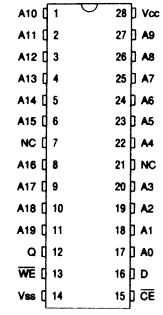
OPTIONS

	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

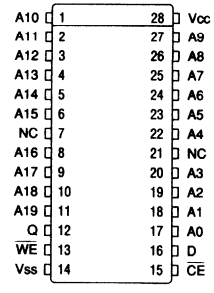
- Part Number Example: MT5LC1001DJ-25 L AT

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

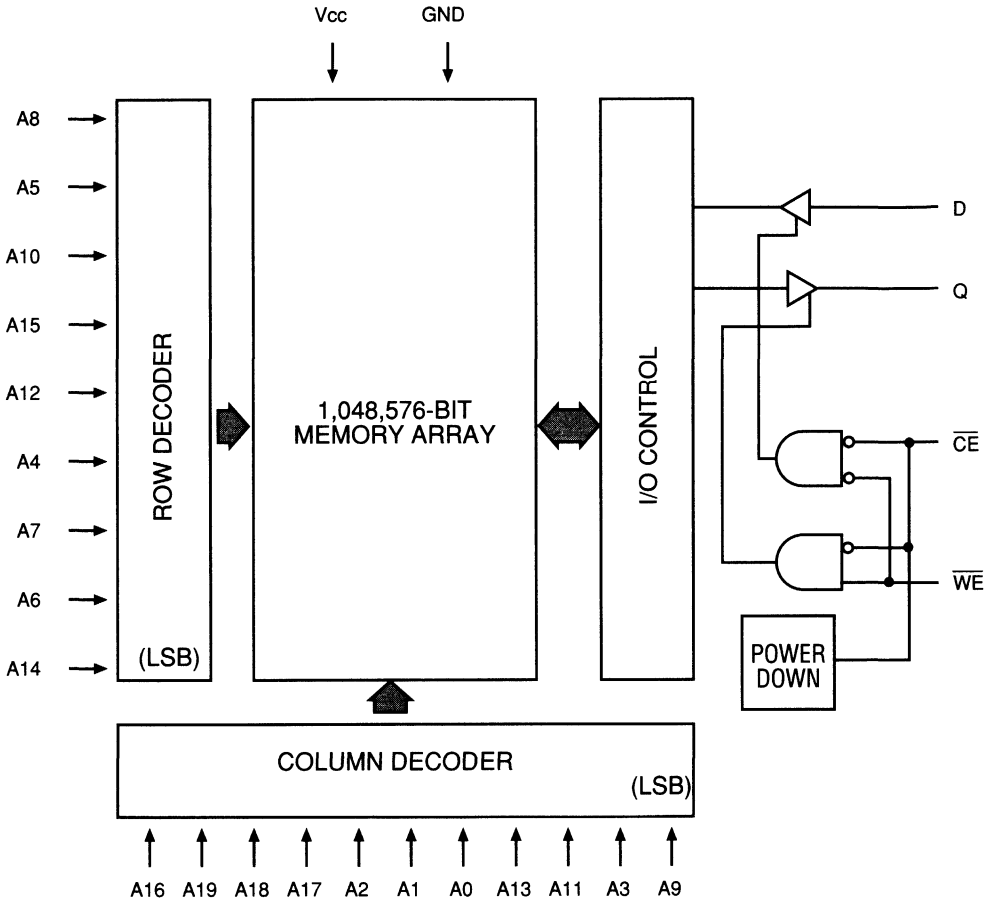
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A6 and A14) are encoded using a Gray code.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC} + 0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	Vcc-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX Outputs Open f = MAX = 1/tRC	Icc	ALL	65	55	45	40	mA	3, 15
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX Outputs Open f = MAX = 1/tRC	I_{SB1}	STD	14	12	8	6	mA	15
			LP	500	500	500	500	µA	15
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	I_{SB2}	STD	300	300	300	300	µA	15
			LP	100	100	100	100	µA	15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	Vcc = 3.3V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	20		25		35		45		ns	
Address access time	^tAA		20		25		35		45	ns	
Chip Enable access time	^tACE		20		25		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		20		25		35		45	ns	
WRITE Cycle											
WRITE cycle time	^tWC	20		25		35		45		ns	
Chip Enable to end of write	^tCW	12		15		20		25		ns	
Address valid to end of write	^tAW	12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		25		ns	
WRITE pulse width	$^tWP2$	15		15		20		25		ns	
Data setup time	^tDS	8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

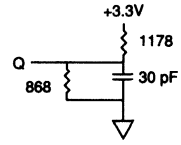


Fig. 1 OUTPUT LOAD EQUIVALENT

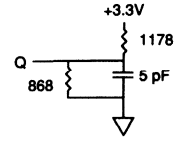


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

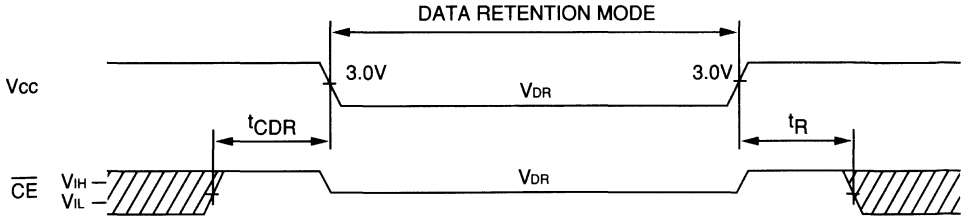
1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
15. Vcc = MAX.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

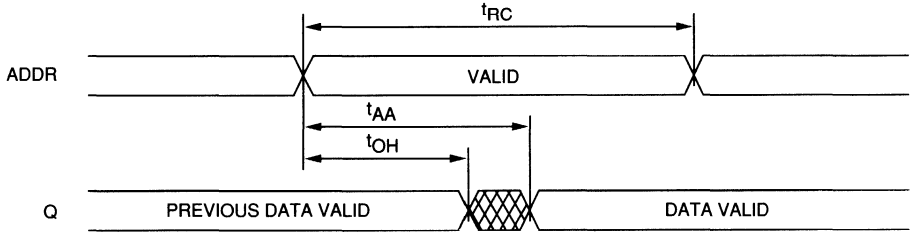
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ Vcc -0.2V Other Inputs: V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ Vss+0.2V Vcc = 2V		I_{CCDR}	TBD	50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

NEW 3.3 VOLT SRAM

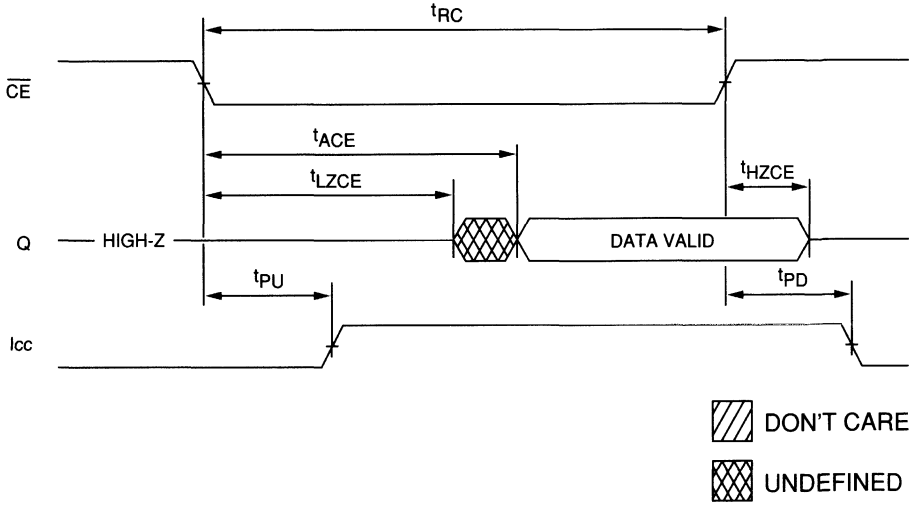
LOW Vcc DATA RETENTION WAVEFORM



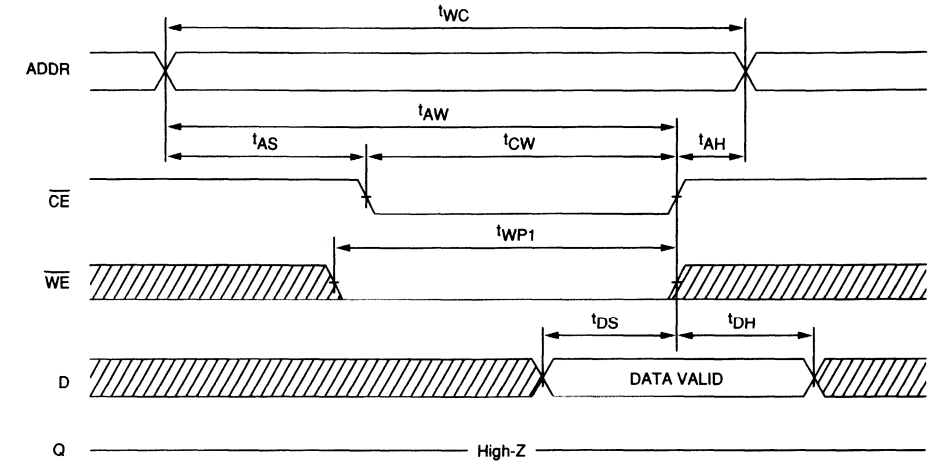
READ CYCLE NO. 1 [8, 9]



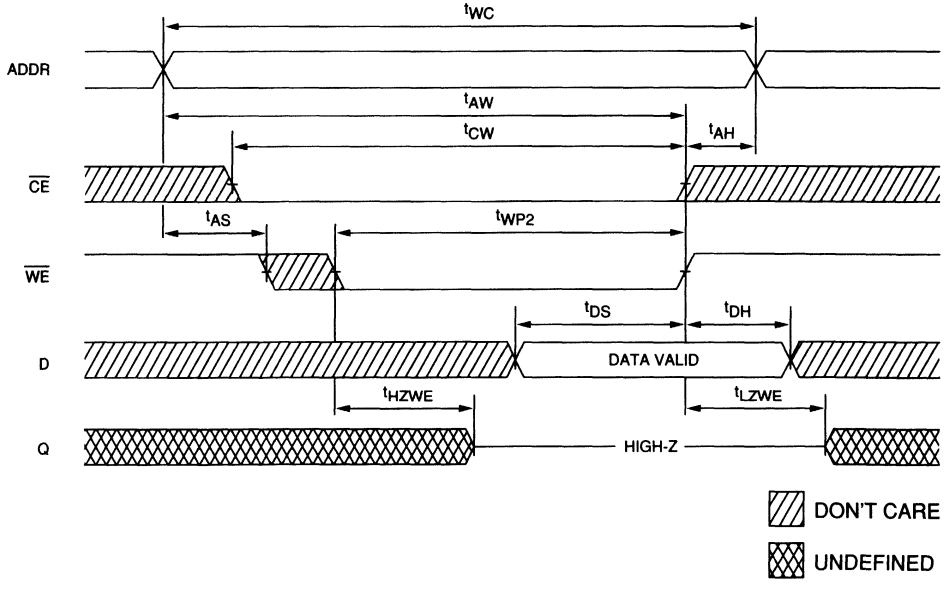
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NEW 3.3 VOLT SRAM

SRAM

64K x 4 SRAM

LOW VOLTAGE

FEATURES

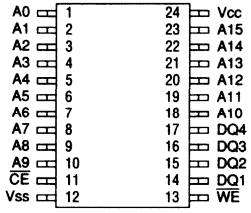
- High speed: 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS — MARKING

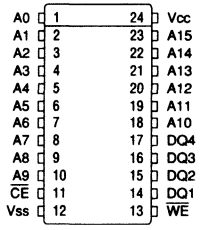
- Timing
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
  - Plastic SOIC (300 mil) — SG
- 2V data retention — L
- 2V data retention, low power — LP
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC2564SG-25 LP AT

PIN ASSIGNMENT (Top View)

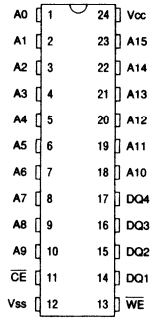
24-Pin SOIC (SF-1)



24-Pin SOJ (SD-1)



24-Pin DIP (SA-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

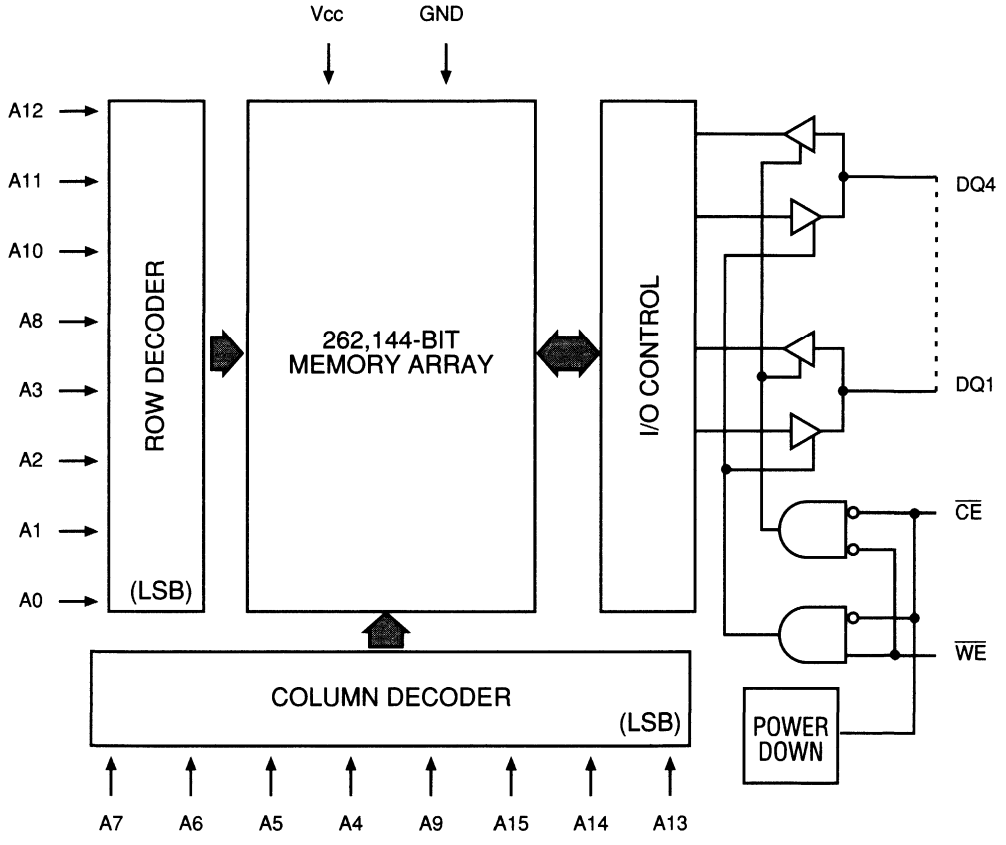
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

NEW 3.3 VOLT SRAM

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	Vcc-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX Outputs Open f = MAX = 1/tRC	Icc	STD	55	50	45	40	mA	3, 14, 15
			LP	50	45	40	35	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX Outputs Open f = MAX = 1/tRC	I_{SB1}	STD	15	12	8	6	mA	14, 15
			LP	500	500	500	500	µA	14, 15
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD	300	300	300	300	µA	14, 15
			LP	300	300	300	300	µA	14, 15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 3.3V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	15		20		25		35		ns	
Address access time	^tAA		15		20		25		35	ns	
Chip Enable access time	^tACE		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		6		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		9		9		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25		35	ns	
WRITE Cycle											
WRITE cycle time	^tWC	15		20		25		35		ns	
Chip Enable to end of write	^tCW	10		15		15		20		ns	
Address valid to end of write	^tAW	10		15		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	10		15		15		20		ns	
Data setup time	^tDS	8		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

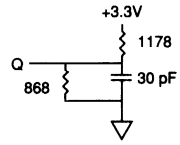


Fig. 1 OUTPUT LOAD EQUIVALENT

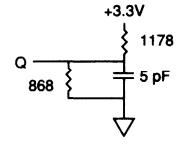


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

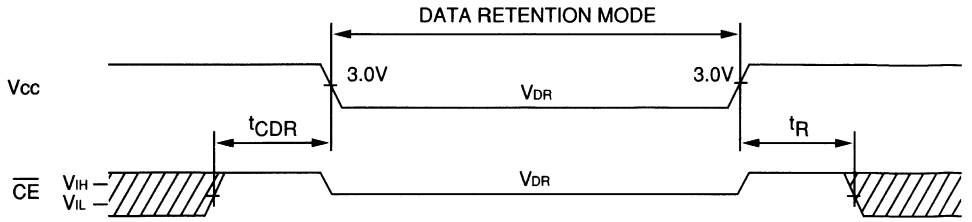
1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
15. Vcc = MAX.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

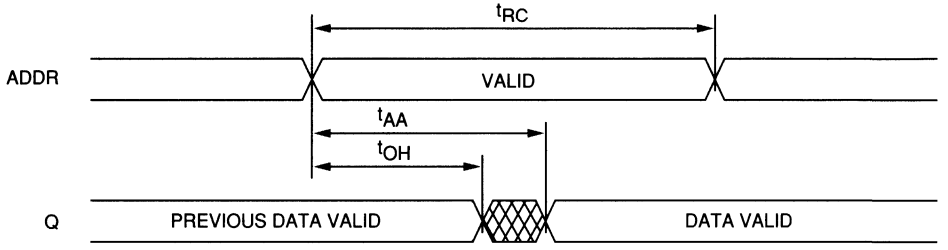
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ Vcc -0.2V Other Inputs: VIN ≥ Vcc -0.2V or VIN ≤ Vss+0.2V Vcc = 2V	ICCDR		TBD	50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

NEW 3.3 VOLT SRAM

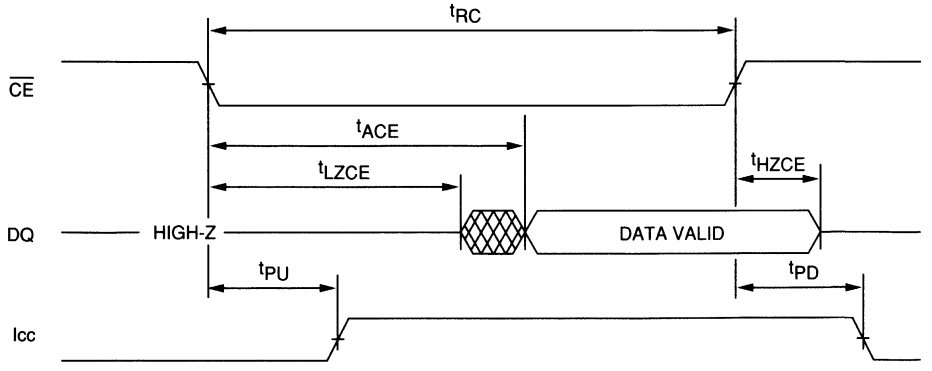
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

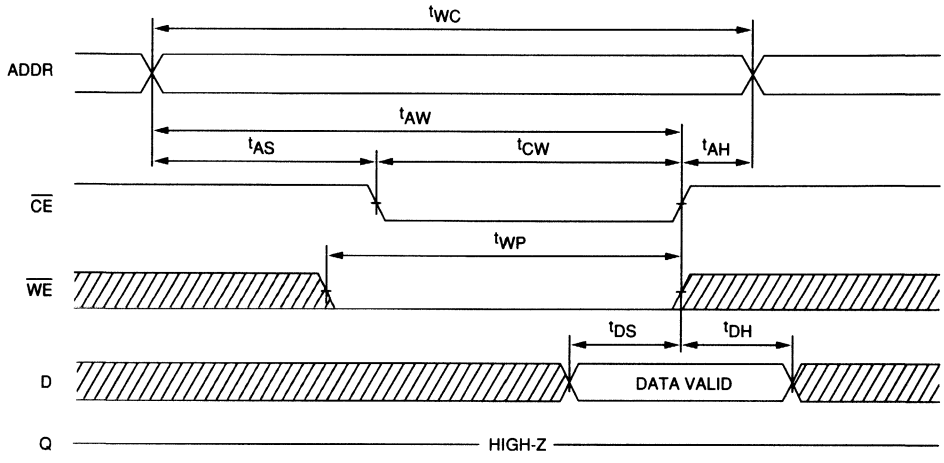


DON'T CARE

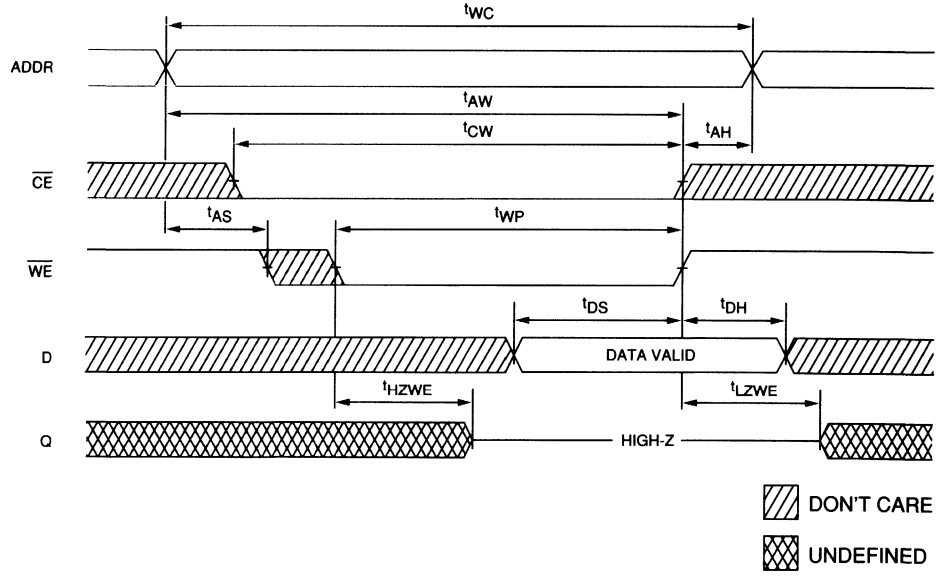
UNDEFINED

NEW 3.3 VOLT SRAM

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NEW 3.3 VOLT SRAM

SRAM

64K x 4 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- High speed: 15, 20, 25, and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

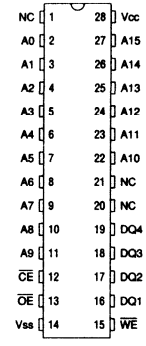
OPTIONS

	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

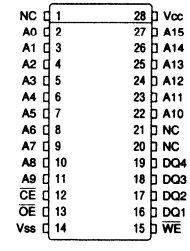
- Part Number Example: MT5LC2565DJ-25 IT

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

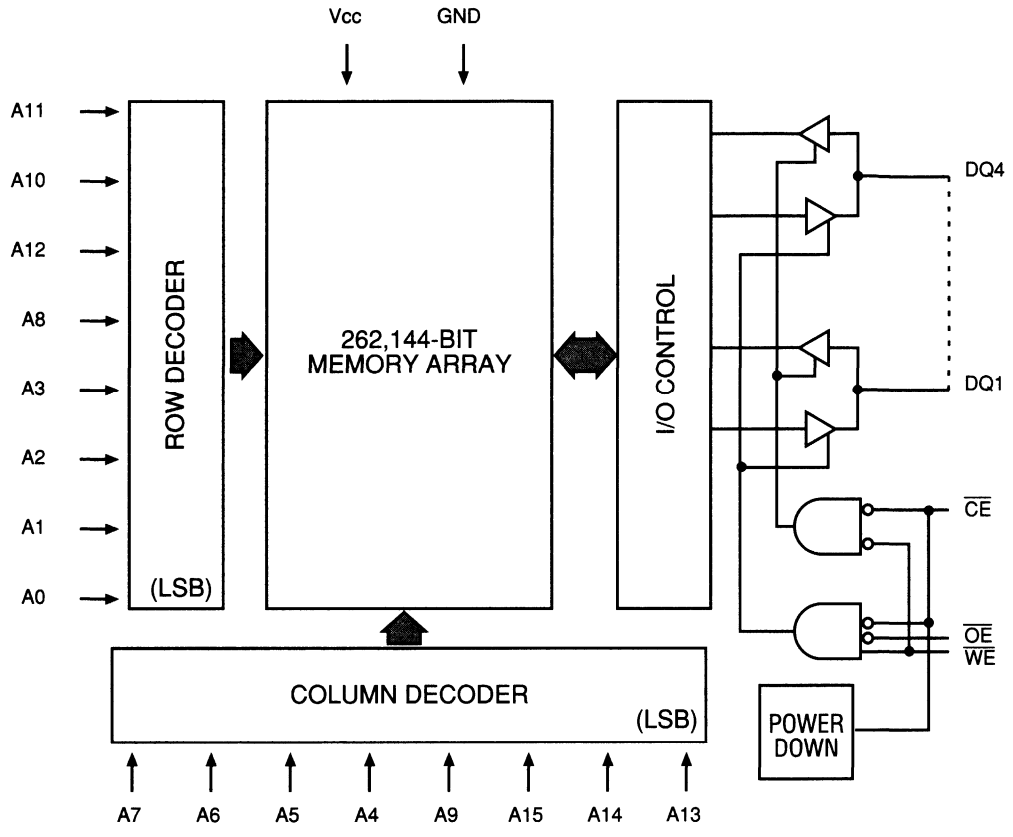
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

NEW 3.3 VOLT SRAM

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	V_{CC}-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX Outputs Open f = MAX = 1/t_{RC}	I_{CC}	STD	55	50	45	40	mA	3, 14, 15
			LP	50	45	40	35	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/t_{RC}	I_{SB1}	STD	15	12	8	6	mA	14, 15
			LP	500	500	500	500	µA	14, 15
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD	300	300	300	300	µA	14, 15
			LP	300	300	300	300	µA	14, 15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	5	pF	4

NEW

3.3 VOLT SRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	tRC	15		20		25		35		ns	
Address access time	tAA		15		20		25		35	ns	
Chip Enable access time	tACE		15		20		25		35	ns	
Output hold from address change	tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	4		6		5		5		ns	7
Chip disable to output in High-Z	tHZCE		9		9		10		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		ns	
Chip disable to power-down time	tPD		15		20		25		35	ns	
Output Enable access time	tAOE		8		8		8		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		6		7		7		12	ns	6
WRITE Cycle											
WRITE cycle time	tWC	15		20		25		35		ns	
Chip Enable to end of write	tCW	10		15		15		20		ns	
Address valid to end of write	tAW	10		15		15		20		ns	
Address setup time	tAS	0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		ns	
WRITE pulse width	tWP	10		15		15		20		ns	
Data setup time	tDS	8		10		10		15		ns	
Data hold time	tDH	0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	4		5		5		5		ns	7
Write Enable to output in High-Z	tHZWE		8		10		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

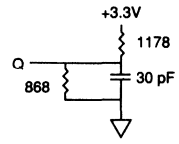


Fig. 1 OUTPUT LOAD EQUIVALENT

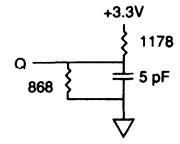


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

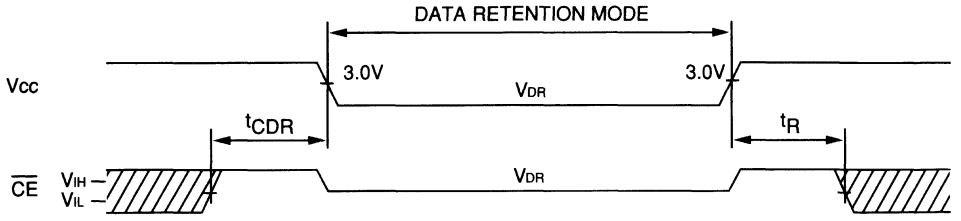
1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
15. Vcc = MAX.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

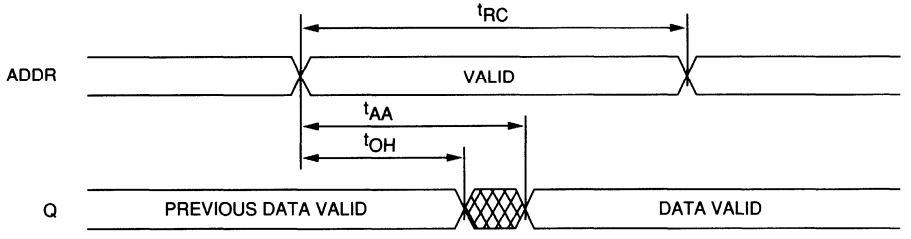
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ Vcc -0.2V Other Inputs: V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ Vss+0.2V Vcc = 2V	I_{CCDR}		TBD	50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

NEW 3.3 VOLT SRAM

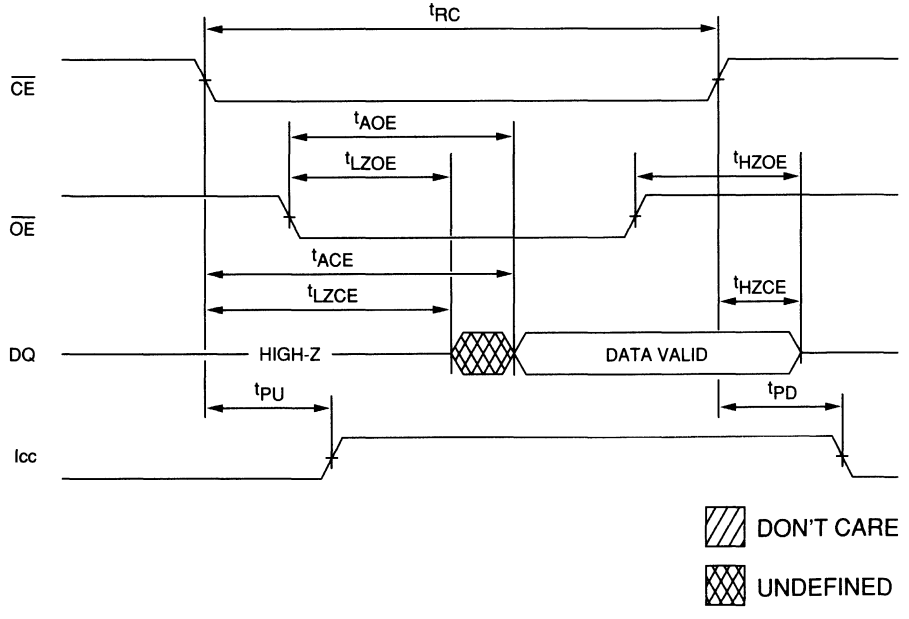
LOW Vcc DATA RETENTION WAVEFORM



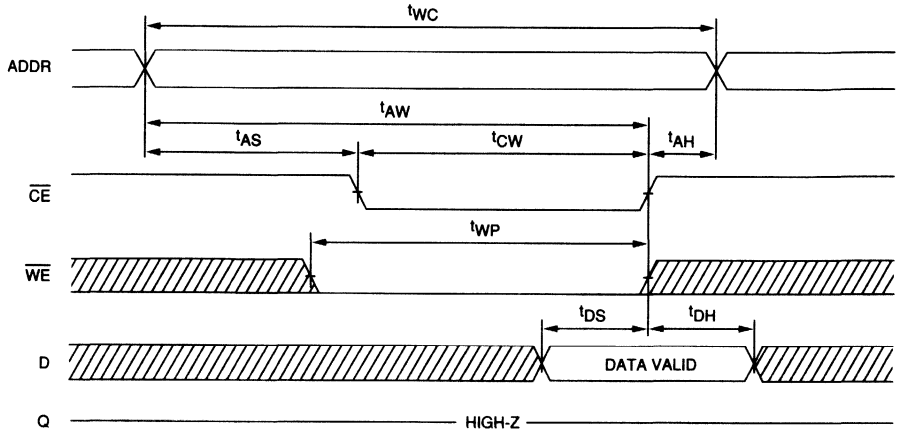
READ CYCLE NO. 1 [8, 9]



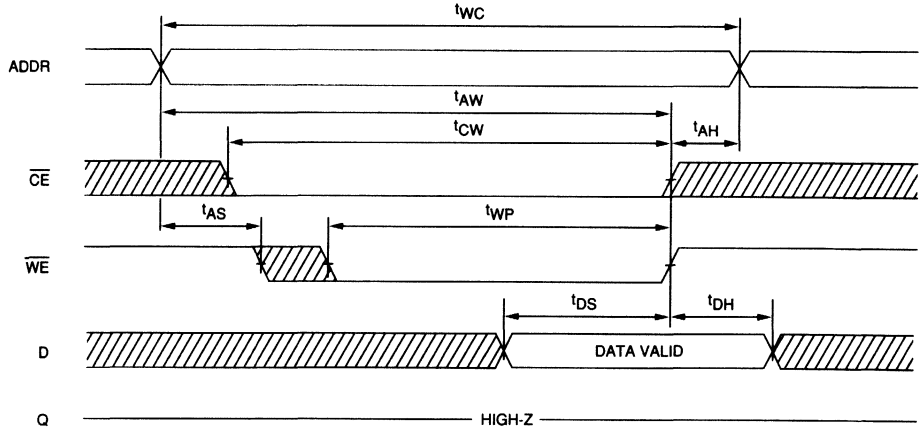
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

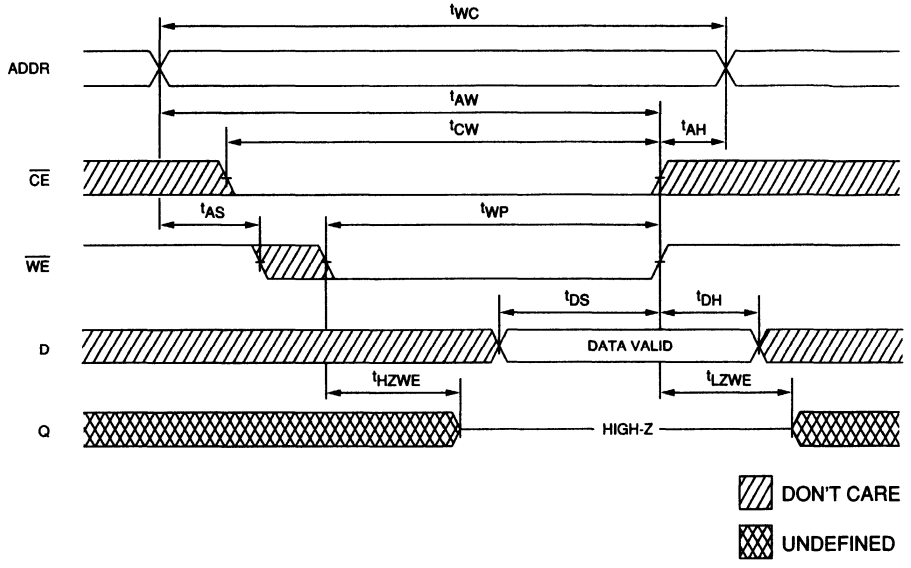


WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

256K x 4 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

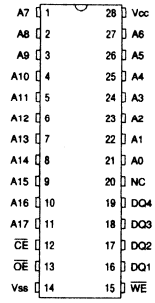
OPTIONS

	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

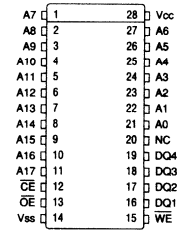
- Part Number Example: MT5LC1005DJ-35 LP IT

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

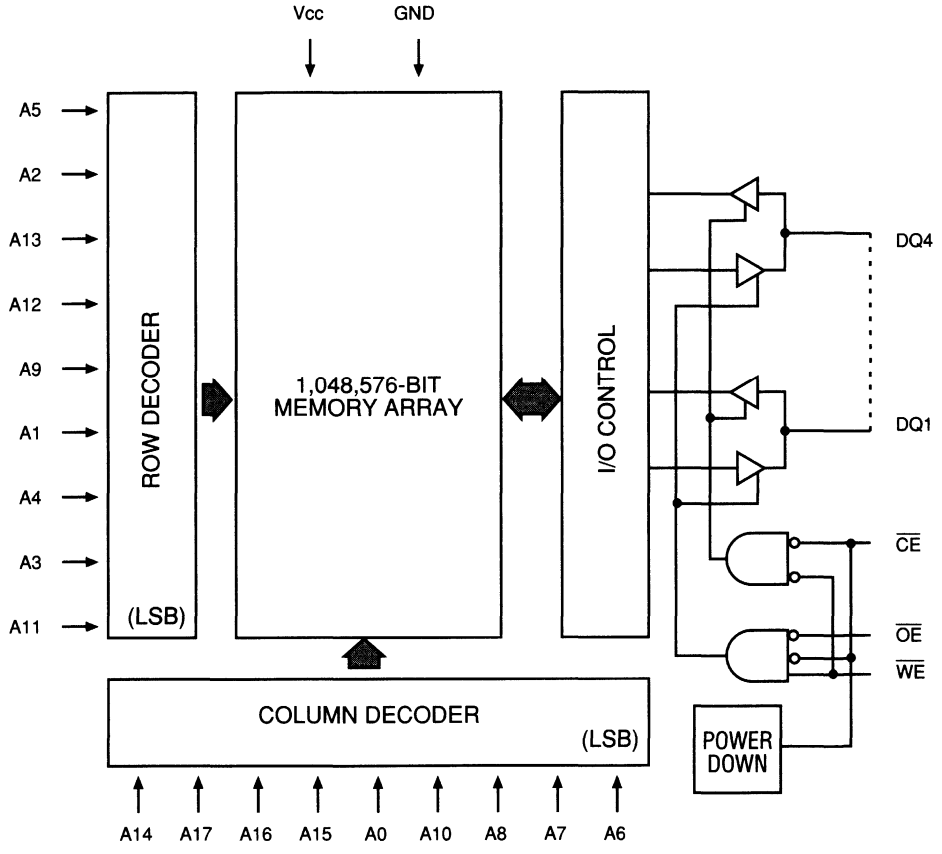
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ are LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A11 and A3) are encoded using a Gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .....-0.5V to +4.6V
V_{IN}.....-0.5V to V_{CC} + 0.5V (+4.6V MAX)
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	V_{CC}-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX Outputs Open f = MAX = $1/^tRC$	I_{CC}	ALL	65	55	45	40	mA	3, 15
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = $1/^tRC$	I_{SB1}	STD	14	12	8	6	mA	15
			LP	500	500	500	500	µA	15
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	STD	300	300	300	300	µA	15
			LP	100	100	100	100	µA	15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	20		25		35		45		ns	
Address access time	^tAA		20		25		35		45	ns	
Chip Enable access time	^tACE		20		25		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD	20			25		35		45	ns	
Output Enable access time	^tAOE		4		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	20		25		35		45		ns	
Chip Enable to end of write	^tCW	12		15		20		25		ns	
Address valid to end of write	^tAW	12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		25		ns	
WRITE pulse width	$^tWP2$	15		15		20		25		ns	
Data setup time	^tDS	8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

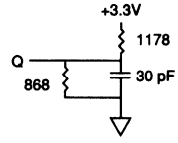


Fig. 1 OUTPUT LOAD EQUIVALENT

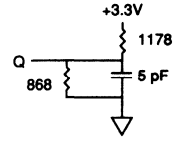


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

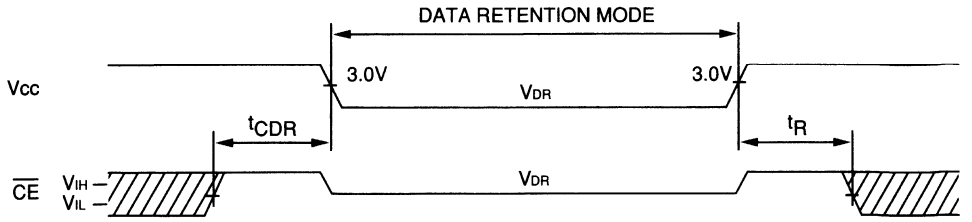
1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
15. Vcc = MAX.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

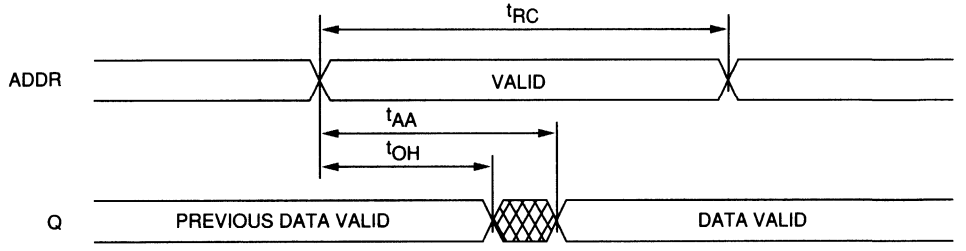
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ Vcc -0.2V Other Inputs: VIN ≥ Vcc -0.2V or VIN ≤ Vss+0.2V Vcc = 2V	ICCDR		TBD	50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

NEW 3.3 VOLT SRAM

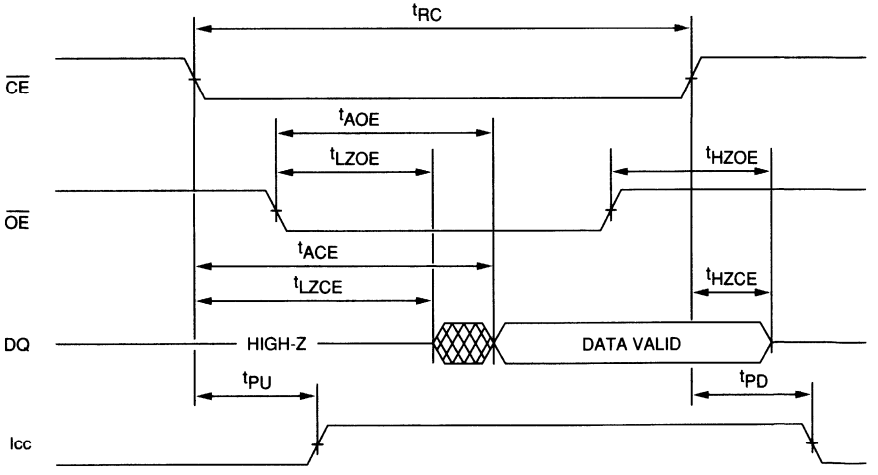
LOW Vcc DATA RETENTION WAVEFORM

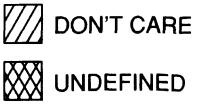


READ CYCLE NO. 1 [8, 9]

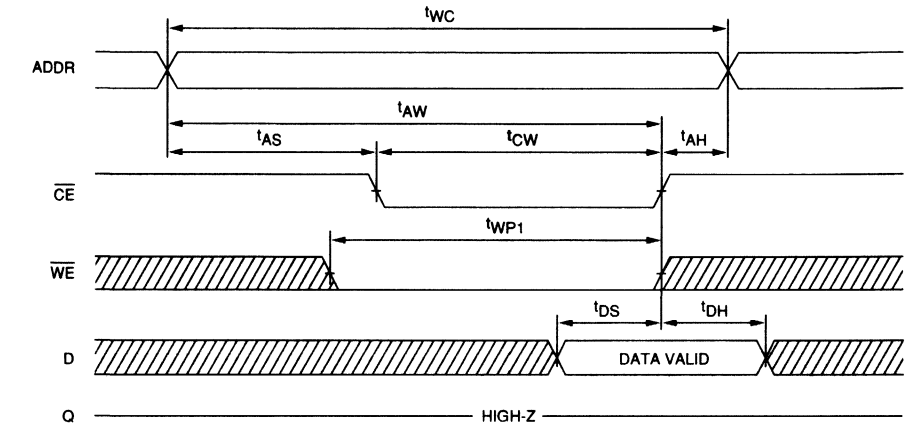


READ CYCLE NO. 2 [7, 8, 10]

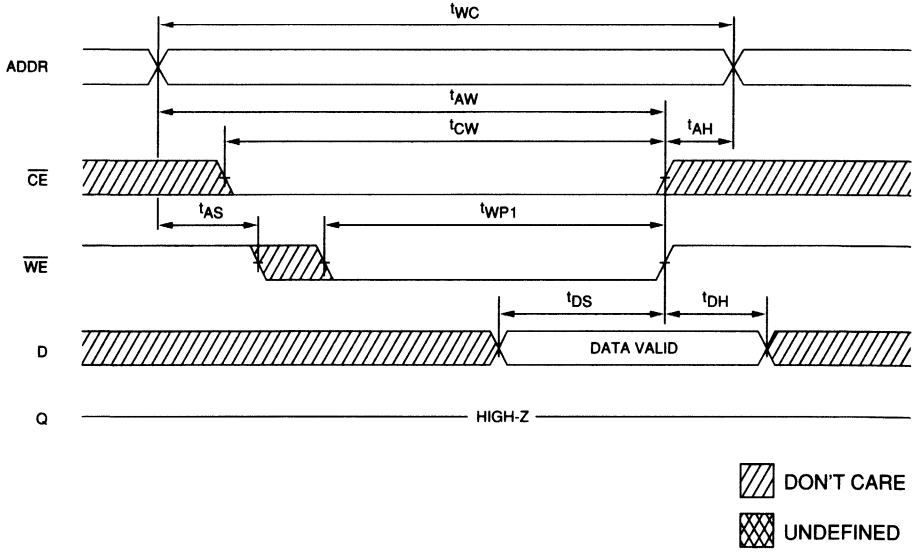




WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



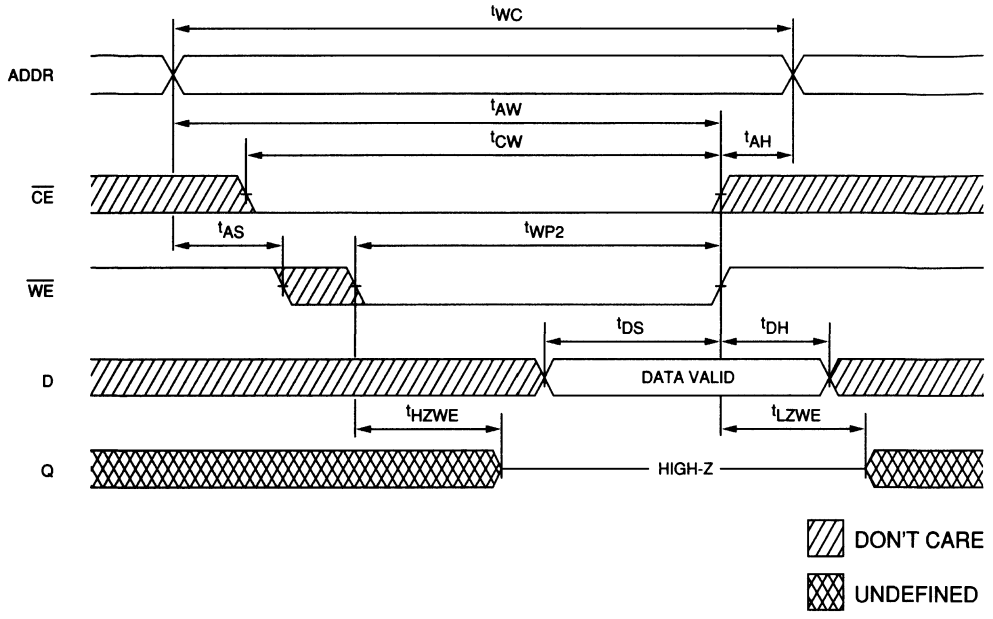
WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

NEW 3.3 VOLT SRAM

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

256K x 4 SRAM

3.3V OPERATION WITH SINGLE CHIP ENABLE

FEATURES

- High speed: 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL compatible
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Fast $\overline{OE}$ access times: 10 and 12ns

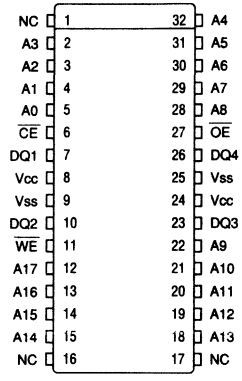
OPTIONS

MARKING

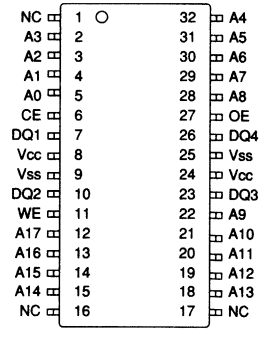
- Timing
  - 20ns access: -20
  - 25ns access: -25
- Packages
  - 32-pin SOJ (400 mil): DJ
  - 32-pin TSOP (400 mil): TG
- Part Number Example: MT5LC256K4D4TG-25

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



32-Pin TSOP
(SE-1)



GENERAL DESCRIPTION

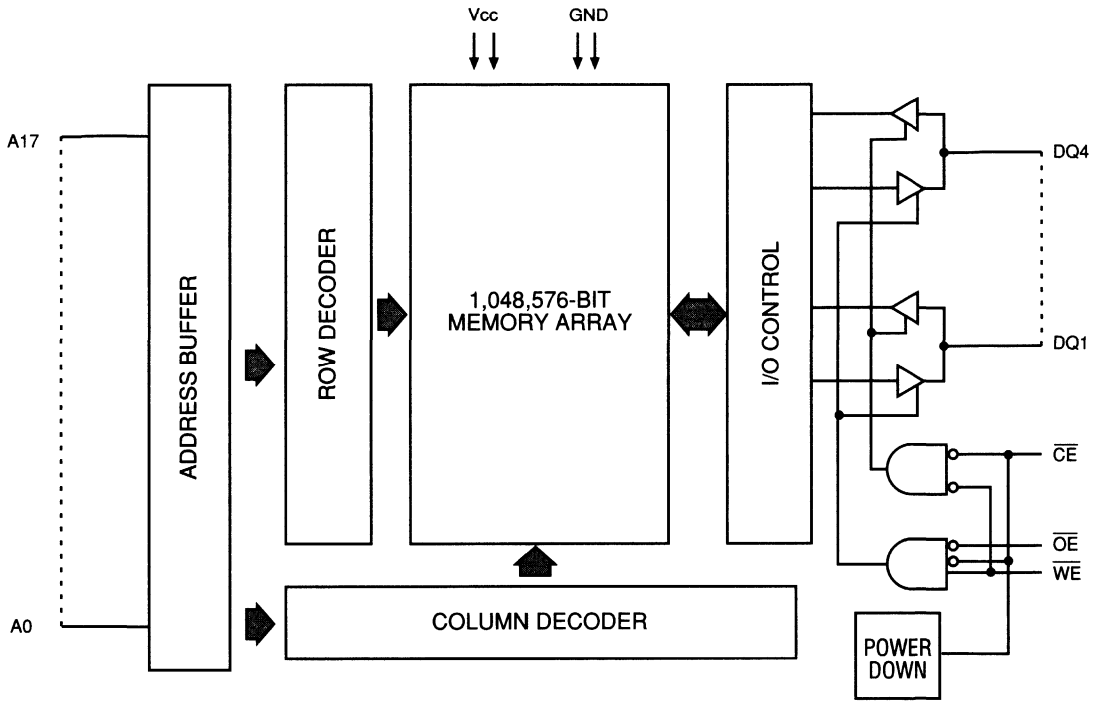
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ are LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 32, 31, 30, 29, 28, 22, 21, 20, 19, 18, 15, 14, 13, 12	A0-A17	Input	Address Inputs: These inputs determine which cell is addressed.
11	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
6	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
27	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
7, 10, 23, 26	DQ1-DQ4	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 3.3V ±0.3V
9, 25	Vss	Supply	Ground: GND
1, 16, 17	NC	-	No Connect: These signals are not internally connected.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to Vcc +0.5V (4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ± 0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC} + 0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100 µA	V_{OH}	Vcc - 0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100 µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX			
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	60	88	80	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	10	16	14	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} =3.3V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ± 0.3V)

DESCRIPTION		-20		-25			
	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle							
READ cycle time	^tRC	20		25		ns	
Address access time	^tAA		20		25	ns	
Chip Enable access time	^tACE		20		25	ns	
Output hold from address change	^tOH	5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		ns	
Chip disable to power-down time	^tPD		20		25	ns	
Output Enable access time	^tAOE		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		ns	
Output disable to output in High-Z	^tHZOE		8		8	ns	6
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	
Chip Enable to end of write	^tCW	13		15		ns	
Address valid to end of write	^tAW	12		14		ns	
Address setup time	^tAS	0		0		ns	
Address hold from end of write	^tAH	0		0		ns	
WRITE pulse width	^tWP	10		12		ns	
Data setup time	^tDS	10		10		ns	
Data hold time	^tDH	0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		ns	7
Write Enable to output in High-Z	^tHZWE		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

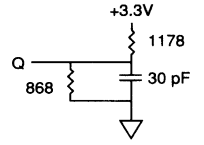


Fig. 1 OUTPUT LOAD EQUIVALENT

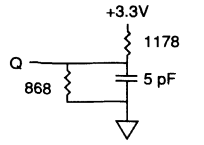
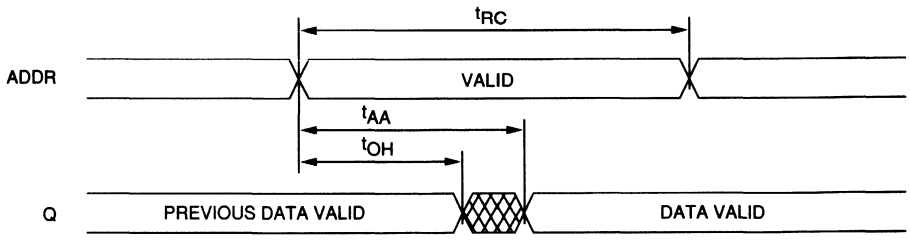


Fig. 2 OUTPUT LOAD EQUIVALENT

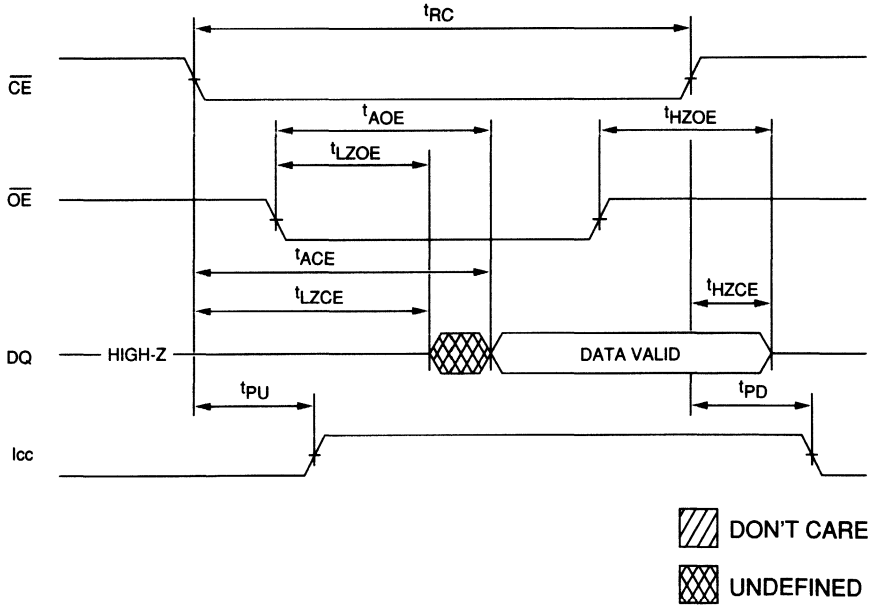
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. The output will be in the High-Z state if output enable is high.

READ CYCLE NO. 1 [8, 9]

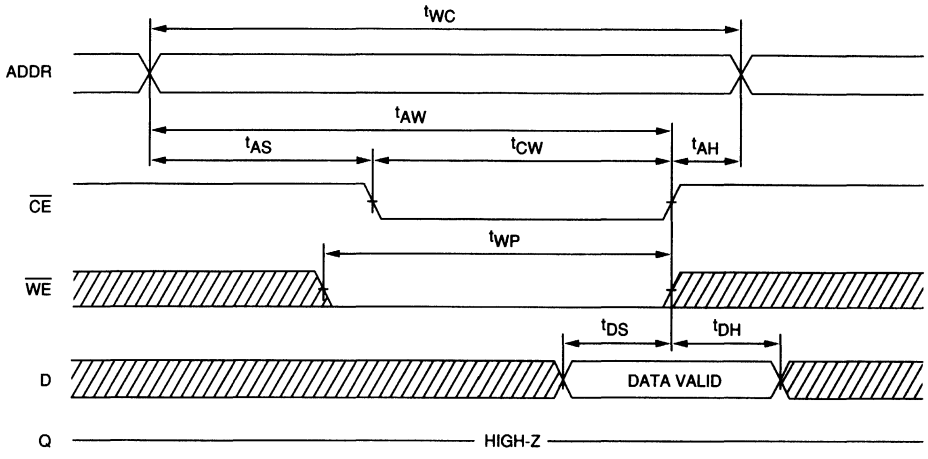


READ CYCLE NO. 2 [7, 8, 10]

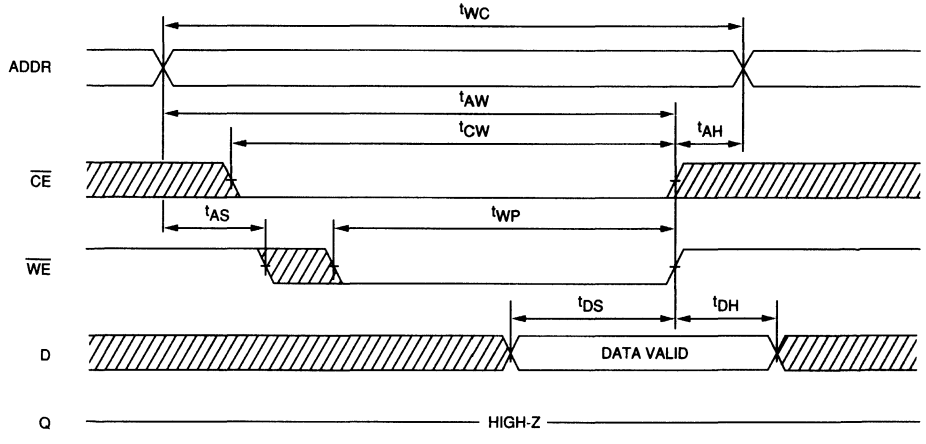


NEW 3.3 VOLT SRAM

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

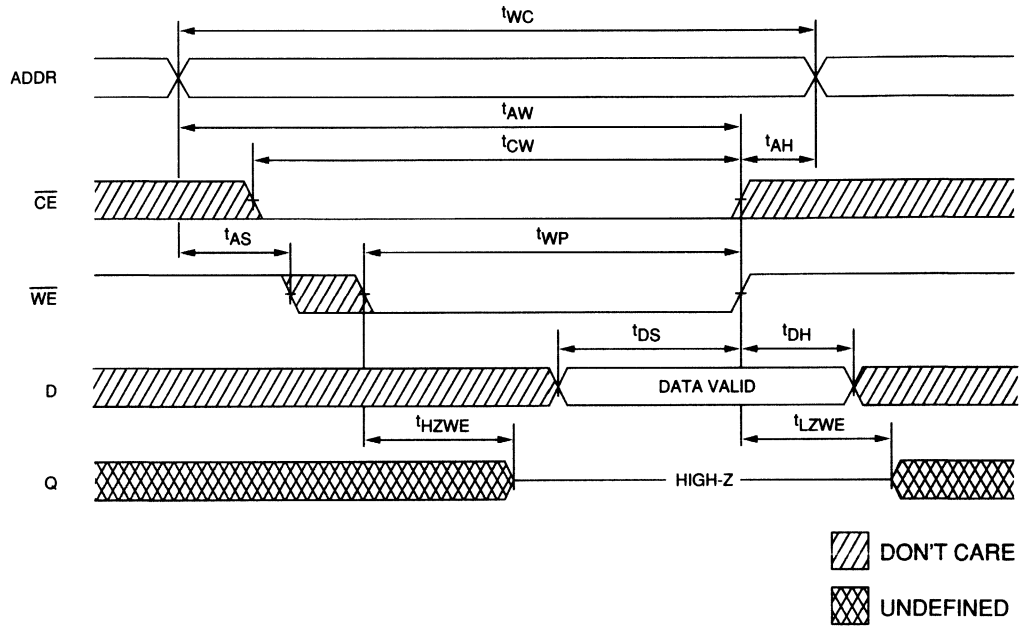


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

1 MEG x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, 35 and 55ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS

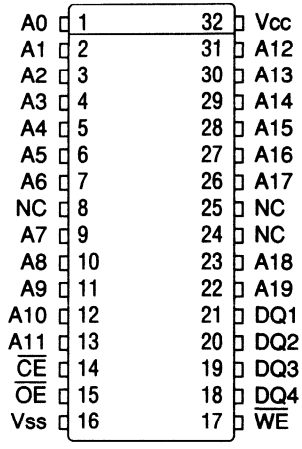
	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
55ns access	-55
• Packages	
Plastic SOJ (400 mil)	DJ
• 2V data retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- Part Number Example: MT5LC1M4C3DJ-35 L IT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

NEW 3.3 VOLT SRAM

SRAM

1 MEG x 4 SRAM

3.3V OPERATION WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 6, 8, and 10ns

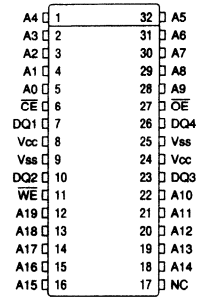
OPTIONS

	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
• 2V data retention	L
• 2V data retention, low power	LP

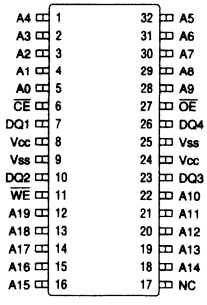
- Part Number Example: MT5LC1M4D4DJ-20LP

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



32-Pin TSOP
(SE-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

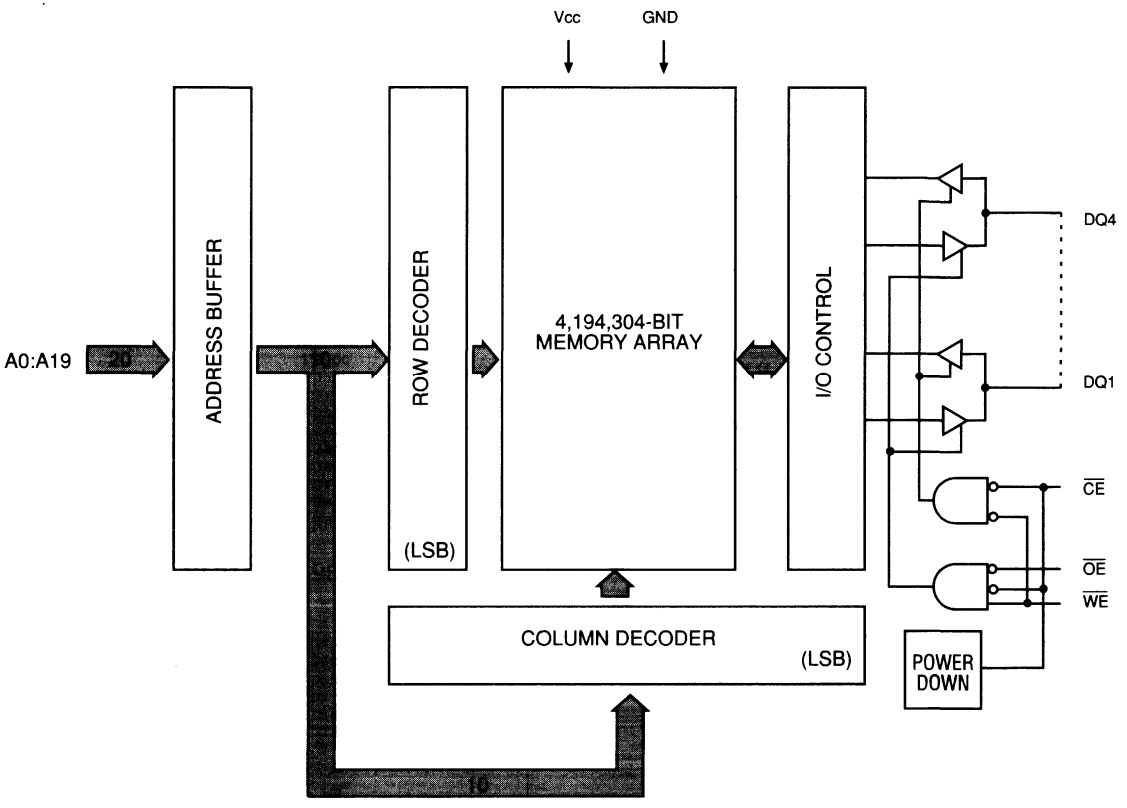
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC} + 0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC} + 0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100mA		V_{CC} -0.2			
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100mA			0.2		
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX				
DESCRIPTION	CONDITIONS	SYMBOL	VER	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC; Outputs Open	I_{CC}	ALL	55	55	50	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	STD	15	12	10	mA	
			LP	1.0	1.0	1.0	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX; f = 0 V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ V_{SS} +0.2V	I_{SB2}	STD	300	300	300	uA	
			LP	100	100	100	uA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		35		ns	
Address access time	^tAA		20		25		35	ns	
Chip Enable access time	^tACE		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		10		12	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		25		35		ns	
Chip Enable to end of write	^tCW	12		15		20		ns	
Address valid to end of write	^tAW	12		15		20		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		ns	
WRITE pulse width	$^tWP2$	15		15		20		ns	
Data setup time	^tDS	8		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

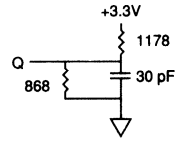


Fig. 1 OUTPUT LOAD EQUIVALENT

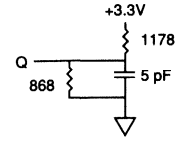


Fig. 2 OUTPUT LOAD EQUIVALENT

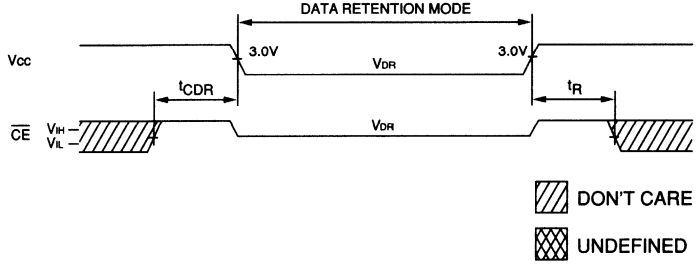
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.

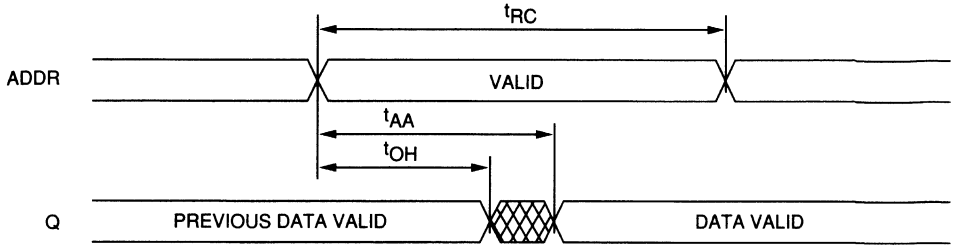
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		VDR	2		V	
Data Retention Current	Vcc = 2.0V $\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	ICCDR		50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0		ns	4
Operation Recovery Time		^{t}R	^{t}RC		ns	4, 11

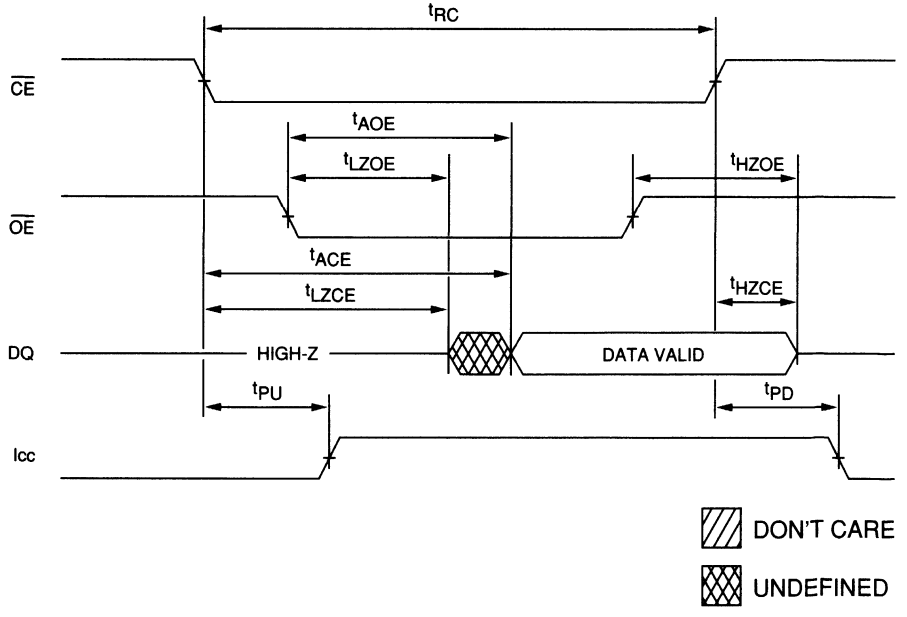
LOW Vcc DATA RETENTION WAVEFORM



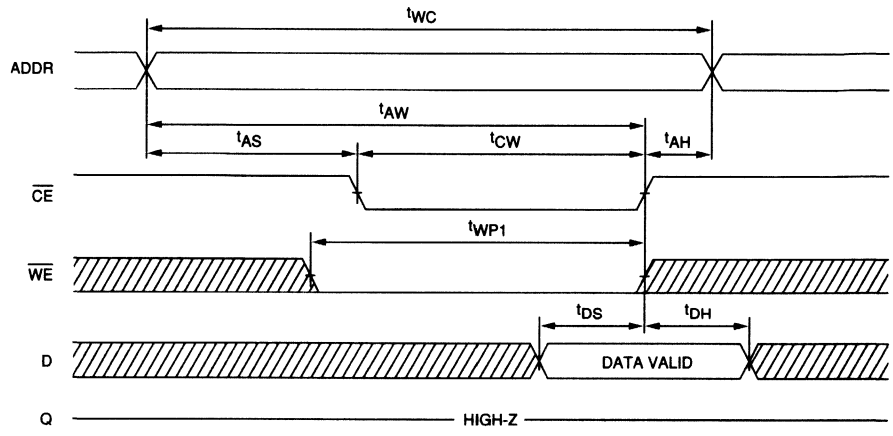
READ CYCLE NO. 1 [8, 9]



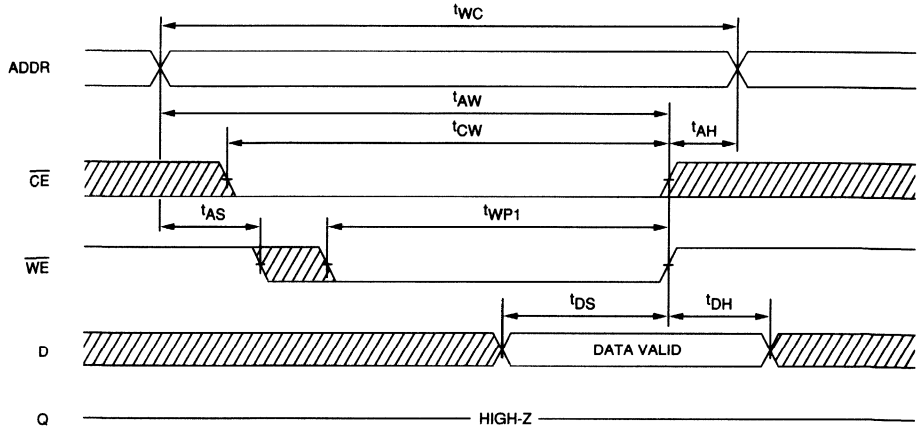
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



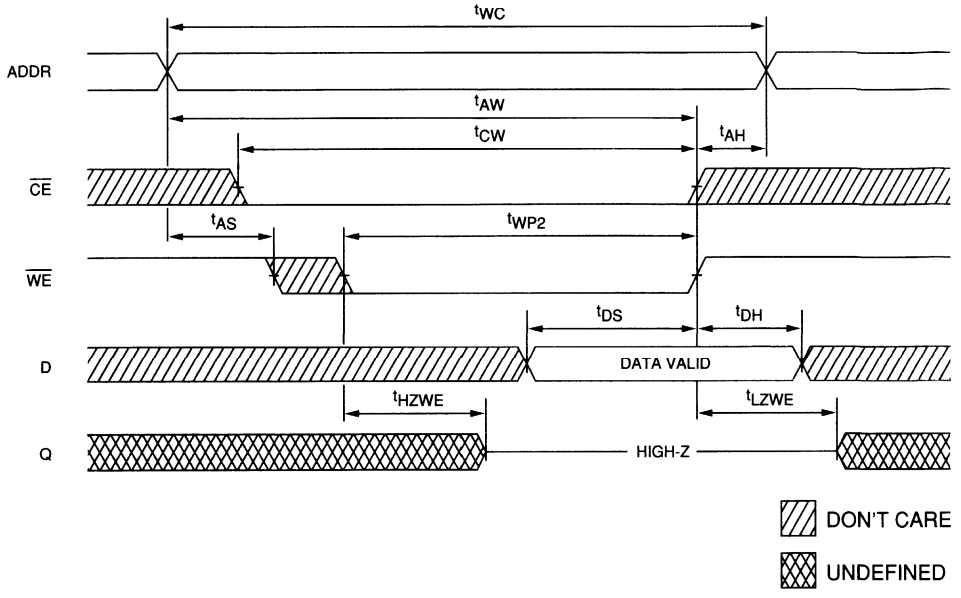
WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

NEW 3.3 VOLT SRAM

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

32K x 8 SRAM

LOW VOLTAGE

FEATURES

- High speed: 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

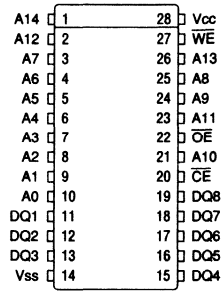
OPTIONS

	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (300 mil)	Z
• 2V data retention	L
• 2V data retention, low power	LP
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

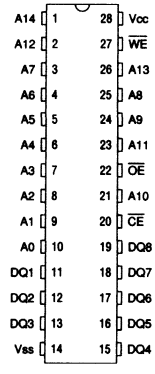
- Part Number Example: MT5LC2568Z-25 LP XT

PIN ASSIGNMENT (Top View)

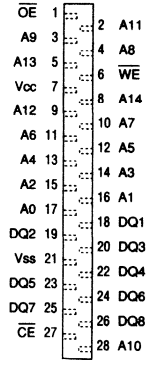
28-Pin SOJ
(SD-2)



28-Pin DIP
(SA-4)



28-Pin ZIP
(SB-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

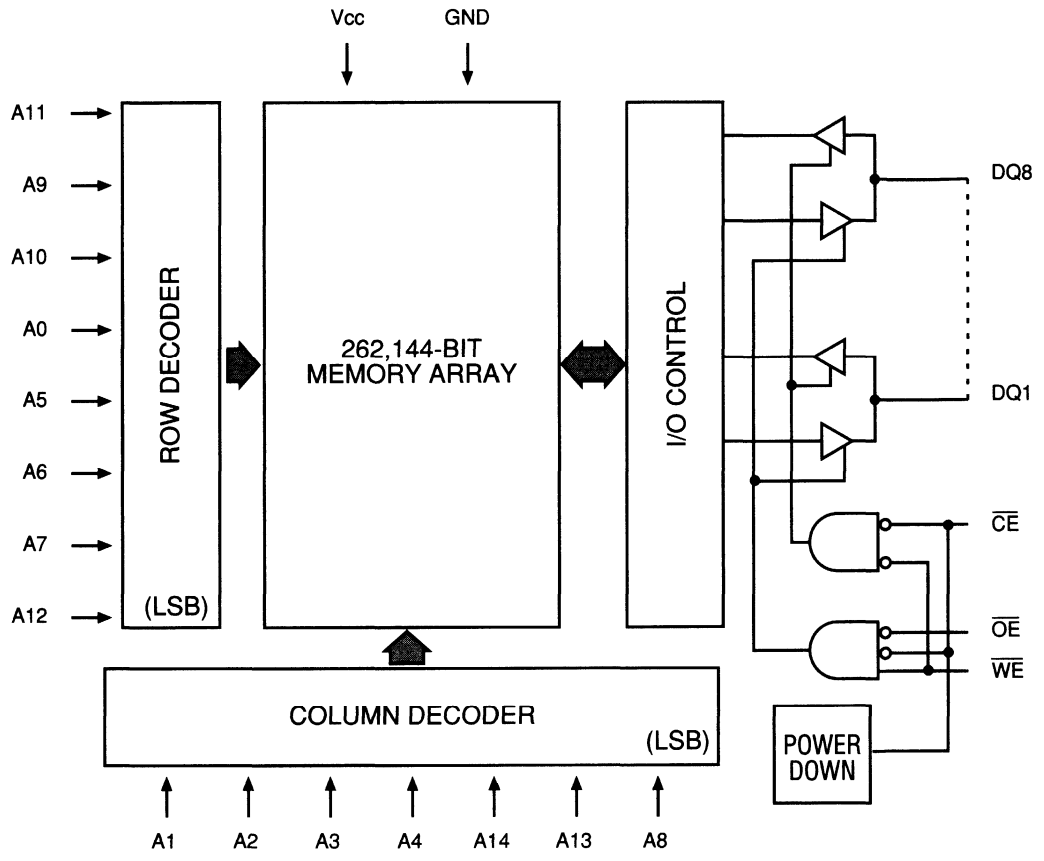
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

The MT5C2568 operates from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

NEW 3.3 VOLT SRAM

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	V_{CC}-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX Outputs Open f = MAX = 1/t_{RC}	I_{CC}	STD	55	50	45	40	mA	3, 14, 15
			LP	50	45	40	35	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/t_{RC}	I_{SB1}	STD	15	12	8	6	mA	14, 15
			LP	500	500	500	500	µA	14, 15
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD	300	300	300	300	µA	14, 15
			LP	300	300	300	300	µA	14, 15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	15		20		25		35		ns	
Address access time	^tAA		15		20		25		35	ns	
Chip Enable access time	^tACE		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	4		6		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		9		9		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25		35	ns	
Output Enable access time	^tAOE		8		8		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		7		7		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		20		25		35		ns	
Chip Enable to end of write	^tCW	10		15		15		20		ns	
Address valid to end of write	^tAW	10		15		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	10		15		15		20		ns	
Data setup time	^tDS	8		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		10		15	ns	6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

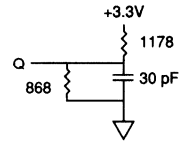


Fig. 1 OUTPUT LOAD EQUIVALENT

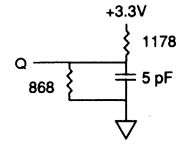


Fig. 2 OUTPUT LOAD EQUIVALENT

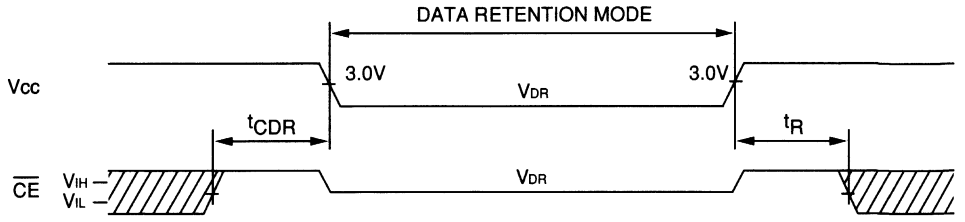
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
15. Vcc = MAX.

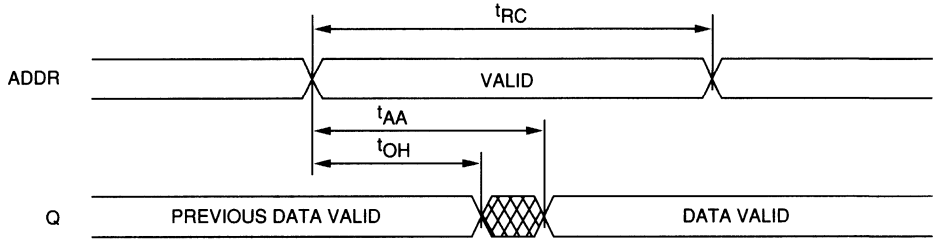
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ Vcc -0.2V Other Inputs: VIN ≥ Vcc -0.2V or VIN ≤ Vss+0.2V Vcc = 2V	ICCDR		TBD	50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

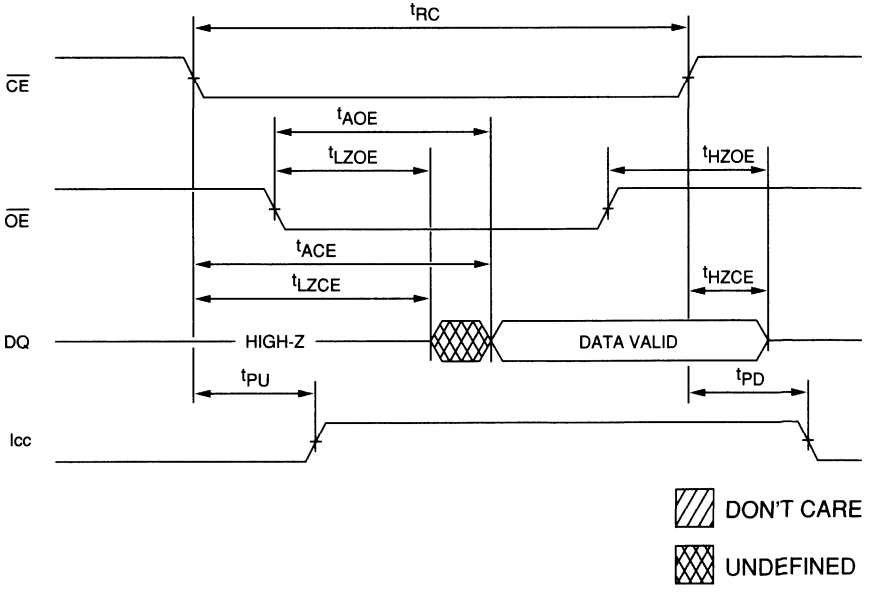
LOW Vcc DATA RETENTION WAVEFORM



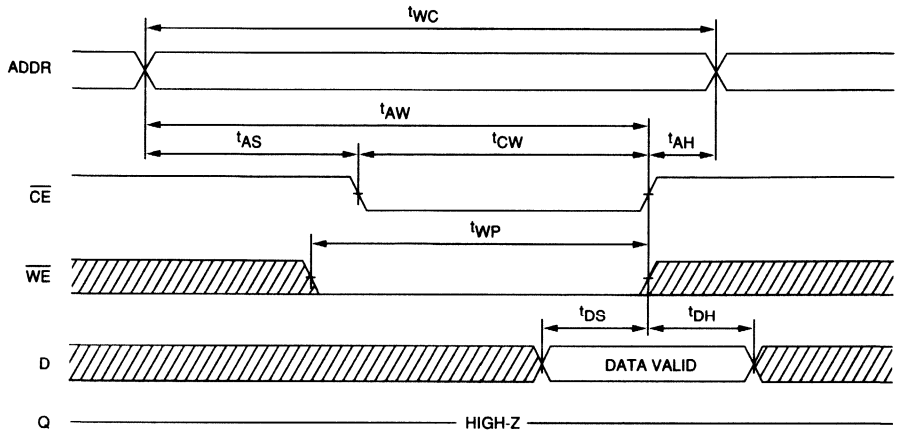
READ CYCLE NO. 1 [8, 9]



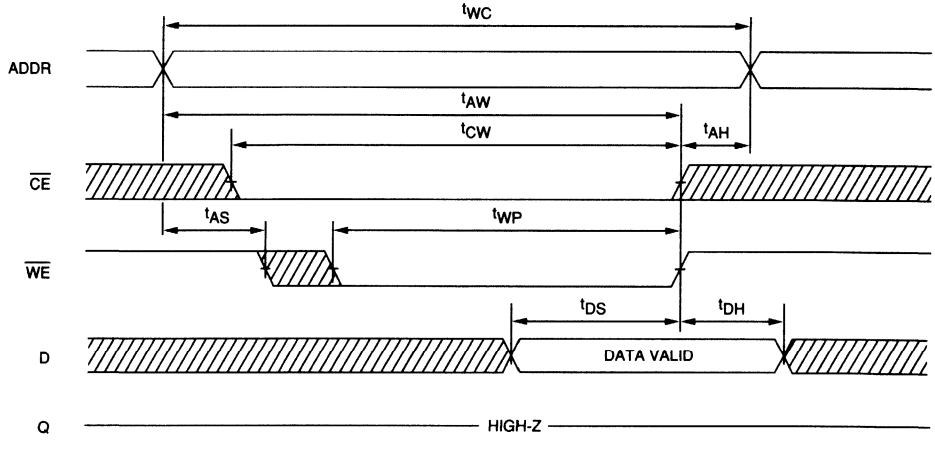
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

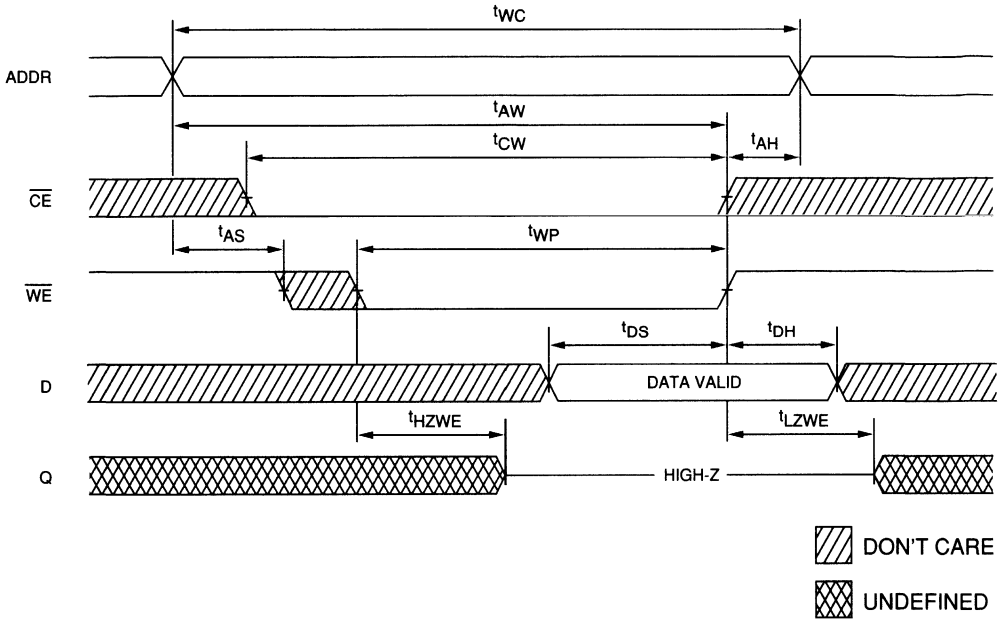


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

128K x 8 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

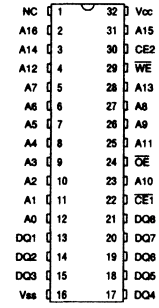
- High speed: 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS — MARKING

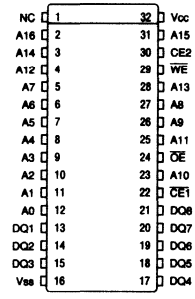
- Timing
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
  - 45ns access — -45
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic DIP (600 mil) — W
  - Plastic SOJ (400 mil) — DJ
- 2V data retention — L
- 2V data retention, low power — LP
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC1008DJ-35 LP IT

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SA-7, SA-8)



32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

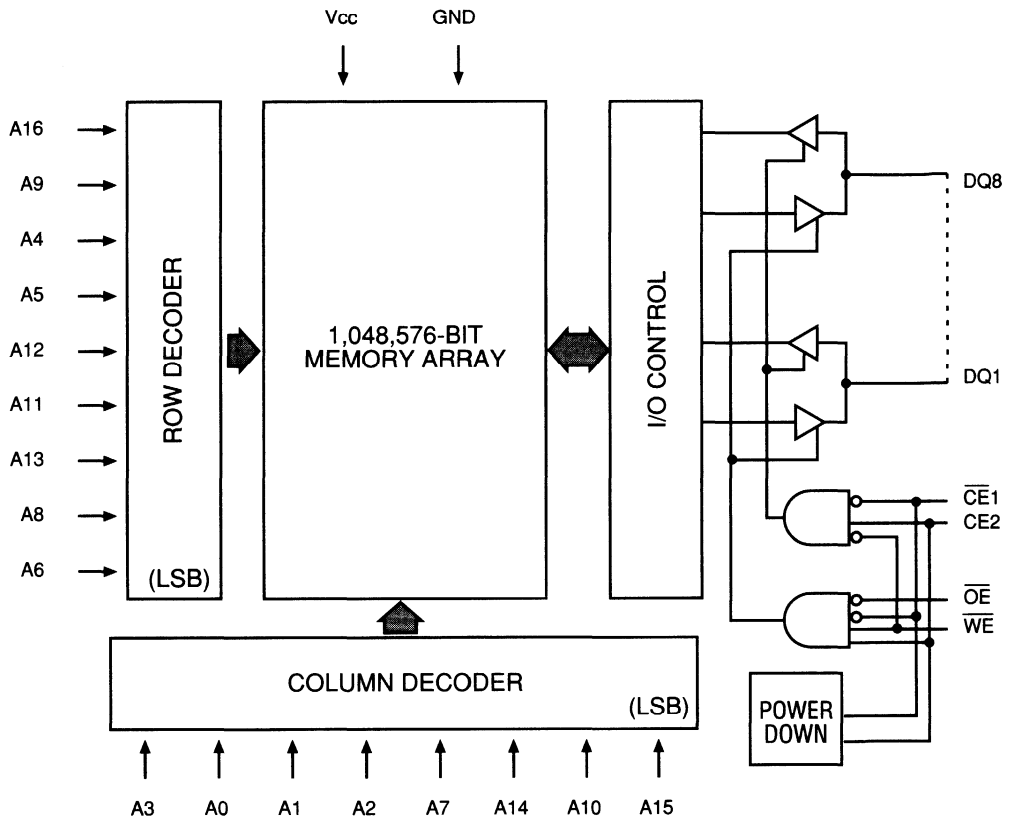
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ goes LOW. The device offers reduced power standby modes when disabled. These modes allow system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a Gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC} + 0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	V_{CC}-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE1}$ ≤ V_{IL} AND CE2 ≥ V_{IH}; Vcc = MAX; Outputs Open f = MAX = 1/t_{RC}	I_{CC}	ALL	65	55	45	40	mA	3, 15, 16
Power Supply Current: Standby	$\overline{CE1}$ ≥ V_{IH} OR CE2 ≤ V_{IL}; Vcc = MAX; Outputs Open f = MAX = 1/t_{RC}	I_{SB1}	STD	14	12	8	6	mA	15, 16, 17
			LP	500	500	500	500	µA	15, 16, 17
	$\overline{CE1}$ ≥ V_{CC} - 0.2V or CE2 ≤ V_{SS} + 0.2V Vcc = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD	300	300	300	300	µA	15, 16, 18
			LP	100	100	100	100	µA	15, 16, 18

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	Vcc = 3.3V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	20		25		35		45		ns	
Address access time	^tAA		20		25		35		45	ns	
Chip Enable access time	^tACE		20		25		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD	20			25		35		45	ns	
Output Enable access time	^tAOE		4		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	20		25		35		45		ns	
Chip Enable to end of write	^tCW	12		15		20		25		ns	
Address valid to end of write	^tAW	12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		25		ns	
WRITE pulse width	$^tWP2$	15		15		20		25		ns	
Data setup time	^tDS	8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

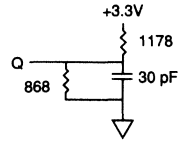


Fig. 1 OUTPUT LOAD EQUIVALENT

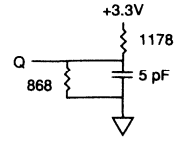


Fig. 2 OUTPUT LOAD EQUIVALENT

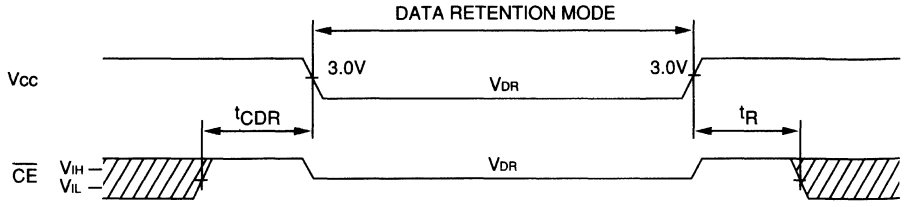
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave form is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
15. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
16. Vcc = MAX.
17. One chip enable must be inactive; the other may be ≥ V_{IH} or ≤ V_{IL}.
18. One chip enable must be inactive; the other may be ≤ Vss +0.2or ≥ Vcc -0.2.

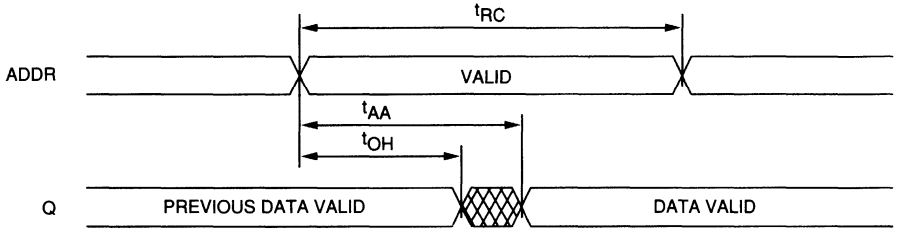
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE1}$ ≥ Vcc -0.2V or CE2 ≤ Vss +0.2V Other Inputs: V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ Vss +0.2V Vcc = 2V	I_{CCDR}		TBD	50	µA	18
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

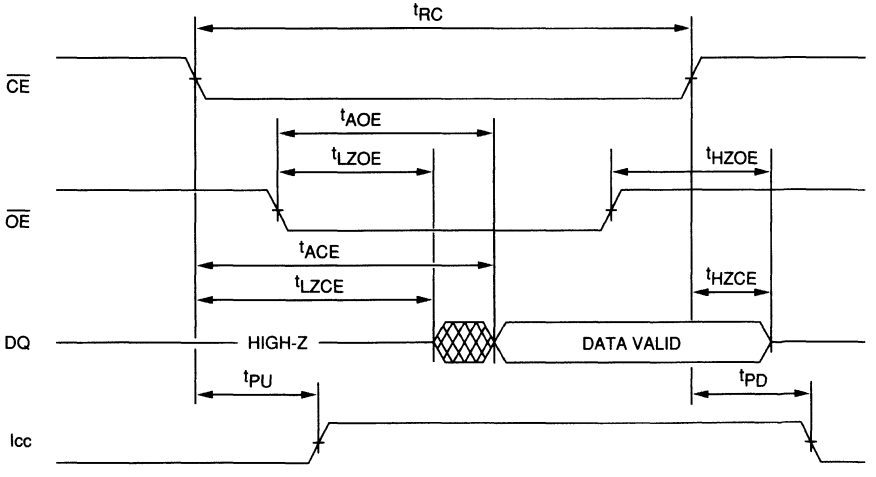
LOW Vcc DATA RETENTION WAVEFORM

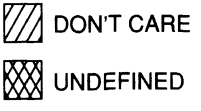


READ CYCLE NO. 1 [8, 9]

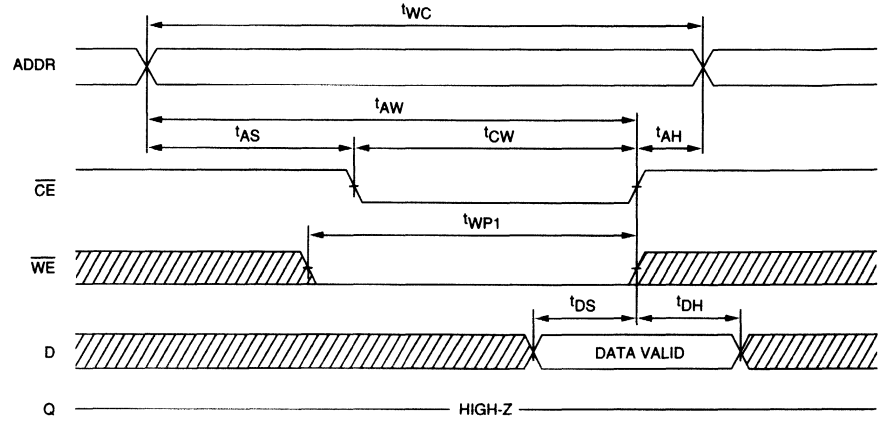


READ CYCLE NO. 2 [7, 8, 10, 12]

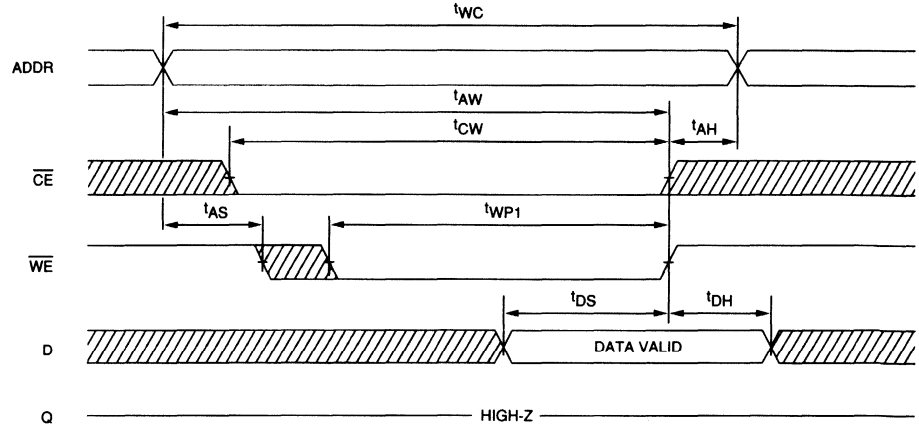




WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



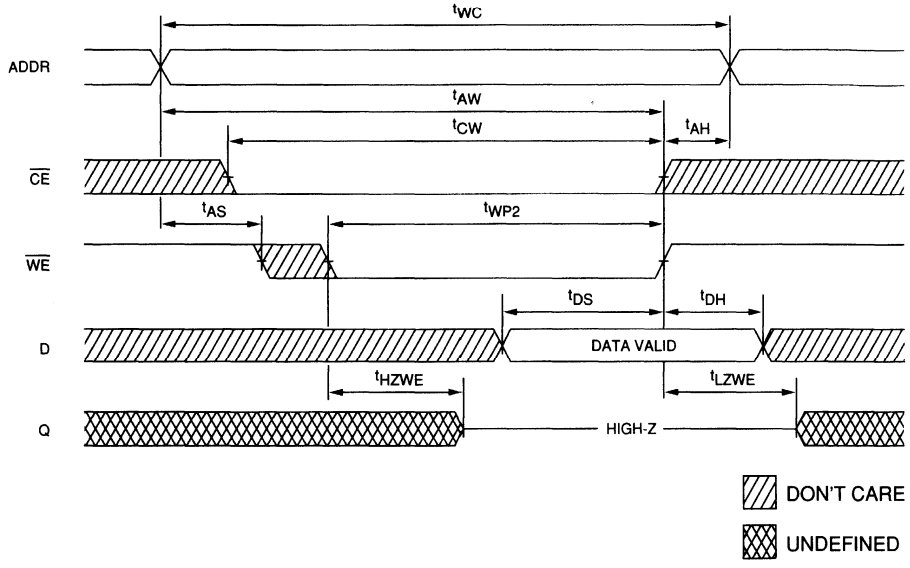
WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

NEW 3.3 VOLT SRAM

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

128K x 8 SRAM

3.3V OPERATION WITH SINGLE CHIP ENABLE

FEATURES

- High speed: 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL compatible
- High-performance, low-power, CMOS double-metal process
- Single 3.3V ±0.3V power supply
- Fast $\overline{OE}$ access times: 10 and 12ns

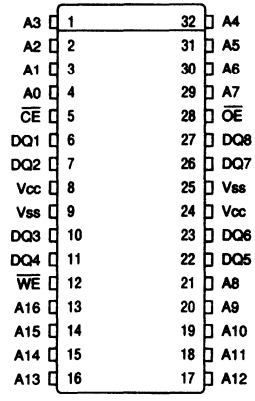
OPTIONS

	MARKING
• Timing	
20ns access	-20
25ns access	-25
• Packages	
32-pin SOJ (400 mil)	DJ
32-pin TSOP (400 mil)	TG

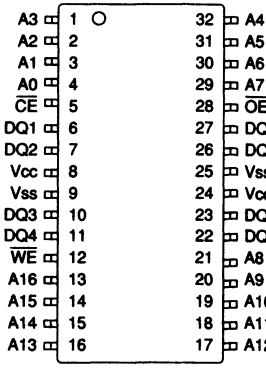
- Part Number Example: MT5LC128K8D4TG-25

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



32-Pin TSOP
(SE-1)



GENERAL DESCRIPTION

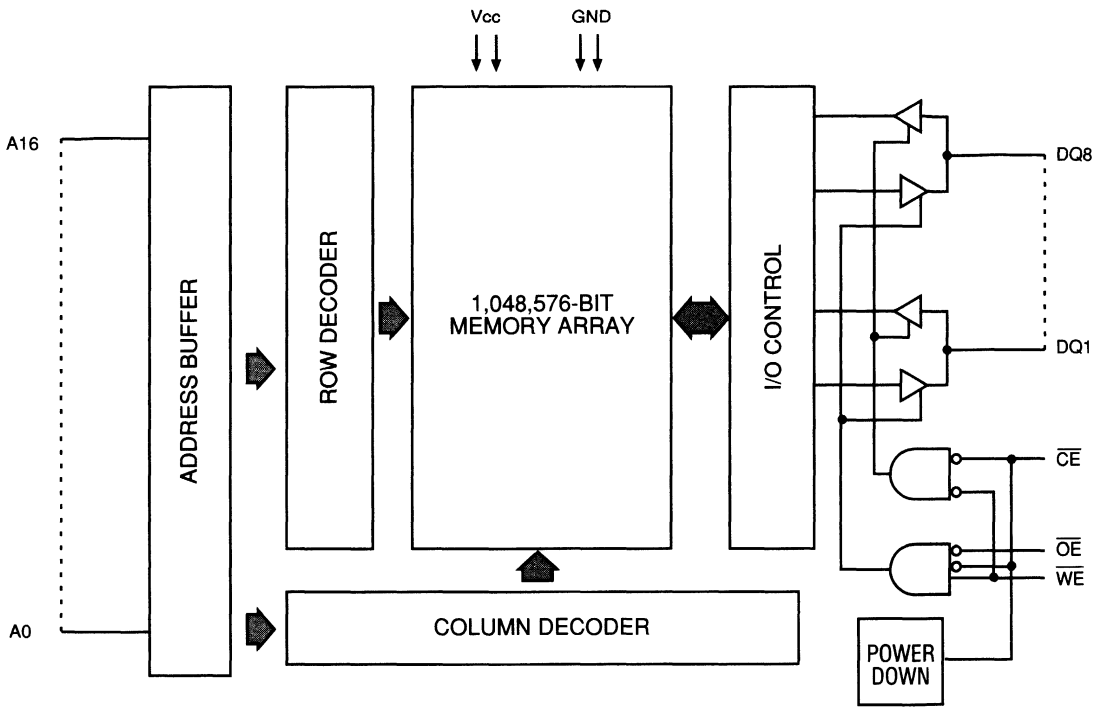
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. This enhancement can place the output in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and chip enable inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 3, 2, 1, 32, 31, 30, 29, 21, 20, 19, 18, 17, 16, 15, 14, 13	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
12	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
5	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
28	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
6, 7, 10, 11, 22, 23, 26, 27	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 3.3V ±0.3V
9, 25	Vss	Supply	Ground: GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC} + 0.5V (4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} =3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC} +0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	V_{CC} - 0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX			
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	60	88	80	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	10	16	14	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ Vss +0.2V V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} =3.3V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25			
	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle							
READ cycle time	^tRC	20		25		ns	
Address access time	^tAA		20		25	ns	
Chip Enable access time	^tACE		20		25	ns	
Output hold from address change	^tOH	5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		ns	
Chip disable to power-down time	^tPD		20		25	ns	
Output Enable access time	^tAOE		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		ns	
Output disable to output in High-Z	^tHZOE		8		8	ns	6
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	
Chip Enable to end of write	^tCW	13		15		ns	
Address valid to end of write	^tAW	12		14		ns	
Address setup time	^tAS	0		0		ns	
Address hold from end of write	^tAH	0		0		ns	
WRITE pulse width	^tWP	10		12		ns	
Data setup time	^tDS	10		10		ns	
Data hold time	^tDH	0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		ns	7
Write Enable to output in High-Z	^tHZWE		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

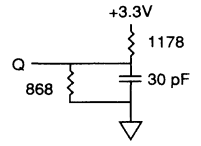


Fig. 1 OUTPUT LOAD EQUIVALENT

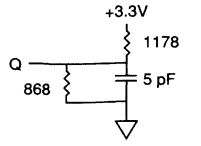
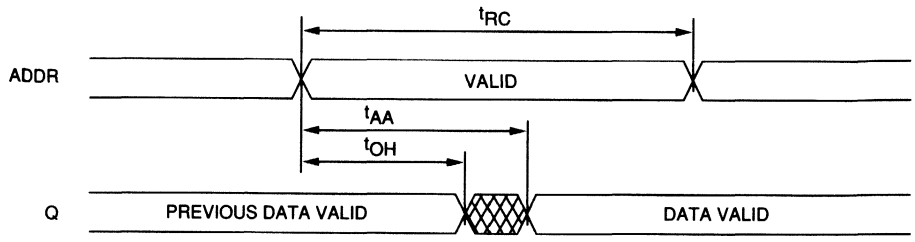


Fig. 2 OUTPUT LOAD EQUIVALENT

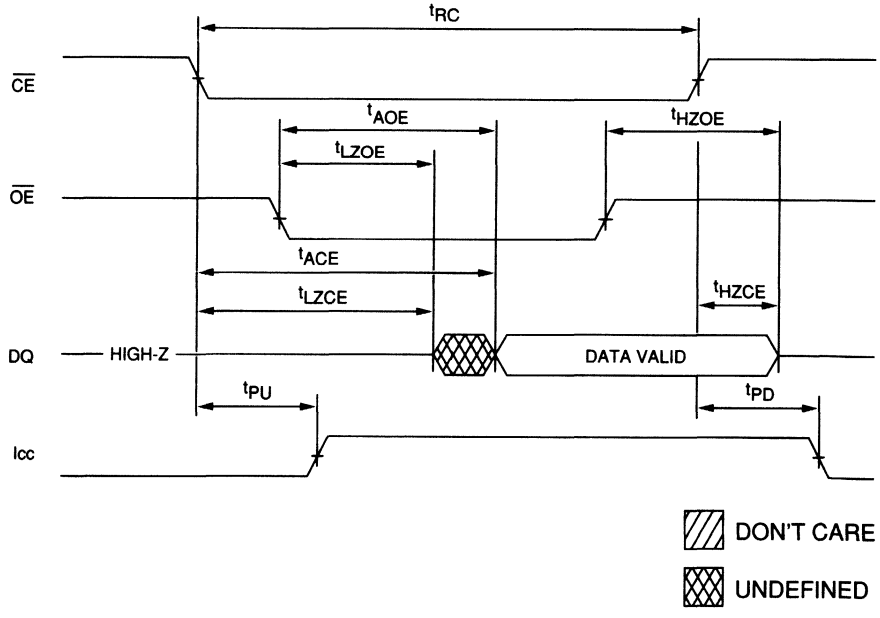
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC /2.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = read cycle time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. The output will be in the High-Z state if output enable is high.

READ CYCLE NO. 1 [8, 9]

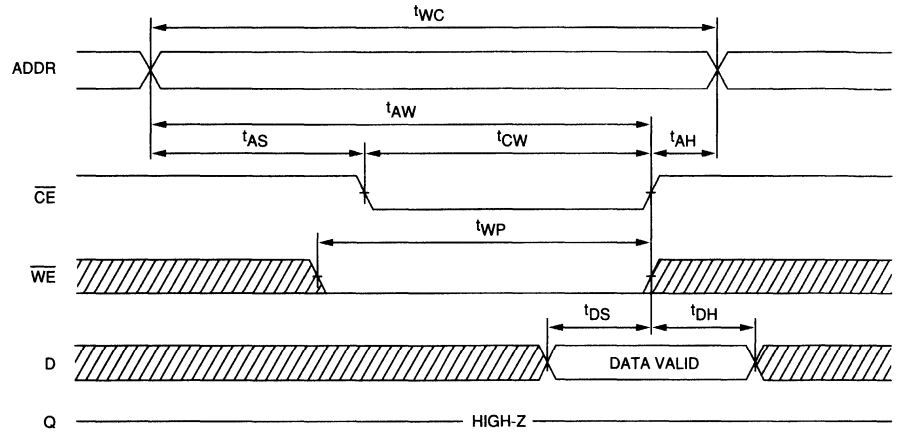


READ CYCLE NO. 2 [7, 8, 10]

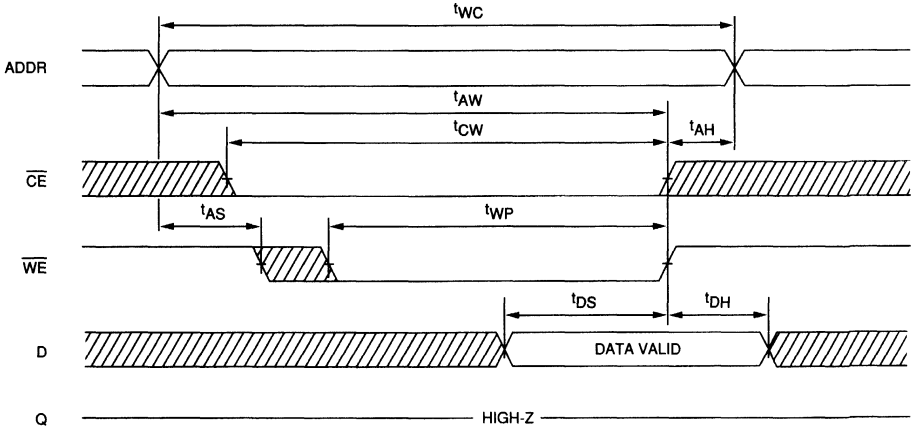


NEW 3.3 VOLT SRAM

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

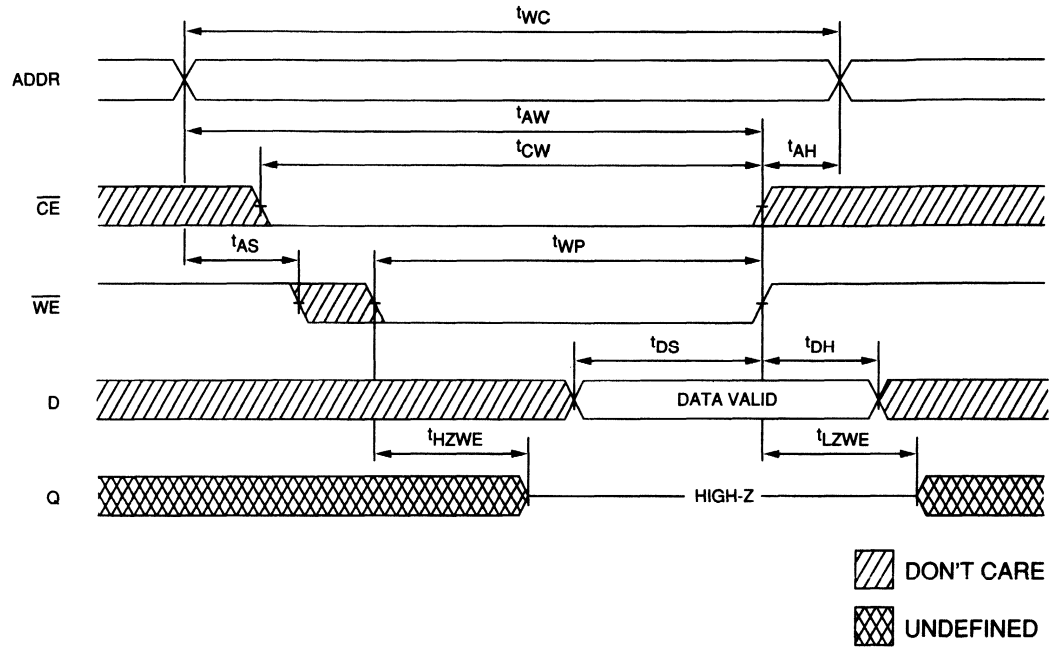


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

512K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, 35 and 55ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3Vpower supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

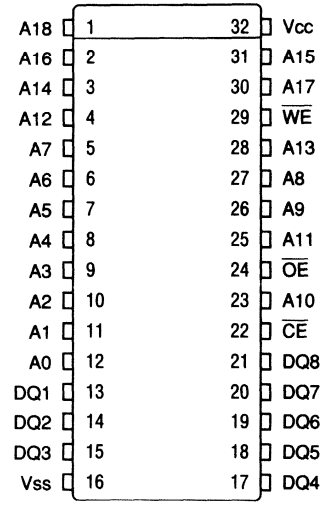
OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
  - 55ns access — -55
- Packages
  - Plastic SOJ (400 mil) — DJ

  NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book.*
- 2V data retention — L
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC512K8C3DJ-25 L IT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

NEW ■ 3.3 VOLT SRAM

SRAM

512K x 8 SRAM

3.3V OPERATION WITH OUTPUT ENABLE

FEATURES

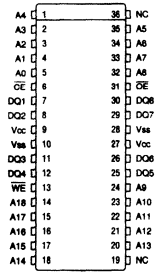
- High speed: 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 6, 8, and 10ns

OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
• 2V data retention	L
• 2V data retention, low power	LP

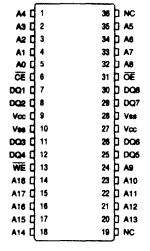
- Part number example: MT5LC512K8D4TG-20LP

PIN ASSIGNMENT (Top View)

36-Pin SOJ
(SD-6)



36-Pin TSOP
(SE-2)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

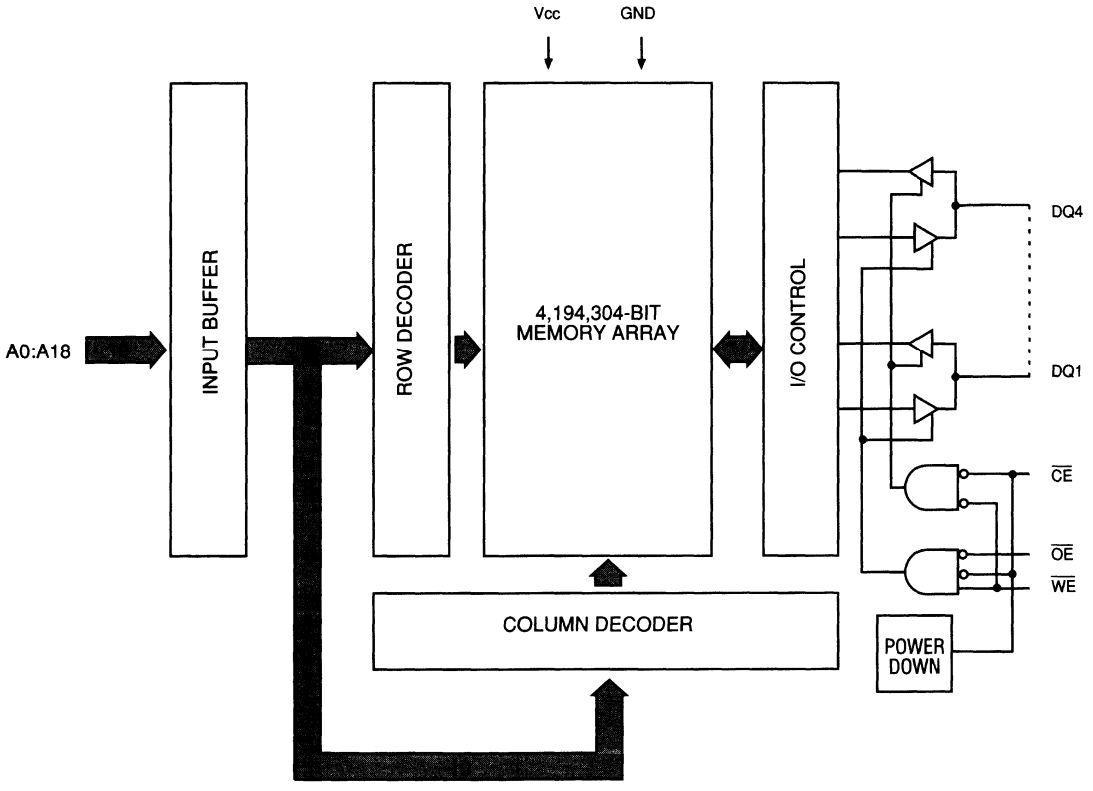
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .....-0.5V to +4.6V
V_{IN}.....-0.5 to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	Vcc-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX				
DESCRIPTION	CONDITIONS	SYMBOL	VER	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs open	Icc	ALL	55	55	50	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs open	I_{SB1}	STD	15	12	10	mA	
			LP	1.0	1.0	1.0	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ V_{SS} +0.2V; f=0	I_{SB2}	STD	300	300	300	µA	
			LP	100	100	100	µA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	5	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		35		ns	
Address access time	^tAA		20		25		35	ns	
Chip Enable access time	^tACE		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		10		12	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		25		35		ns	
Chip Enable to end of write	^tCW	12		15		20		ns	
Address valid to end of write	^tAW	12		15		20		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		ns	
WRITE pulse width	$^tWP2$	15		15		20		ns	
Data setup time	^tDS	8		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

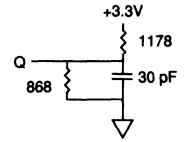


Fig. 1 OUTPUT LOAD EQUIVALENT

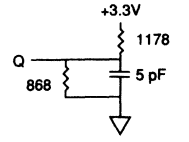


Fig. 2 OUTPUT LOAD EQUIVALENT

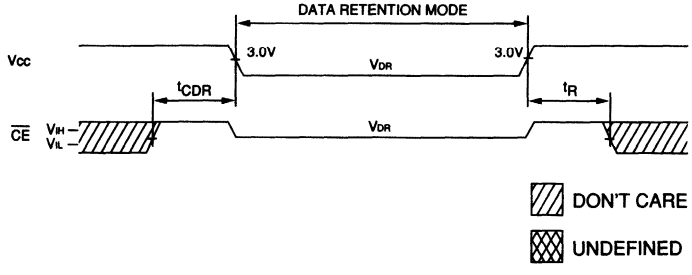
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.

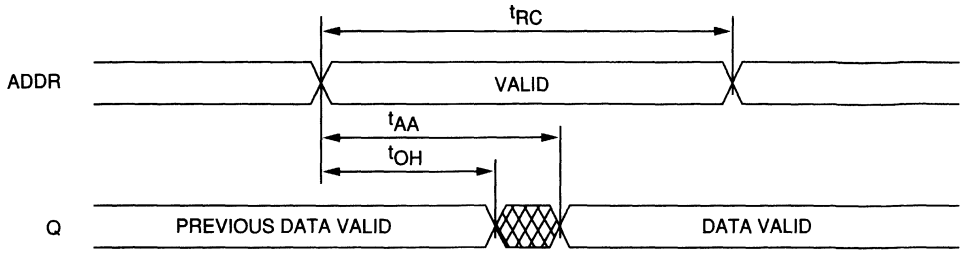
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current	Vcc = 2V $\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	I_{CCDR}		50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0		ns	4
Operation Recovery Time		^{t}R	^{t}RC		ns	4, 11

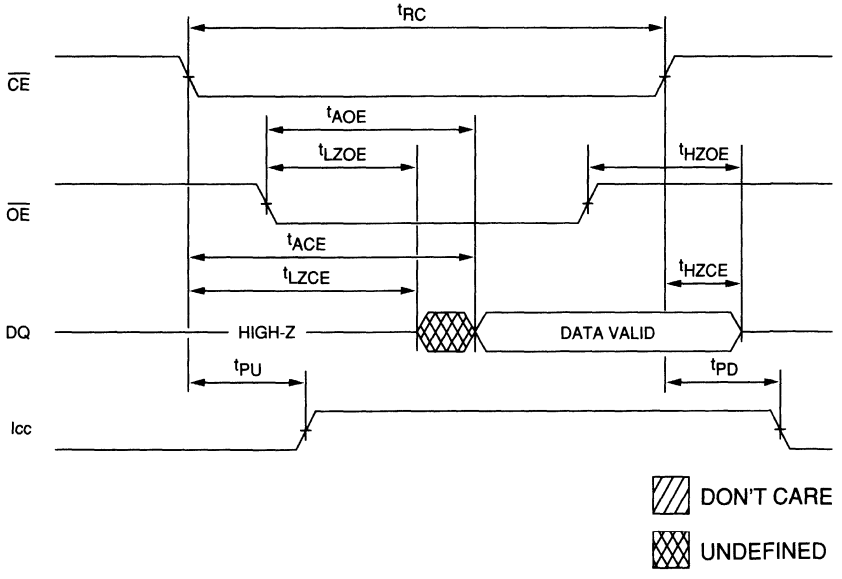
LOW Vcc DATA RETENTION WAVEFORM



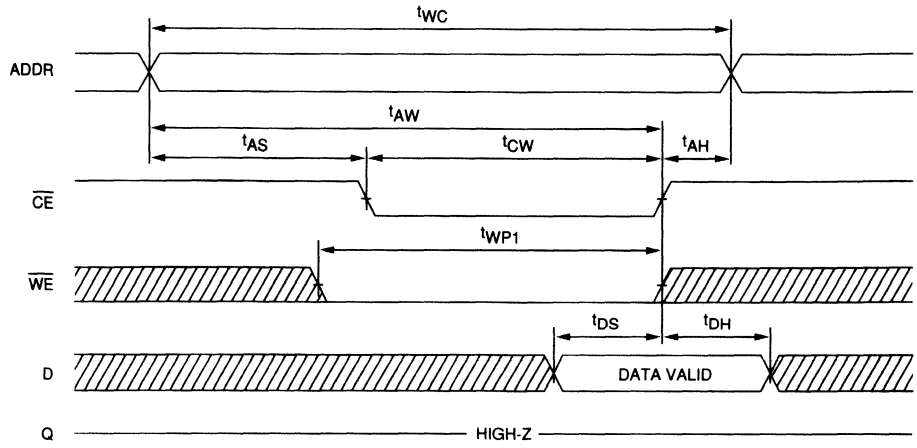
READ CYCLE NO. 1 [8, 9]



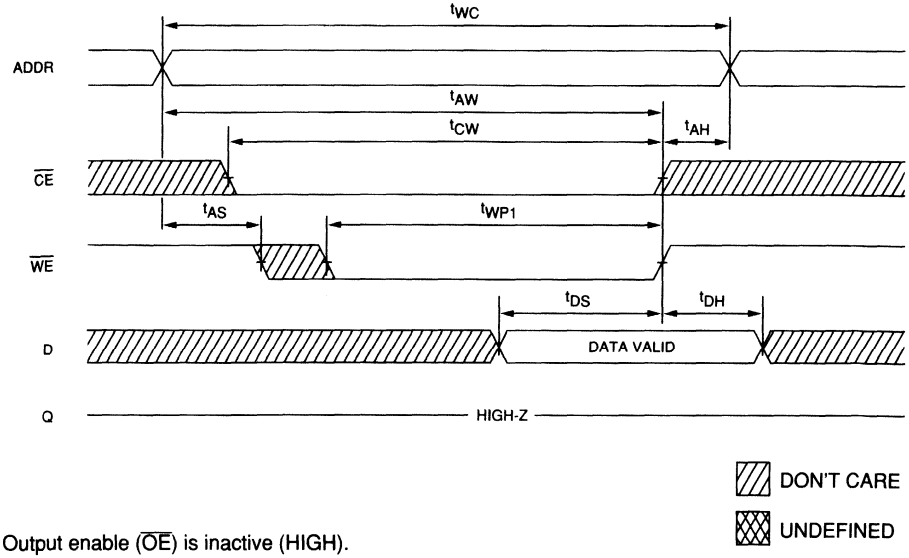
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

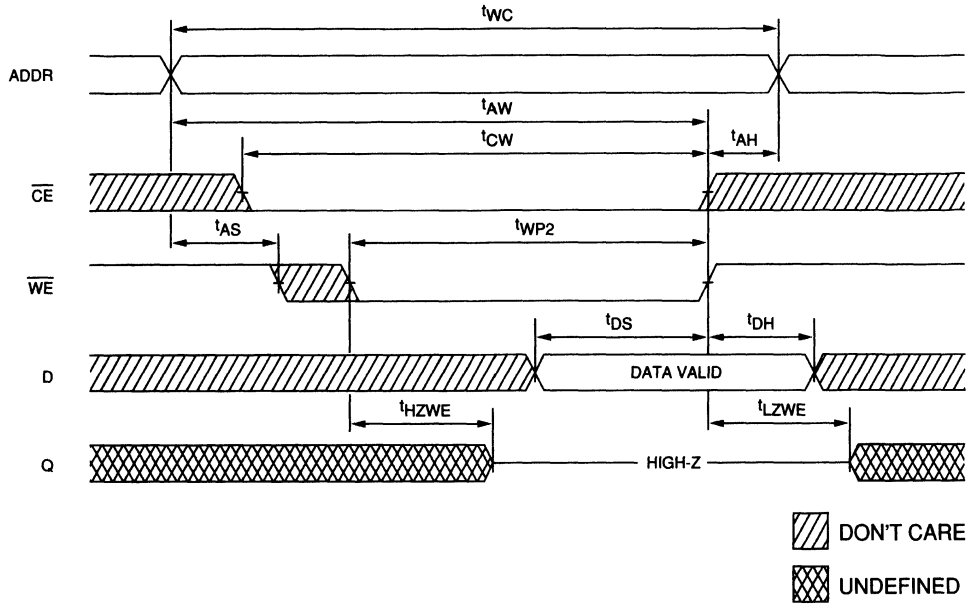


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

NEW 3.3 VOLT SRAM

SRAM

64K x 16 SRAM

3.3V OPERATION WITH OUTPUT ENABLE

FEATURES

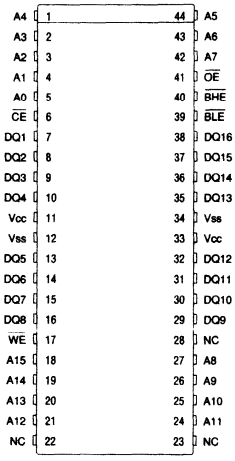
- Fast access times: 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3Vpower supply
- Individual byte controls for both READ and WRITE cycles
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 10 and 12ns

OPTIONS MARKING

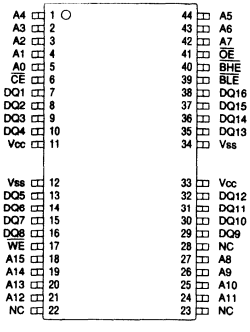
- Timing
  - 20ns access -20
  - 25ns access -25
- Packages
  - 44-pin SOJ (400 mil) DJ
  - 44-pin TSOP (400 mil) TG
- Part Number Example: MT5LC64K16D4TG-25

PIN ASSIGNMENT (Top View)

44-Pin SOJ
(SD-7)



44-Pin TSOP
(SE-3)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

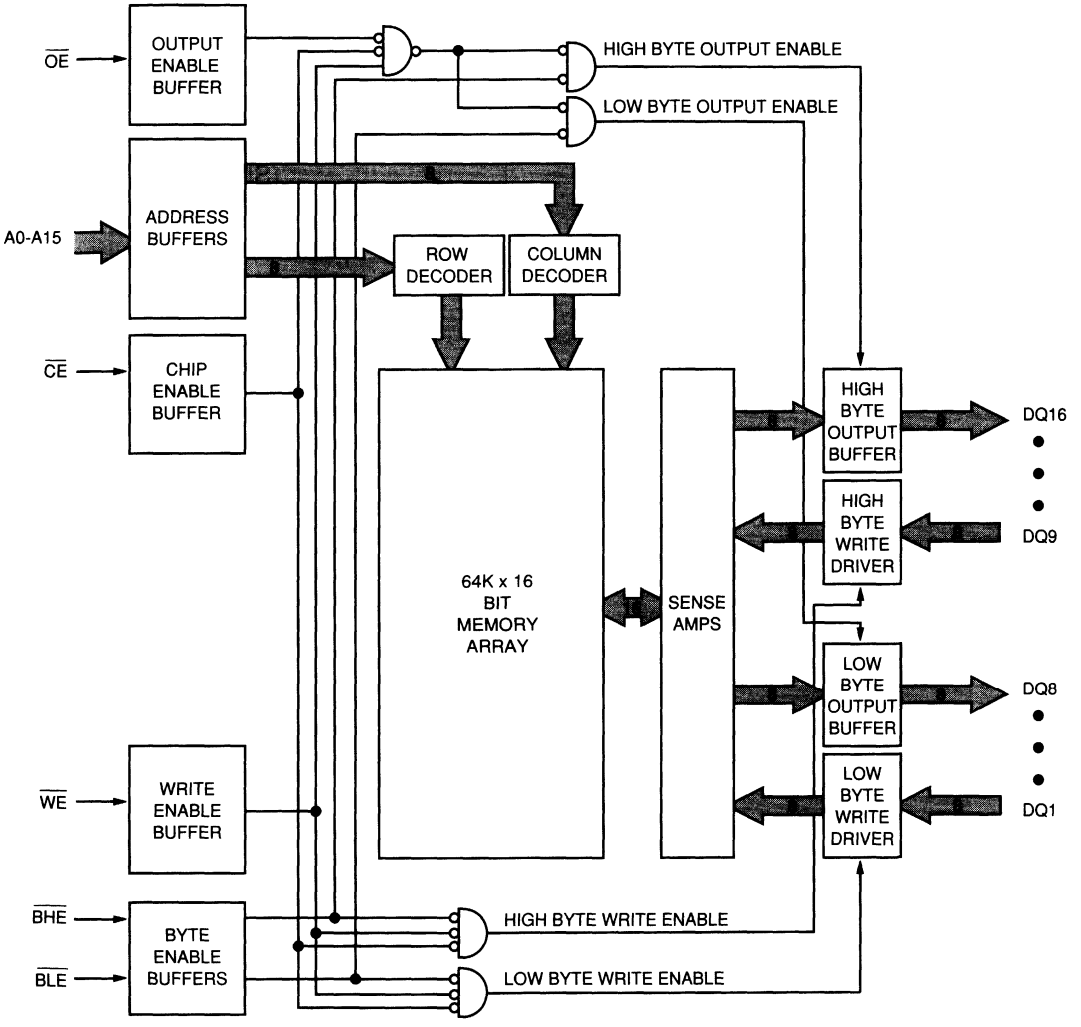
The MT5LC64K16D4 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW chip enable, separate upper and lower byte enables and a fast output enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls DQ1-DQ8, the lower bits. $\overline{BHE}$ controls DQ9-DQ16, the upper bits.

The MT5LC64K16D4 operates from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

NEW
3.3 VOLT SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 1, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19, 18	A0-A15	Input	Address Inputs: These inputs determine which cell is accessed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte, D1-D8. When $\overline{BHE}$ is LOW, data is written or read to the upper byte, D9-D16.
6	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip automatically goes into standby power mode.
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
22, 23, 28	NC	-	No Connect: These signals are not internally connected.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16.
11, 33	Vcc	Supply	Power Supply: +3.3V ±0.3V
12, 34	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH-Z	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to 4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 0.3V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	V_{CC}-0.2		V	1
Output Low Voltage	I_{OL} = 2mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	v	

				MAX			
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	60	88	80	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	10	16	14	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2V V_{CC} = MAX; $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I	6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 3.3V	$C_{I/O}$	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25			
	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle							
READ cycle time	^tRC	20		25		ns	
Address access time	^tAA		20		25	ns	
Chip Enable access time	^tACE		20		25	ns	
Output hold from address change	^tOH	5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		ns	6, 7
Chip disable to output in High-Z	^tHZCE		8		8	ns	6, 7
Output Enable access time	^tAOE		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE		8		8	ns	6, 7
Byte Enable access time	^tABE		10		12	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		ns	6, 7
Byte disable to output in High-Z	^tHZBE		8		8	ns	6, 7
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	
Chip Enable to end of write	^tCW	13		15		ns	
Address valid to end of write	^tAW	12		14		ns	
Address setup time	^tAS	0		0		ns	
Address hold from end of write	^tAH	0		0		ns	
Write pulse width	^tWP	10		12		ns	
Data setup time	^tDS	10		10		ns	
Data hold time	^tDH	0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		ns	6, 7
Write Enable to output in High-Z	^tHZWE		8		8	ns	6, 7
Byte Enable to end of write	^tBW	12		14		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

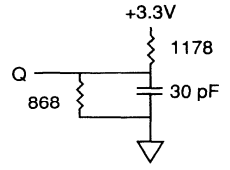


Fig. 1 OUTPUT LOAD EQUIVALENT

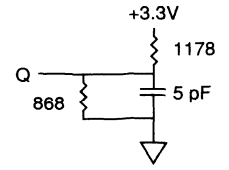
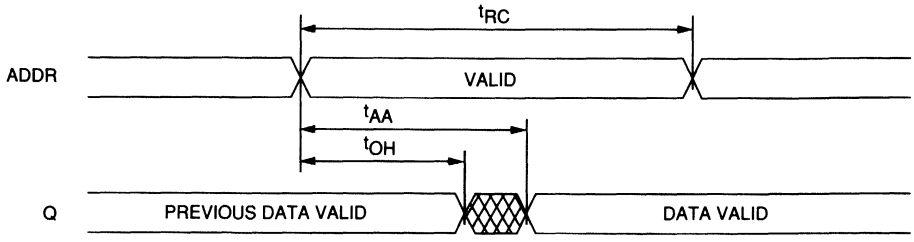


Fig. 2 OUTPUT LOAD EQUIVALENT

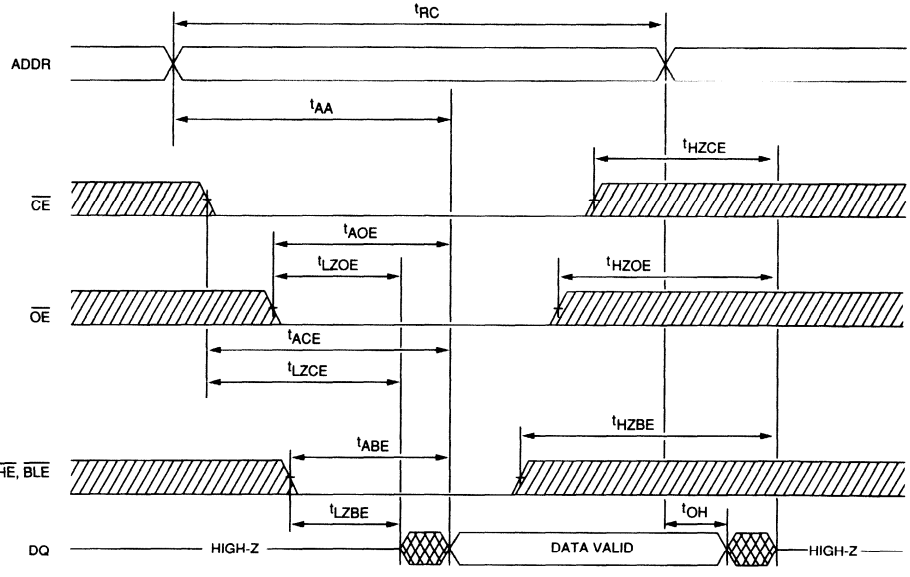
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, $^{t}HZOE$ is less than $^{t}LZOE$, and $^{t}HZBE$ is less than $^{t}LZBE$.
8. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
9. $\overline{WE}$ is HIGH for READ cycle.
10. Device is continuously selected. Chip enable is held in its active state.
11. Address valid prior to, or coincident with, the latest occurring chip enable.
12. $\overline{BHE}$ and $\overline{BLE}$ are held in their active state (LOW).
13. The output will be in the High-Z state if output enable is HIGH.

READ CYCLE NO. 1 [9, 10, 12]

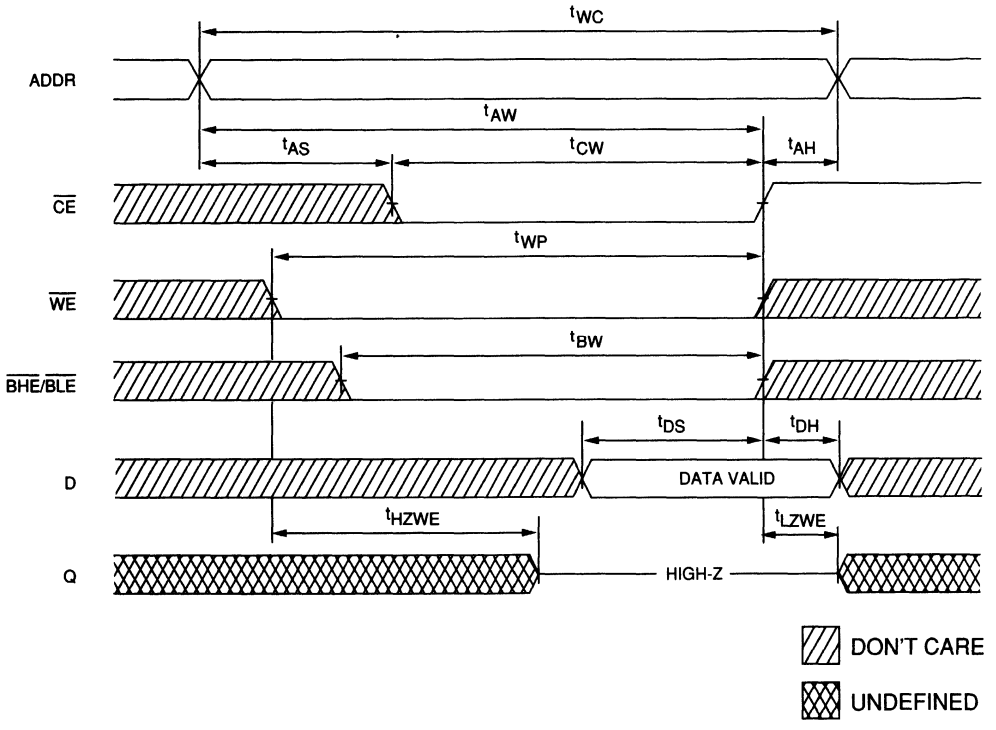


READ CYCLE NO. 2 [7, 9]

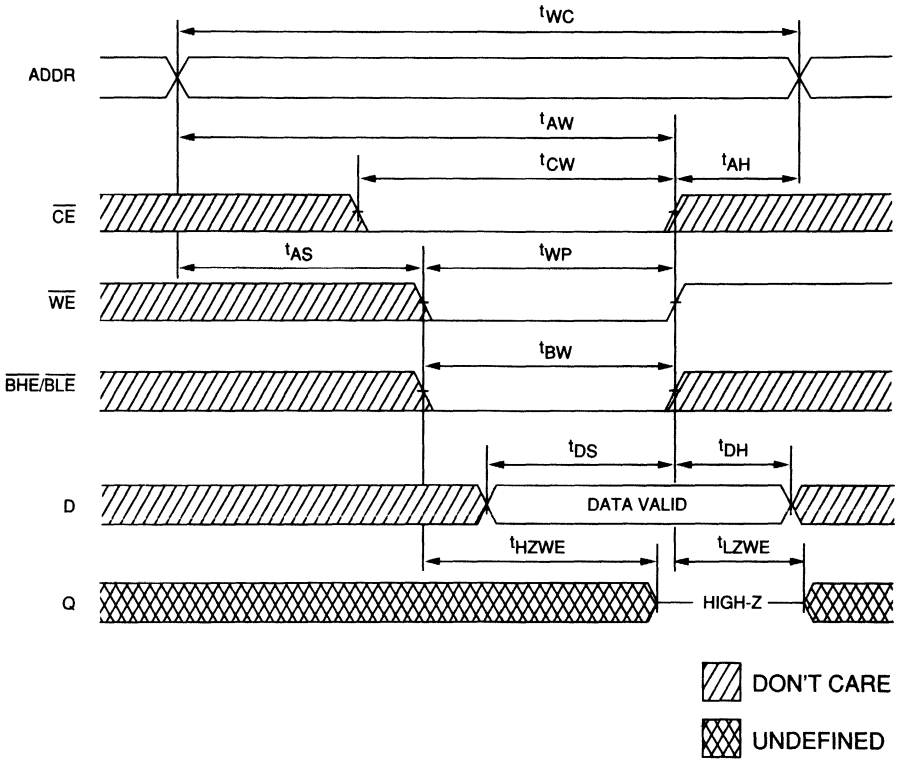


WRITE CYCLE NO. 1 [8, 13]

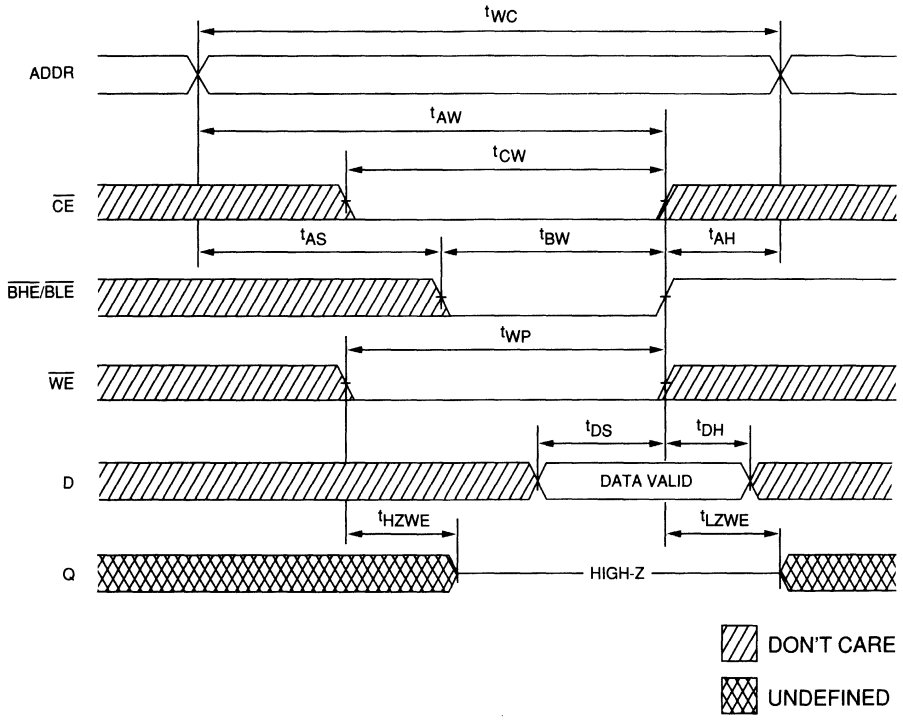
Chip Enable Controlled



WRITE CYCLE NO. 2 [8, 13]
Write Enable Controlled



WRITE CYCLE NO. 3 [8, 13]
Byte Enable Controlled



NEW 3.3 VOLT SRAM

SRAM

256K x 16 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for greater noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Separate upper and lower byte control ($\overline{BHE}$, $\overline{BLE}$)
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 6ns
- Automatic $\overline{CE}$ power down

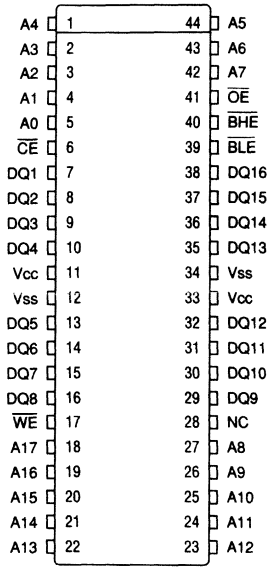
OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ

  NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.
- 2V data retention — L
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC256K16D4DJ-15 L IT

PIN ASSIGNMENT (Top View)

44-Pin SOJ
(SD-7)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for very high performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The high and low bytes of both the READ and WRITE operations are controlled by $\overline{BHE}$ and $\overline{BLE}$ respectively.

The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

MICRON

5V SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Die	Page
				PLCC	PQFP	SOJ	TSOP		
128K x 9	Synchronous SPARC® Cache SRAM	MT58C1289	16, 20	-	-	32	-	CD1 CD2	3-1
16K x 16	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58C1616	12, 15, 20, 25	52	52	-	-	CD1 CD2	3-11
16K x 18	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58C1618	12, 15, 20, 25	52	52	-	-	CD1	3-21

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

SYNCHRONOUS SRAM

128K x 9 SRAM

FULLY REGISTERED INPUTS AND OUTPUTS

FEATURES

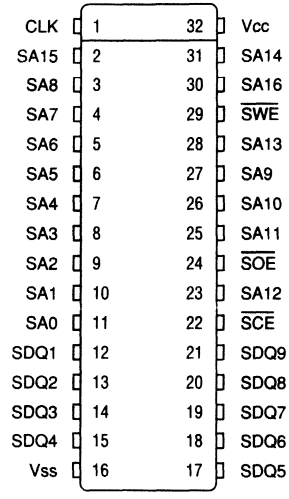
- Timing specific to SPARC® microprocessor
- Fast access times: 16.6 and 20ns
- Fast clock to data valid: 10ns
- Single +5V ±10% power supply
- READ data and WRITE data registers
- Common, TTL-compatible data inputs and outputs
- All inputs and outputs registered with clock
- Fully synchronous, pipelined architecture

OPTIONS / MARKING

- Timing
  - 16.6ns access: -16
  - 20ns access: -20
- Packages
  - 32-pin SOJ (400mil): DJ
- Part Number Example: MT58C1289DJ-16

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

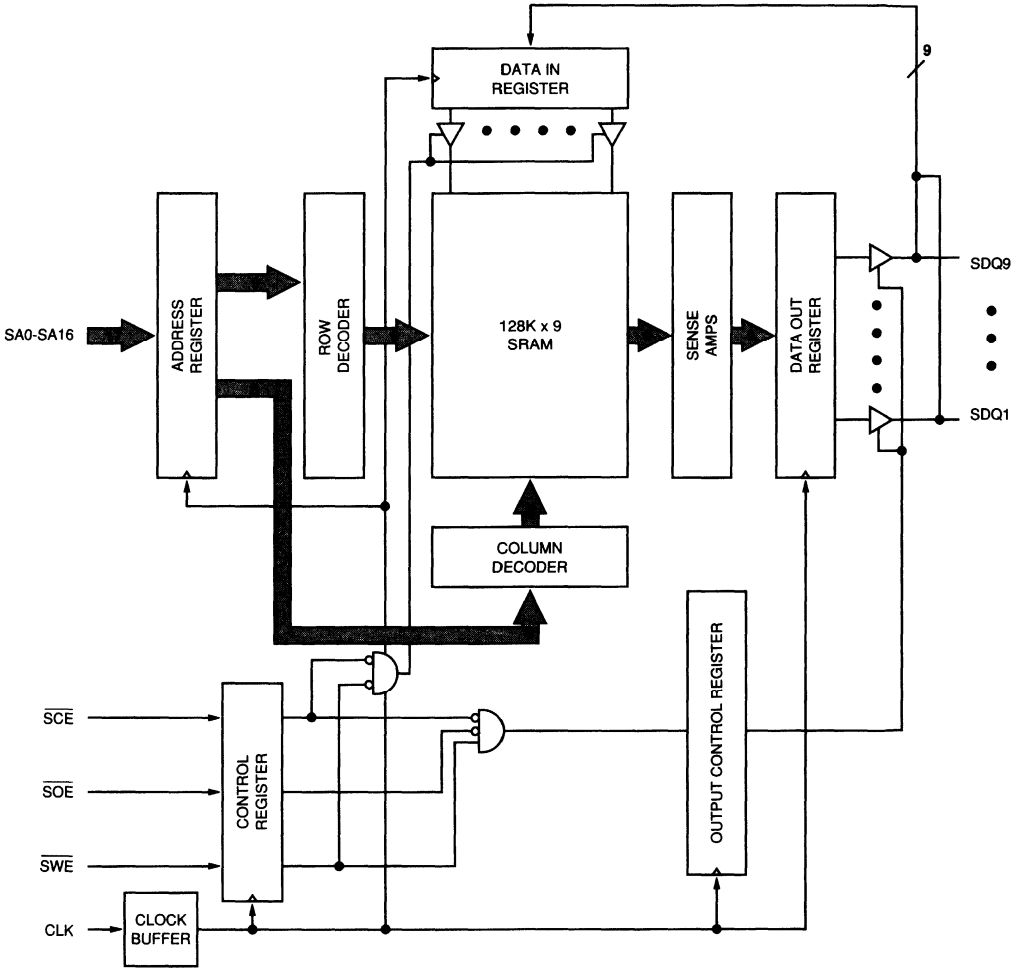
The MT58C1289 is a fully "pipelined" SRAM that integrates registers for address, data in, data out and synchronous chip enable ($\overline{SCE}$), output enable ($\overline{SOE}$) and write enable ($\overline{SWE}$). All registers are triggered with the positive edge of the clock signal (CLK).

READ cycles are performed when $\overline{SWE}$ is HIGH and $\overline{SOE}$ and $\overline{SCE}$ are LOW at the positive edge of CLK. Read data is then presented at the next positive edge of CLK.

WRITE cycles occur when $\overline{SWE}$ and $\overline{SCE}$ are LOW at the rising edge CLK. Data present at the data input registers is written to the SRAM address present at the address input registers on that same rising edge of CLK. The WRITE cycle is internally self-timed, eliminating the need for complex write pulse generation external to the SRAM. The WRITE cycle requires three preceding deselect cycles when a WRITE cycle follows a READ cycle. This allows the D/Q lines to be in the High-Z state when write data is applied. The SRAM is deselected if $\overline{SCE}$ is HIGH when a positive edge of CLK occurs.

The MT58C1289 operates from a +5V power supply.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
11, 10, 9, 8, 7, 6, 5, 4, 3, 27, 26, 25, 23, 28, 31, 2, 30	SA0-SA16	Input	Address Inputs: These inputs are synchronous and must meet the setup and hold times around the positive edge of CLK. The address inputs are clocked into the address register on each positive edge of CLK.
29	$\overline{SWE}$	Input	Synchronous Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{SWE}$ is registered on every positive edge of CLK and must meet the setup and hold times referenced to that edge. WRITE cycles are self-timed internally by the SRAM.
1	CLK	Input	Clock: All timing is controlled by the positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK and must meet the setup and hold times referenced to that edge.
22	$\overline{SCE}$	Input	Synchronous Chip Enable: This signal is used to enable the device. This is a synchronous input and must meet the setup and hold times around CLK. When $\overline{SCE}$ is HIGH, the SRAM automatically goes into the standby power mode.
24	$\overline{SOE}$	Input	Synchronous Output Enable: This active LOW input enables the output drivers. This is a synchronous input and must meet the setup and hold times around CLK.
12, 13, 14, 15, 17, 18, 19, 20, 21	SDQ1-SDQ9	Input/ Output	SRAM Data I/O: For a READ, control signals and address are presented at the rising edge of CLK and data is valid ^{t}KQ after the next rising edge of CLK. Data presented for a WRITE cycle must meet the setup and hold times around CLK.
32	Vcc	Supply	Power Supply: +5V ±10%
16	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	$\overline{SCE}$	$\overline{SWE}$	CLK	$\overline{SOE}$	D	Q NEXT CLOCK	POWER
Deselected	H	X	↑	X	X	High-Z	Standby
READ	L	H	↑	H	X	High-Z	Active
READ	L	H	↑	L	X	Q1-Q9	Active
WRITE	L	L	↑	X	D1-D9	High-Z	Active

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX			
DESCRIPTION	CONDITIONS	SYMBOL	-16	-20	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	70	60	mA	
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX; V_{IL} ≤ V_{SS} +0.2V V_{IH} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-16 MIN	-16 MAX	-20 MIN	-20 MAX	UNITS	NOTES
Clock							
Clock cycle time	tKC	16.6		20		ns	
Clock HIGH time	tKH	5		5		ns	
Clock LOW time	tKL	5		5		ns	
READ Cycle							
READ cycle time	tRC	16.6		20		ns	9
Address setup time	tSAS	3		3		ns	9
Address hold time	tSAH	0.5		1		ns	9
Chip Enable setup time	tSCES	3		3		ns	9
Chip Enable hold time	tSCEH	0.5		1		ns	9
Output Enable setup time	tSOES	3		3		ns	9
Output Enable hold time	tSOEH	0.5		1		ns	9
Write Enable setup time	tSWES	3		3		ns	9
Write Enable hold time	tSWEH	0.5		1		ns	9
Output hold time from clock	tKOH	2		3		ns	
Clock to data valid	tKQ		10		10	ns	
Clock to output High-Z	tKQHZ		8		10	ns	4, 6, 7
Clock to output Low-Z	tKQLZ	0		0		ns	4, 6, 7
WRITE Cycle							
WRITE cycle time	tWC	16.6		20		ns	
Address setup time	tSAS	3		3		ns	9
Address hold time	tSAH	0.5		1		ns	9
Chip Enable setup time	tSCES	3		3		ns	9
Chip Enable hold time	tSCEH	0.5		1		ns	9
Write Enable setup time	tSWES	3		3		ns	9
Write Enable hold time	tSWEH	0.5		1		ns	9
Data setup time	tSDS	3		3		ns	
Data hold time	tSDH	0.5		1		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

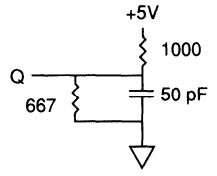


Fig. 1 OUTPUT LOAD EQUIVALENT

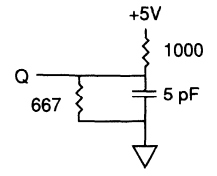
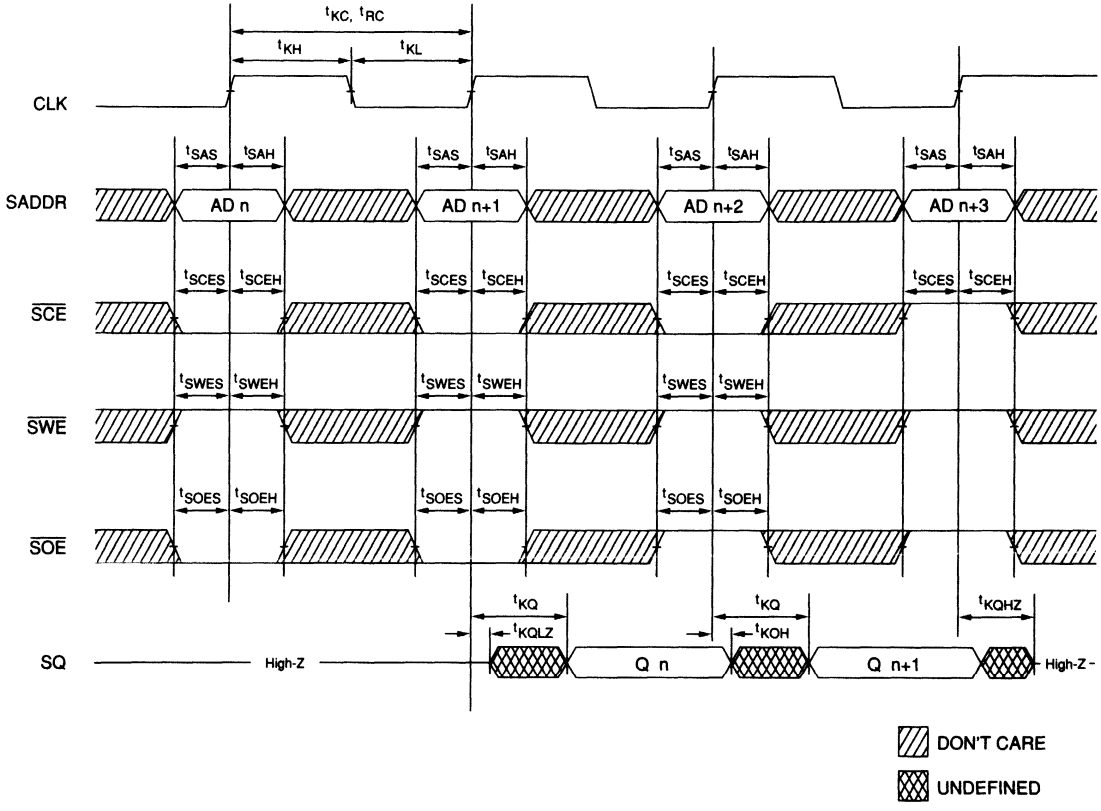


Fig. 2 OUTPUT LOAD EQUIVALENT

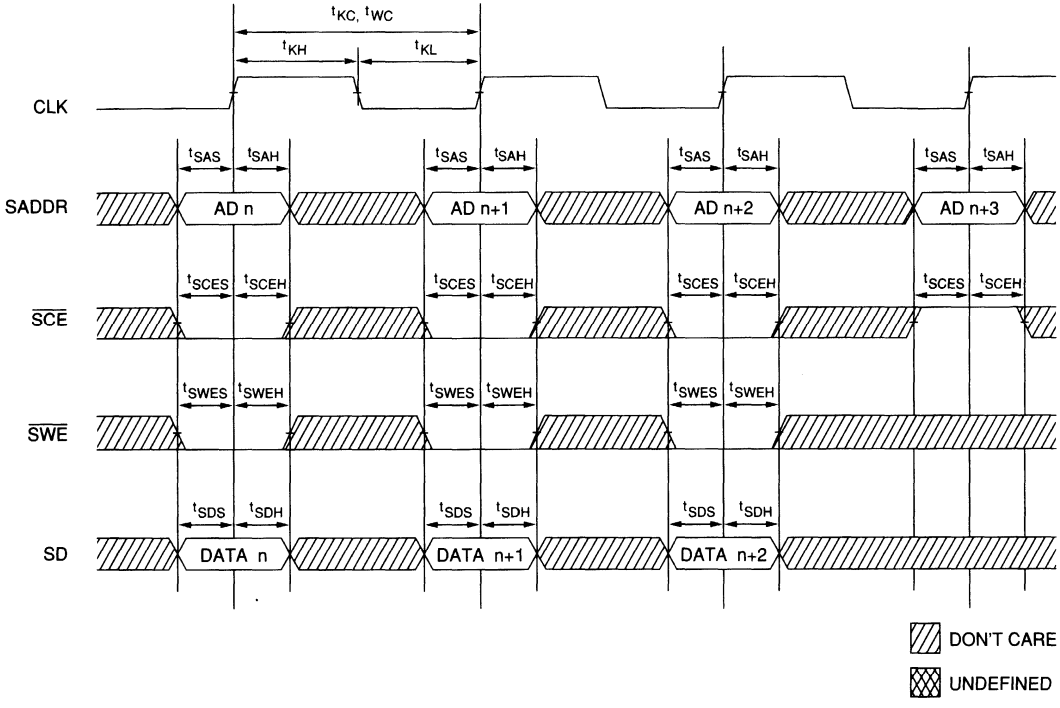
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}KQHZ$ is less than $^{t}KQLZ$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK.

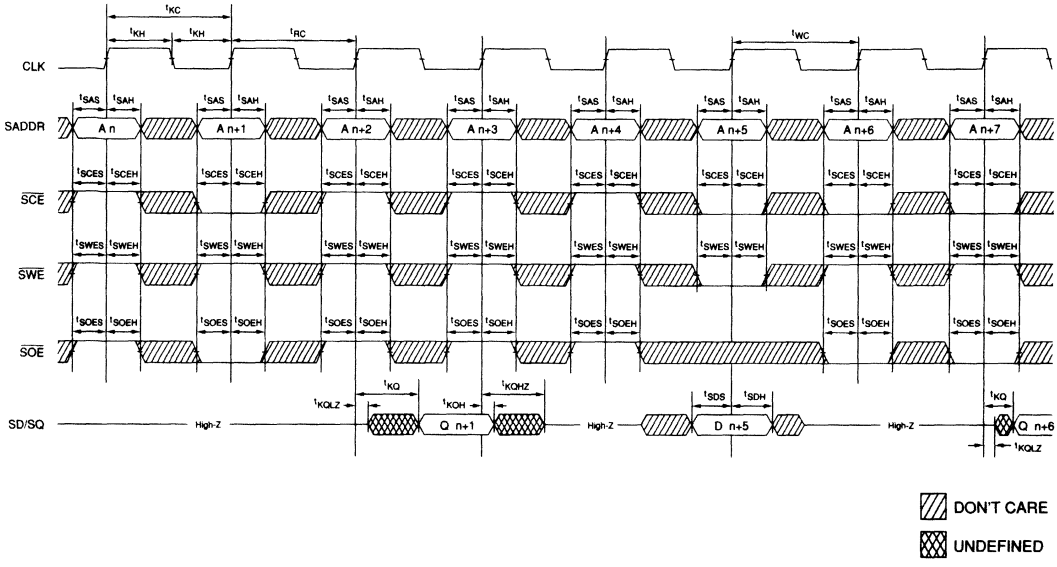
READ TIMING [7, 8, 9]



WRITE TIMING [7, 9]



READ/WRITE TIMING [7, 8, 9]



5 VOLT SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

16K x 16 SRAM

WITH CLOCKED, REGISTERED INPUTS

FEATURES

- Fast access times: 12, 15, 20 and 25ns
- Fast $\overline{OE}$: 5, 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Clock-controlled, registered address, write control and dual $\overline{CE}$s

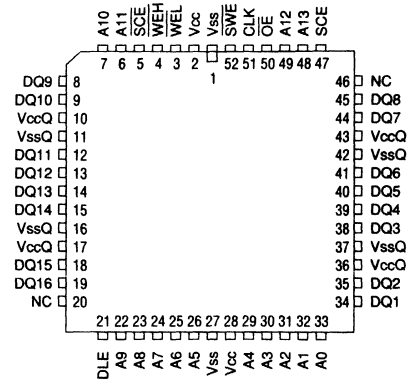
OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

- Part Number Example: MT58C1616LG-12

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

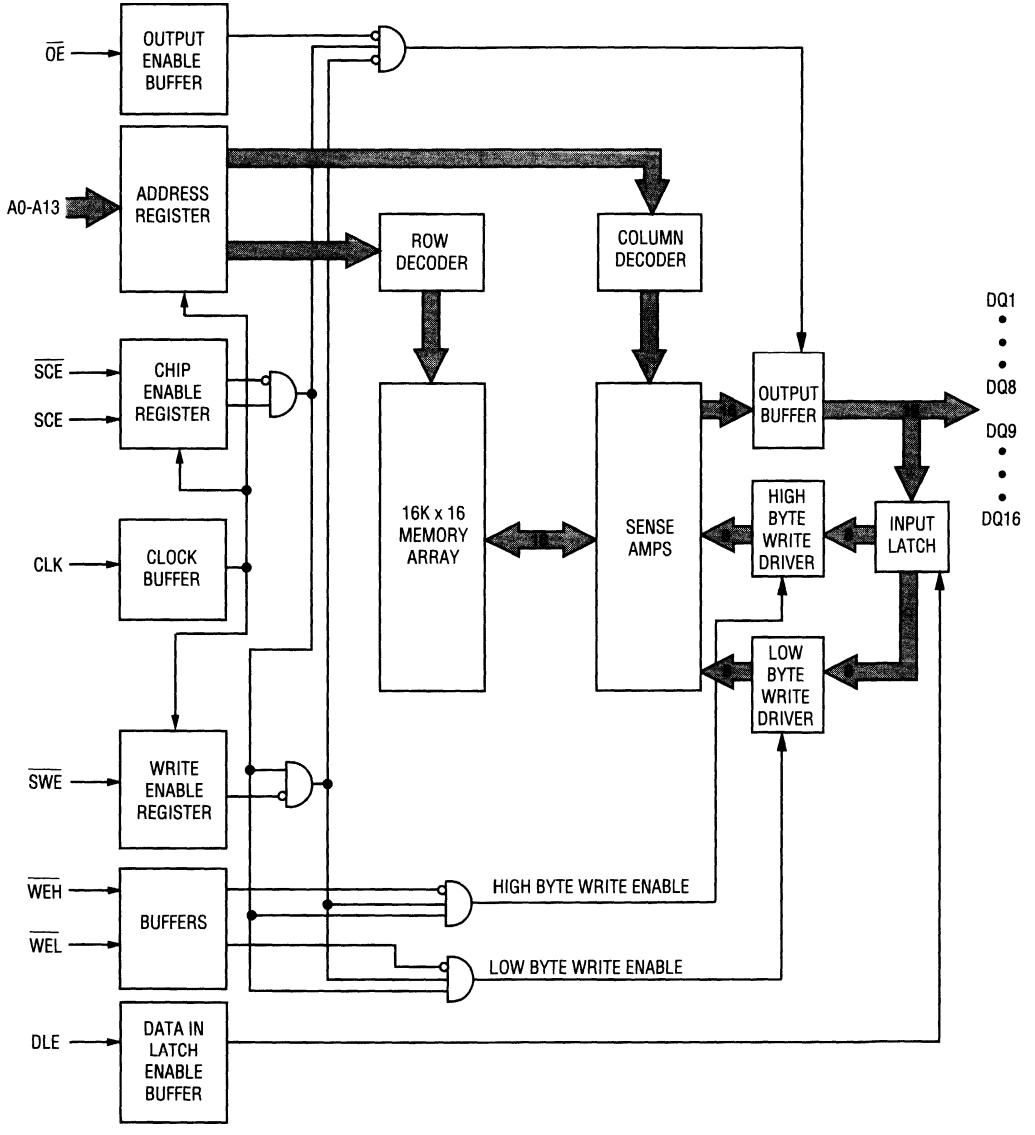
The MT58C1616 SRAM integrates a 16K x 16 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered, single-clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{SCE}$, SCE) and the synchronous write enable ($\overline{SWE}$). Asynchronous inputs include the byte write enables ($\overline{WEL}$, $\overline{WEH}$), output enable ($\overline{OE}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{OE}$ during READ cycles, is asynchronous. The entire data word (DQ1 - DQ16) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and systems that benefit from a wide data bus.

Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 while $\overline{WEH}$ controls DQ9-DQ16. $\overline{WEL}$/$\overline{WEH}$ allow LATE WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{SCE}$) allow on-chip address decoding to be accomplished when the devices are used in a dual-bank mode.

A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present at the inputs is held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58C1616 operates from a single +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{SWE}$	Input	Synchronous Write Enable: This input is a Synchronous Write Enable, and must meet the setup and hold times around the rising edge of CLK. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	CLK	Input	Clock: This signal registers the address, SCE, $\overline{SCE}$ and $\overline{SWE}$ inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
3, 4	$\overline{WEL}$, $\overline{WEH}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{WEL}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{WEH}$ is LOW, data is written to the upper byte, D9-D16. A LATE WRITE cycle can be aborted if both $\overline{WEL}$ and $\overline{WEH}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{SCE}$, SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{SCE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual-bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around CLK if data is latched.
20, 46	NC NC	Input/ Output	These pins are no connects (NCs). NCs are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE while being latched.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{SCE}$	$\overline{SWE}$	$\overline{WEL}$	$\overline{WEH}$	DLE	$\overline{OE}$	DQ
Deselected cycle	L	X	X	X	X	X	X	High-Z
Deselected cycle	X	H	X	X	X	X	X	High-Z
READ	H	L	H	X	X	X	H	High-Z
READ	H	L	H	X	X	X	L	Q1-Q16
WORD WRITE DQ1-DQ16, transparent data-in	H	L	L	L	L	H	X	D1-D16
Word Write DQ1-DQ16, latched data-in	H	L	L	L	L	L	X	D1-D16
ABORTED WRITE	H	L	L	H	H	X	X	High-Z
BYTE WRITE DQ1-DQ8, transparent data-in	H	L	L	L	H	H	X	D1-D8
BYTE WRITE DQ9-DQ16, transparent data-in	H	L	L	H	L	H	X	D9-D16
BYTE WRITE DQ1-DQ8, latched data-in	H	L	L	L	H	L	X	D1-D8
BYTE WRITE DQ9-DQ16, latched data-in	H	L	L	H	L	L	X	D9-D16

NOTE:
1. Registered inputs (addresses, $\overline{SWE}$, SCE and $\overline{SCE}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.
4. This device contains circuitry to ensure that inputs are in High-Z during power-up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -1V to +7V
Voltage on any pin Relative to V_{SS}/V_{SSQ} ..-1V to V_{CC}+1V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE}$ ≤ V_{IL}; SCE ≥ V_{IH}; f = MAX V_{CC} = MAX; Outputs Open	I_{CC}	150	310	280	250	230	mA	3
Power Supply Current: Standby	f = MAX; SCE ≤ V_{IL}; $\overline{SCE}$ ≥ V_{IH} V_{CC} = MAX; Outputs Open	I_{SB1}	50	80	75	70	65	mA	
	$\overline{SCE}$ ≥ V_{CC} -0.2; SCE ≤ V_{SS} +0.2 V_{CC} = MAX; V_{IL} ≤ V_{SS} +0.2 V_{IH} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	15	15	15	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$	9	pF	4

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	Θ_{JA}	60	°C/W	
Thermal resistance – Junction to Case		Θ_{JC}	9	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 5V ±10%)

		-12		-15		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	tKC	12		15		20		25		ns	
Clock HIGH time	tKH	5		5		5		5		ns	
Clock LOW time	tKL	6		6		8		8		ns	
Chip Enable											
SCE/$\overline{SCE}$ setup time	tSCES	3		3		3		3		ns	10
SCE/$\overline{SCE}$ hold time	tSCEH	2		2		2		2		ns	10
Address											
Address setup time	tSAS	3		3		3		3		ns	10
Address hold time	tSAH	2		2		2		2		ns	10
READ Cycle											
READ cycle time	tRC	12		15		20		25		ns	11
Clock to output valid	tKQ		12		15		20		25	ns	
Clock to output invalid	tKQX	4		6		6		6		ns	10
Clock to output in Low-Z (WRITE cycle to READ cycle)	tKQLZ	6		6		6		6		ns	6, 7
Clock to output in Low-Z (Idle cycle to READ cycle)	tKQLZ	2		2		2		2		ns	6, 7
Clock to output in High-Z	tKQHZ	4	8	6	8	6	10	6	12	ns	6, 7
$\overline{SWE}$ setup time	tSWNS	3		3		3		3		ns	10
$\overline{SWE}$ hold time	tSWNH	2		2		2		2		ns	10
$\overline{OE}$ to output valid	tOEQ		5		6		8		10	ns	
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ	0	5	0	6	0	8	0	8	ns	6, 7
WRITE Cycle											
WRITE cycle time	tWC	12		15		20		25		ns	11
$\overline{SWE}$ setup time	tSWES	3		3		3		3		ns	10
$\overline{SWE}$ hold time	tSWEH	2		2		2		2		ns	10
Data setup time	tDS	4		5		6		7		ns	8, 10
Data hold time	tDH	2		2		2		2		ns	8, 10
Data to DLE not setup time	tDLNS	1		1		1		1		ns	9, 10
Data to DLE not hold time	tDLNH	3		3		3		3		ns	9, 10
DLE setup time to end of write (unlatched write)	tDLW	8		8		10		10		ns	
DLE setup time	tDLS	4		6		6		7		ns	9, 10
DLE hold time	tDLH	2		2		2		2		ns	9, 10
$\overline{WEL}$ / $\overline{WEH}$ setup time	tWES	4		6		6		7		ns	10
$\overline{WEL}$ / $\overline{WEH}$ hold time	tWEH	2		2		2		2		ns	10
$\overline{WEL}$ / $\overline{WEH}$ not setup time (aborted WRITE)	tWNS		0		0		0		0	ns	10
$\overline{WEL}$ / $\overline{WEH}$ not hold time (aborted WRITE)	tWNH	2		2		2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

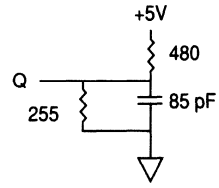


Fig. 1 OUTPUT LOAD EQUIVALENT

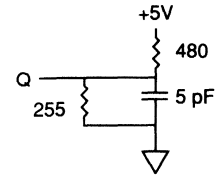
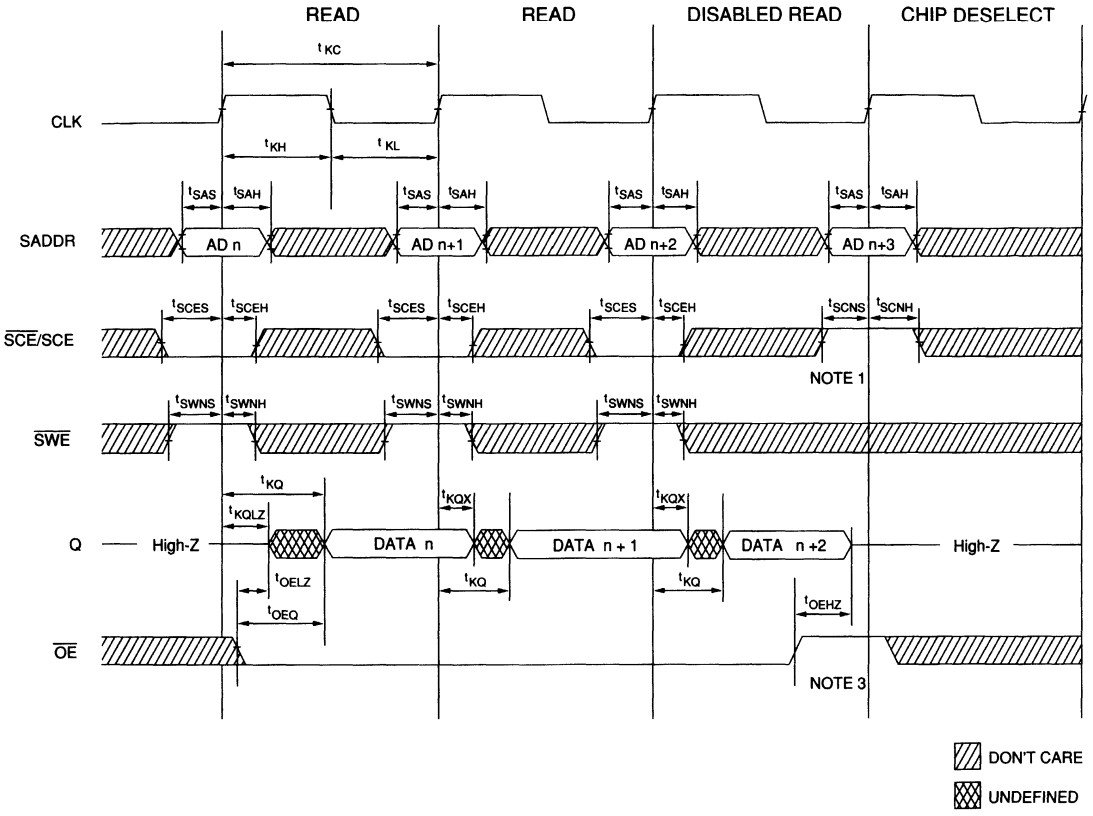


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

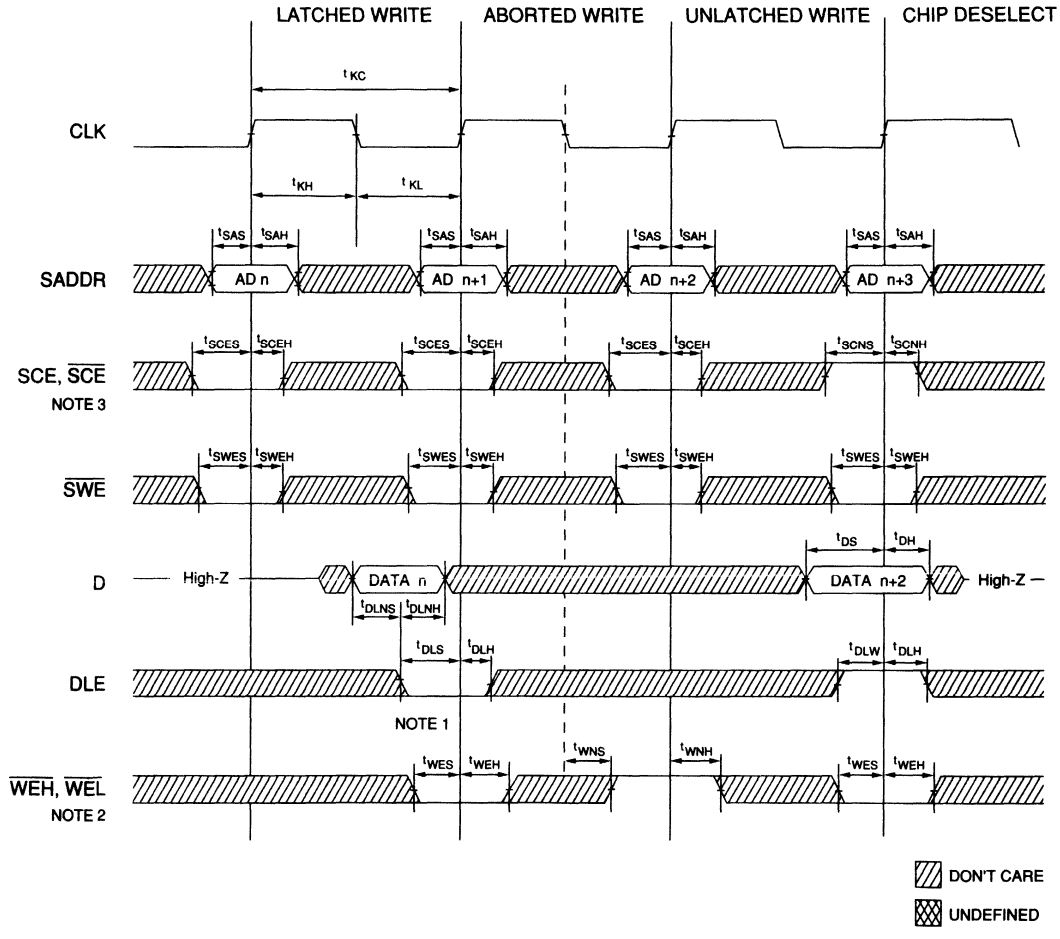
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}KQHZ is less than ^{t}KQLZ and ^{t}OEHZ is less than ^{t}OELZ.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock.
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable and data latch enable.
11. ^{t}RC = ^{t}WC = ^{t}KC

READ TIMING [2]



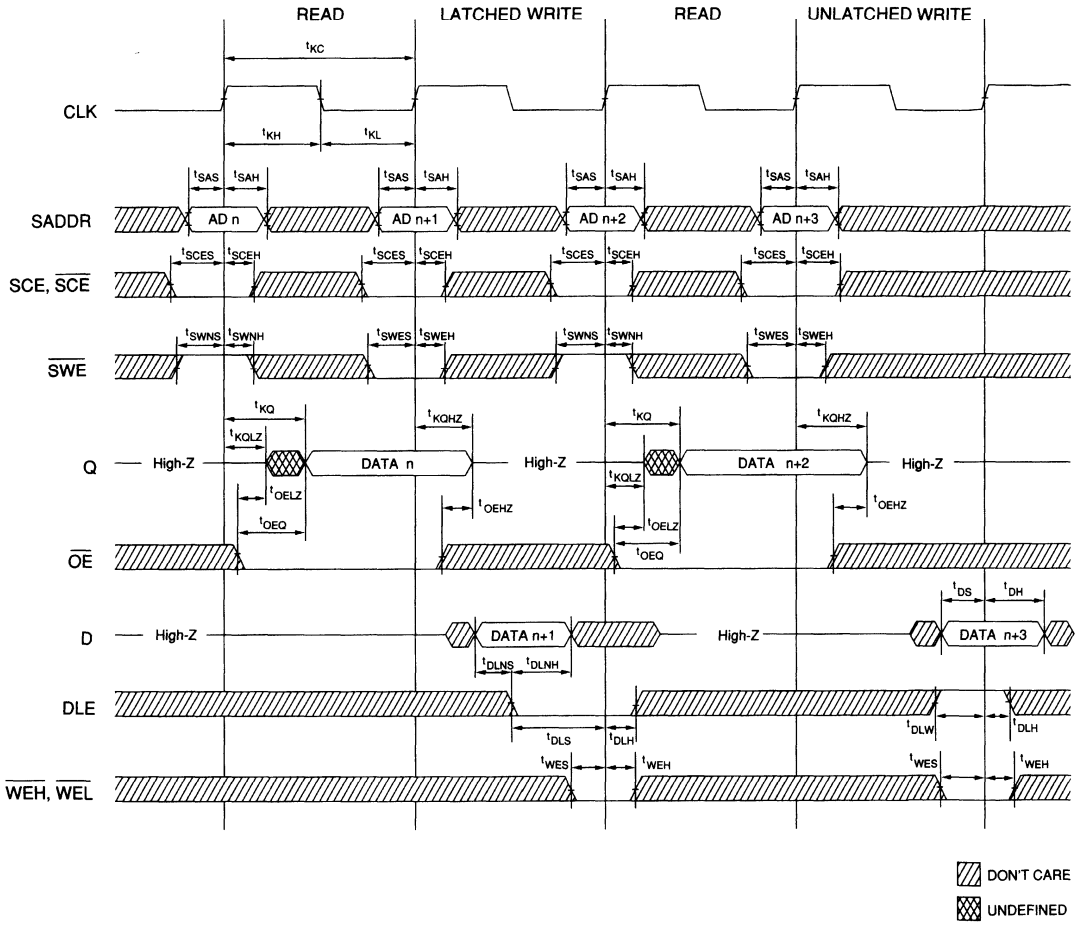
NOTE: 1. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.
2. $\overline{WEL}$ / $\overline{WEH}$ are "don't care" signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{OE}$) is inactive during a READ cycle.

WRITE TIMING



NOTE:
1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{WEH}$, $\overline{WEL}$) are available for use as byte write enables at the system level. They are also available to perform a LATE WRITE cycle abort.
3. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.

READ/WRITE TIMING



SYNCHRONOUS SRAM

16K x 18 SRAM

WITH CLOCKED, REGISTERED INPUTS

FEATURES

- Fast access times: 12, 15, 20 and 25ns
- Fast $\overline{OE}$: 5, 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Parity bits
- Clock-controlled registered address, write control and dual $\overline{CE}$s

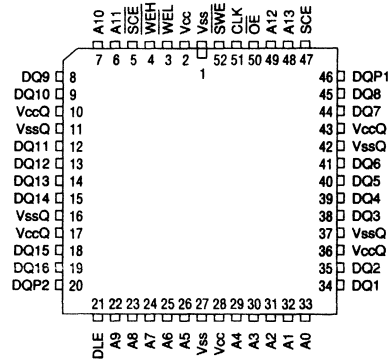
OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

- Part Number Example: MT58C1618LG-12

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

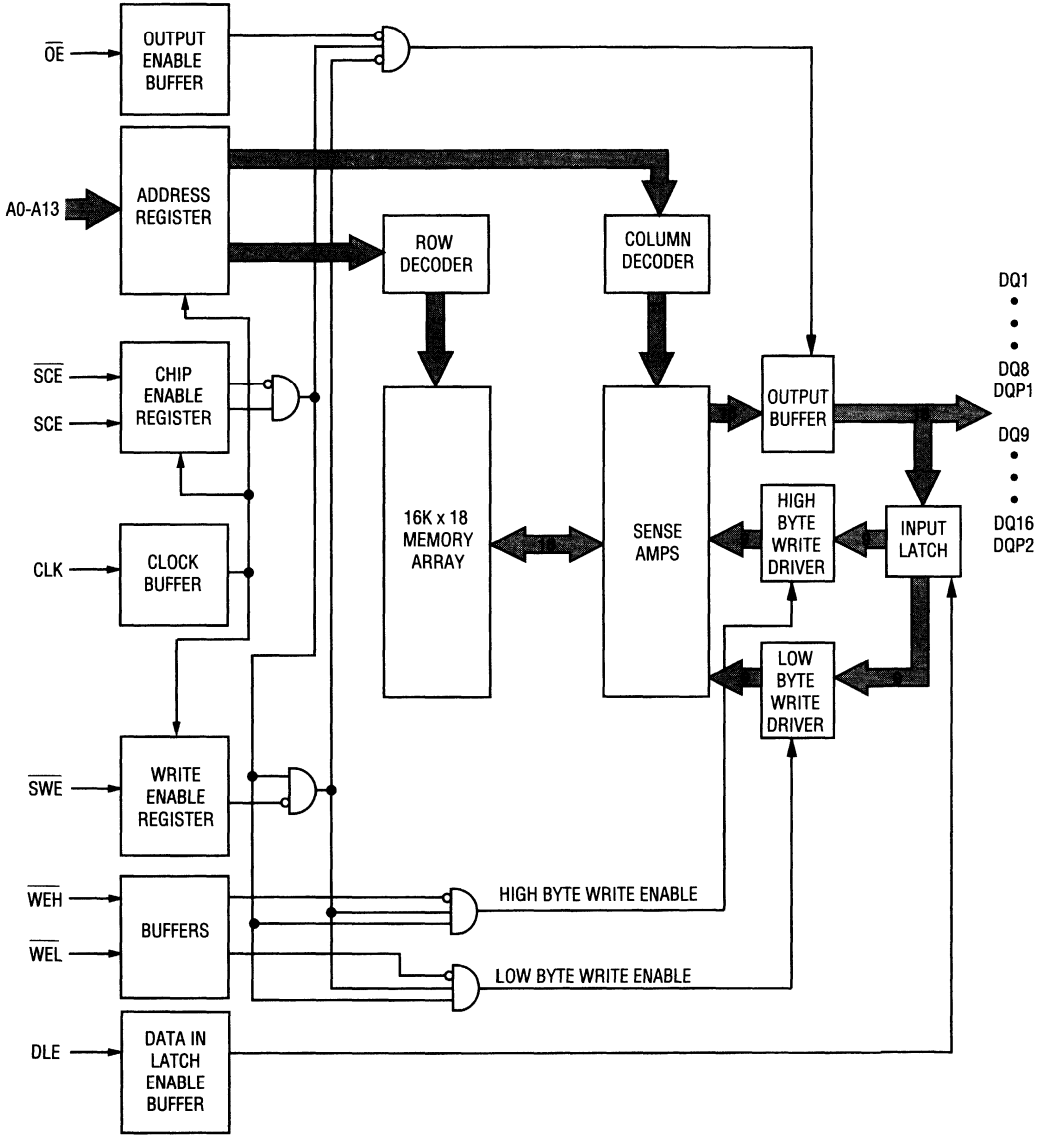
The MT58C1618 SRAM integrates a 16K x 18 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{SCE}$, SCE) and the synchronous write enable ($\overline{SWE}$). Asynchronous inputs include the byte write enables ($\overline{WEL}$, $\overline{WEH}$), output enable ($\overline{OE}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{OE}$ during READ cycles, is asynchronous. The entire data word (DQ1-DQ16, DQP1/2) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and those systems that benefit from a wide data bus.

Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 and DQP1 while $\overline{WEH}$ controls DQ9-DQ16 and DQP2. $\overline{WEL}$/$\overline{WEH}$ allow LATE WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{SCE}$) allow on-chip address decoding to be accomplished when the devices are used in a dual-bank mode.

A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present at the input is held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58C1618 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{SWE}$	Input	Synchronous Write Enable: This input is a synchronous write enable and must meet the setup and hold times around the rising edge of CLK. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	CLK	Input	Clock: This signal latches the address, SCE, $\overline{SCE}$ and $\overline{SWE}$ inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3, 4	$\overline{WEL}$, $\overline{WEH}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{WEL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{WEH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. A LATE WRITE cycle can be aborted if both $\overline{WEL}$ and $\overline{WEH}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{SCE}$, SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{SCE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual-bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around CLK if data is latched.
46, 20	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16. Parity data must meet the setup and hold time around DLE while being latched.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE while being latched.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{SCE}$	$\overline{SWE}$	$\overline{WEL}$	$\overline{WEH}$	DLE	$\overline{OE}$	DQ
Deselected cycle	L	X	X	X	X	X	X	High-Z
Deselected cycle	X	H	X	X	X	X	X	High-Z
READ	H	L	H	X	X	X	H	High-Z
READ	H	L	H	X	X	X	L	Q1-Q16, QP1, QP2
WORD WRITE DQ1-DQ16, DQP1, DQP2, transparent data-in	H	L	L	L	L	H	X	D1-D16, DP1, DP2
WORD WRITE DQ1-DQ16, DQP1, DQP2, latched data-in	H	L	L	L	L	L	X	D1-D16, DP1, DP2
ABORTED WRITE	H	L	L	H	H	X	X	High-Z
BYTE WRITE DQ1-DQ8, DQP1, transparent data-in	H	L	L	L	H	H	X	D1-D8, DP1
BYTE WRITE DQ9-DQ16, DQP2, transparent data-in	H	L	L	H	L	H	X	D9-D16, DP2
BYTE WRITE DQ1-DQ8, DQP1, latched data-in	H	L	L	L	H	L	X	D1-D8, DP1
BYTE WRITE DQ9-DQ16, DQP2, latched data-in	H	L	L	H	L	L	X	D9-D16, DP2

NOTE:
1. Registered inputs (addresses, $\overline{SWE}$, SCE and $\overline{SCE}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -1V to +7V
Voltage on any pin Relative to V_{SS}/V_{SSQ} ..-1V to V_{CC}+1V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE} \le V_{IL}$; $SCE \ge V_{IH}$; f = MAX V_{CC} = MAX; Outputs Open	I_{CC}	150	310	280	250	230	mA	3
Power Supply Current: Standby	f = MAX; $SCE \le V_{IL}$; $\overline{SCE} \ge V_{IH}$ V_{CC} = MAX; Outputs Open	I_{SB1}	50	80	75	70	65	mA	
	$\overline{SCE} \ge V_{CC}$ -0.2; $SCE \le V_{SS}$ +0.2 V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2 $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	15	15	15	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$	9	pF	4

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	ØJA	60	°C/W	
Thermal resistance – Junction to Case		ØJC	9	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = V_{CCQ} = 5V \pm 10\%$)

		-12		-15		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^tKC	12		15		20		25		ns	
Clock HIGH time	^tKH	5		5		5		5		ns	
Clock LOW time	^tKL	6		6		8		8		ns	
Chip Enable											
SCE/$\overline{SCE}$ setup time	^tSCES	3		3		3		3		ns	10
SCE/$\overline{SCE}$ hold time	^tSCEH	2		2		2		2		ns	10
Address											
Address setup time	^tSAS	3		3		3		3		ns	10
Address hold time	^tSAH	2		2		2		2		ns	10
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	11
Clock to output valid	^tKQ		12		15		20		25	ns	
Clock to output invalid	^tKQX	4		6		6		6		ns	10
Clock to output in Low-Z (WRITE cycle to READ cycle)	^tKQLZ	6		6		6		6		ns	6, 7
Clock to output in Low-Z (Idle cycle to READ cycle)	^tKQLZ	2		2		2		2		ns	6, 7
Clock to output in High-Z	^tKQHZ	4	8	6	8	6	10	6	12	ns	6, 7
$\overline{SWE}$ setup time	^tSWNS	3		3		3		3		ns	10
$\overline{SWE}$ hold time	^tSWNH	2		2		2		2		ns	10
$\overline{OE}$ to output valid	^tOEQ		5		6		8		10	ns	
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ	0	5	0	6	0	8	0	8	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	11
$\overline{SWE}$ setup time	^tSWES	3		3		3		3		ns	10
$\overline{SWE}$ hold time	^tSWEH	2		2		2		2		ns	10
Data setup time	^tDS	4		5		6		7		ns	8, 10
Data hold time	^tDH	2		2		2		2		ns	8, 10
Data to DLE not setup time	^tDLNS	1		1		1		1		ns	9, 10
Data to DLE not hold time	^tDLNH	3		3		3		3		ns	9, 10
DLE setup time to end of write (unlatched write)	^tDLW	8		8		10		10		ns	
DLE setup time	^tDLS	4		6		6		7		ns	9, 10
DLE hold time	^tDLH	2		2		2		2		ns	9, 10
$\overline{WEL}$ / $\overline{WEH}$ setup time	^tWES	4		6		6		7		ns	10
$\overline{WEL}$ / $\overline{WEH}$ hold time	^tWEH	2		2		2		2		ns	10
$\overline{WEL}$ / $\overline{WEH}$ not setup time (aborted WRITE)	^tWNS		0		0		0		0	ns	10
$\overline{WEL}$ / $\overline{WEH}$ not hold time (aborted WRITE)	^tWNH	2		2		2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

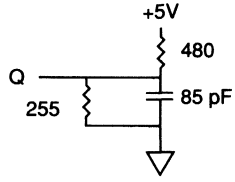


Fig. 1 OUTPUT LOAD EQUIVALENT

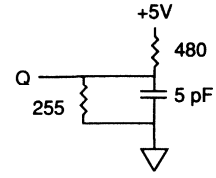
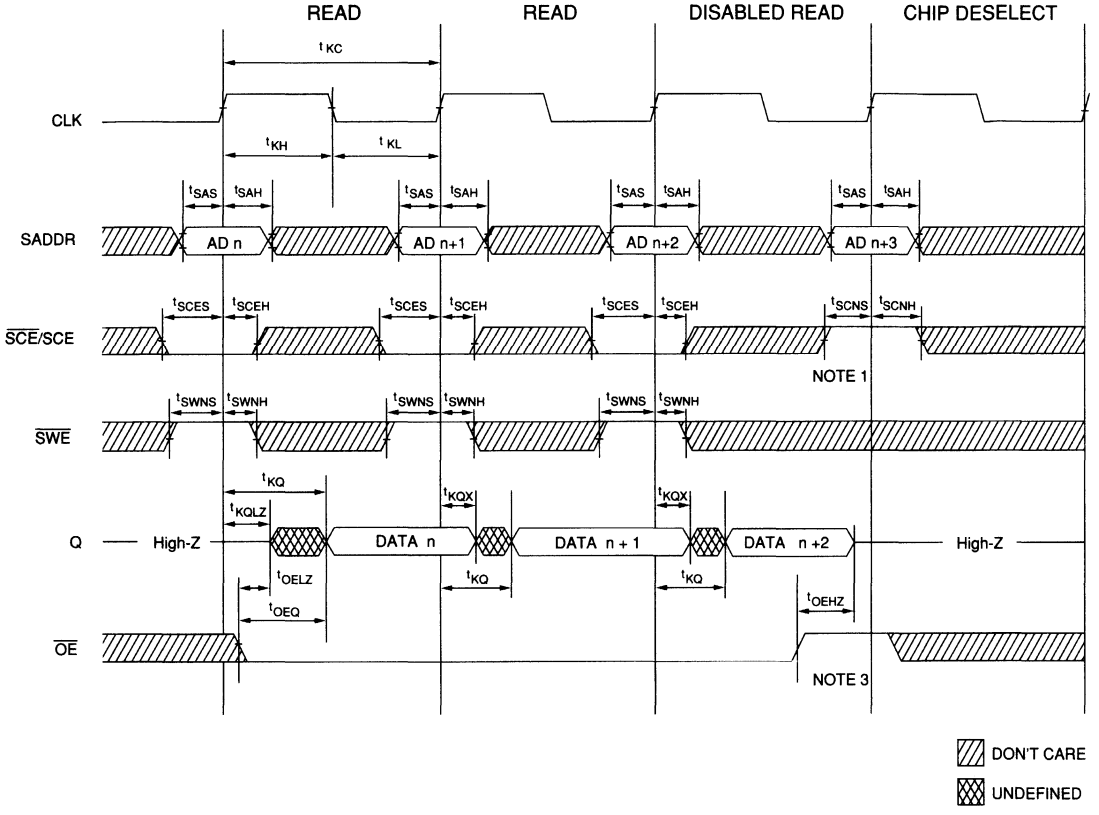


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

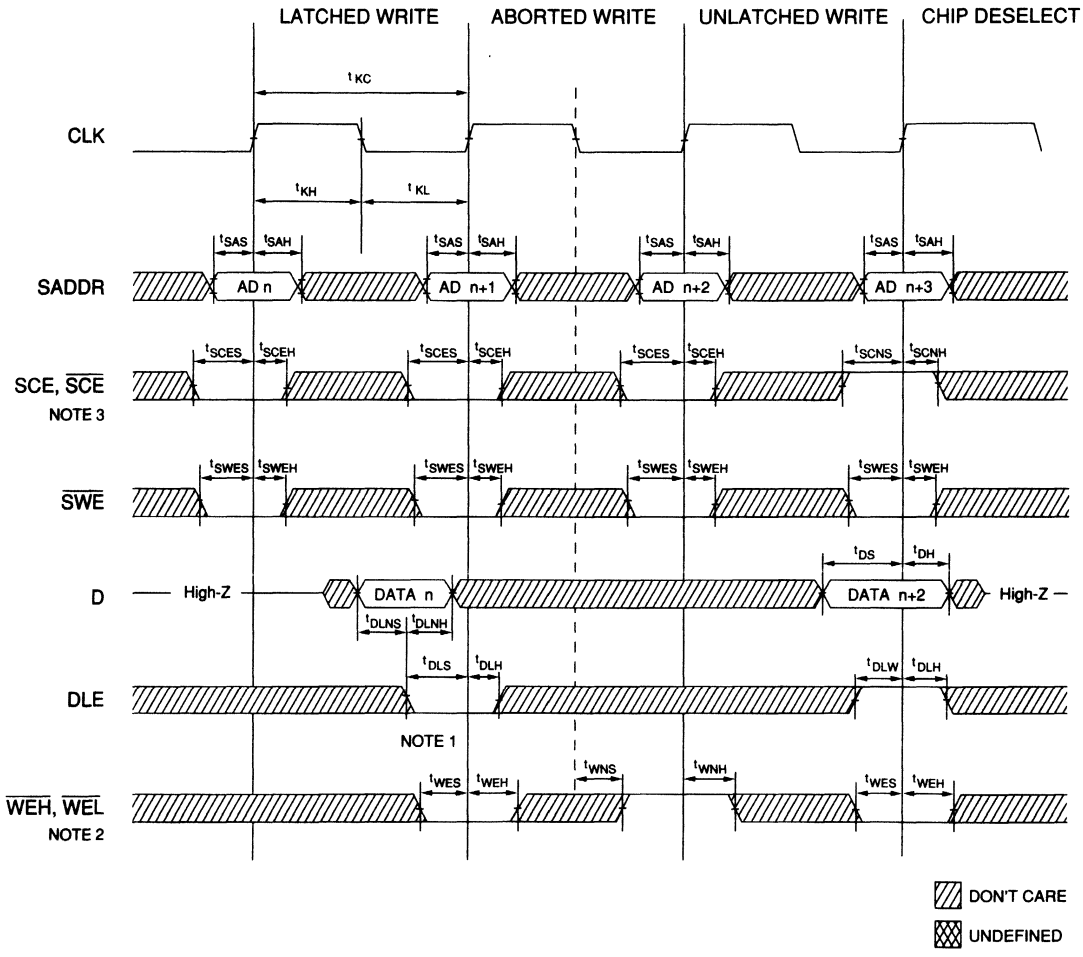
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}KQHZ$ is less than $^{t}KQLZ$ and $^{t}OEHZ$ is less than $^{t}OELZ$.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock.
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable and data latch enable.
11. $^{t}RC = {}^{t}WC = {}^{t}KC$

READ TIMING [2]



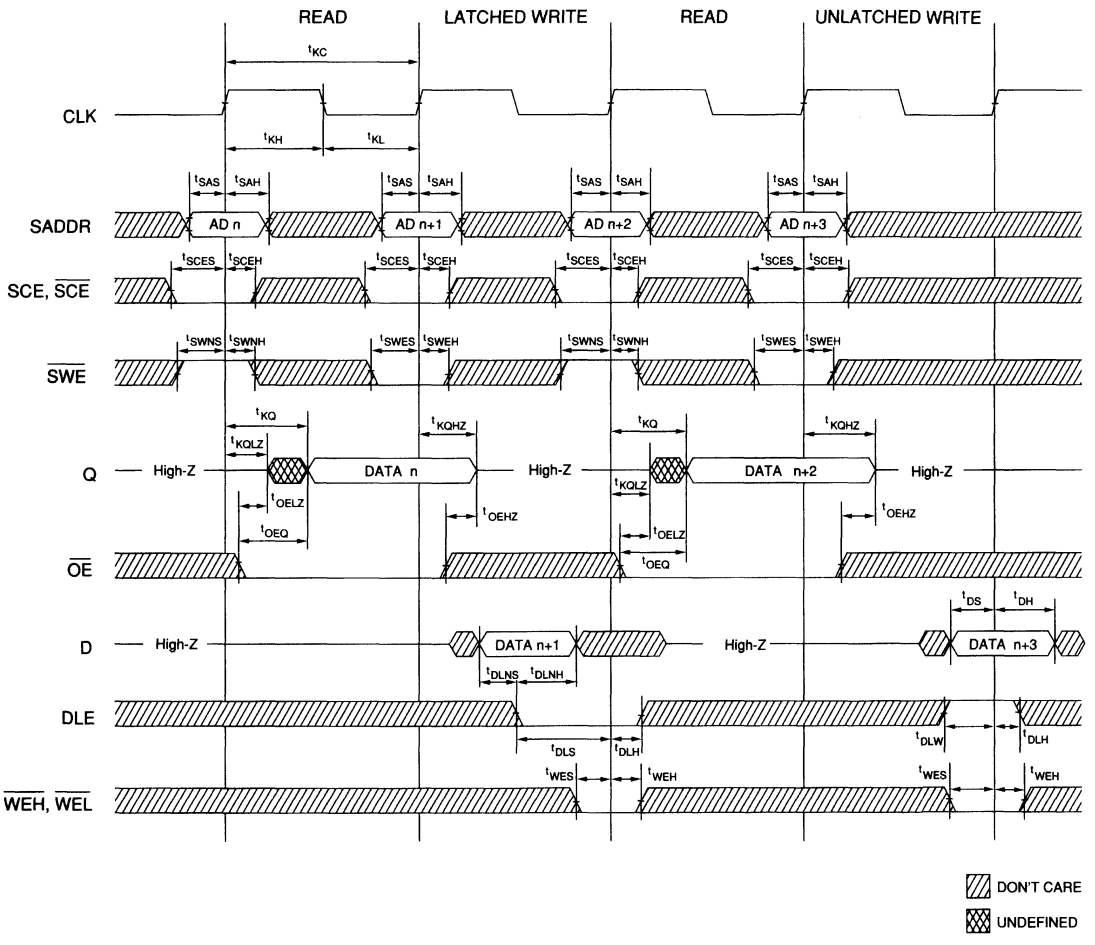
NOTE: 1. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.
2. $\overline{WEL}$ / $\overline{WEH}$ are "don't care" signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{OE}$) is inactive during a READ cycle.

WRITE TIMING



NOTE:
1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{WEH}$, $\overline{WEL}$) are available for use as byte write enables at the system level. They are also available to perform a LATE WRITE cycle abort.
3. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.

READ/WRITE TIMING



MICRON

3.3V SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Die	Page
				PLCC	PQFP	SOJ	TSOP		
16K x 16	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58LC1616	20, 25	52	52	-	-	CD1 CD2	4-1
16K x 18	Registered Address, Write Control, Dual Chip Enable, Data Input Latch, Output Enable	MT58LC1618	20, 25	52	52	-	-	CD1	4-11

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

SYNCHRONOUS SRAM

16K x 16 SRAM

3.3V OPERATION
CLOCKED, REGISTERED INPUTS

NEW
3.3 VOLT SYNCHRONOUS SRAM

FEATURES

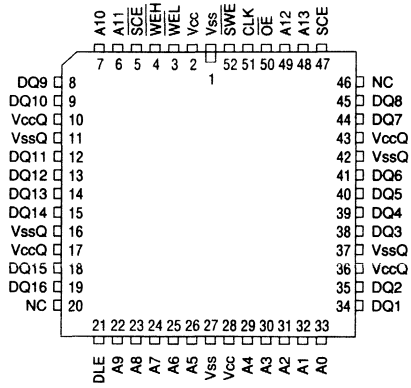
- Fast access times: 20 and 25ns
- Fast $\overline{OE}$: 8 and 10ns
- Single +3.3V ±0.3V power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Clock-controlled, registered address, write control and dual $\overline{CE}$s

OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 52-pin PLCC — EJ
  - 52-pin PQFP — LG
- Part Number Example: MT58LC1616LG-20

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC1616 SRAM is designed to operate at 3.3 volts. It integrates a 16K x 16 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered, single-clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{SCE}$, SCE) and the synchronous write enable ($\overline{SWE}$). Asynchronous inputs include the byte write enables ($\overline{WEL}$, $\overline{WEH}$), output enable ($\overline{OE}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{OE}$ during READ cycles, is asynchronous. The entire data word (DQ1 - DQ16) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and those systems that benefit from a wide data bus.

Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 while $\overline{WEH}$ controls DQ9-DQ16. $\overline{WEL}$/$\overline{WEH}$ allow WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{SCE}$) allow on-chip address decoding to be accomplished when the devices are used in a dual-bank mode.

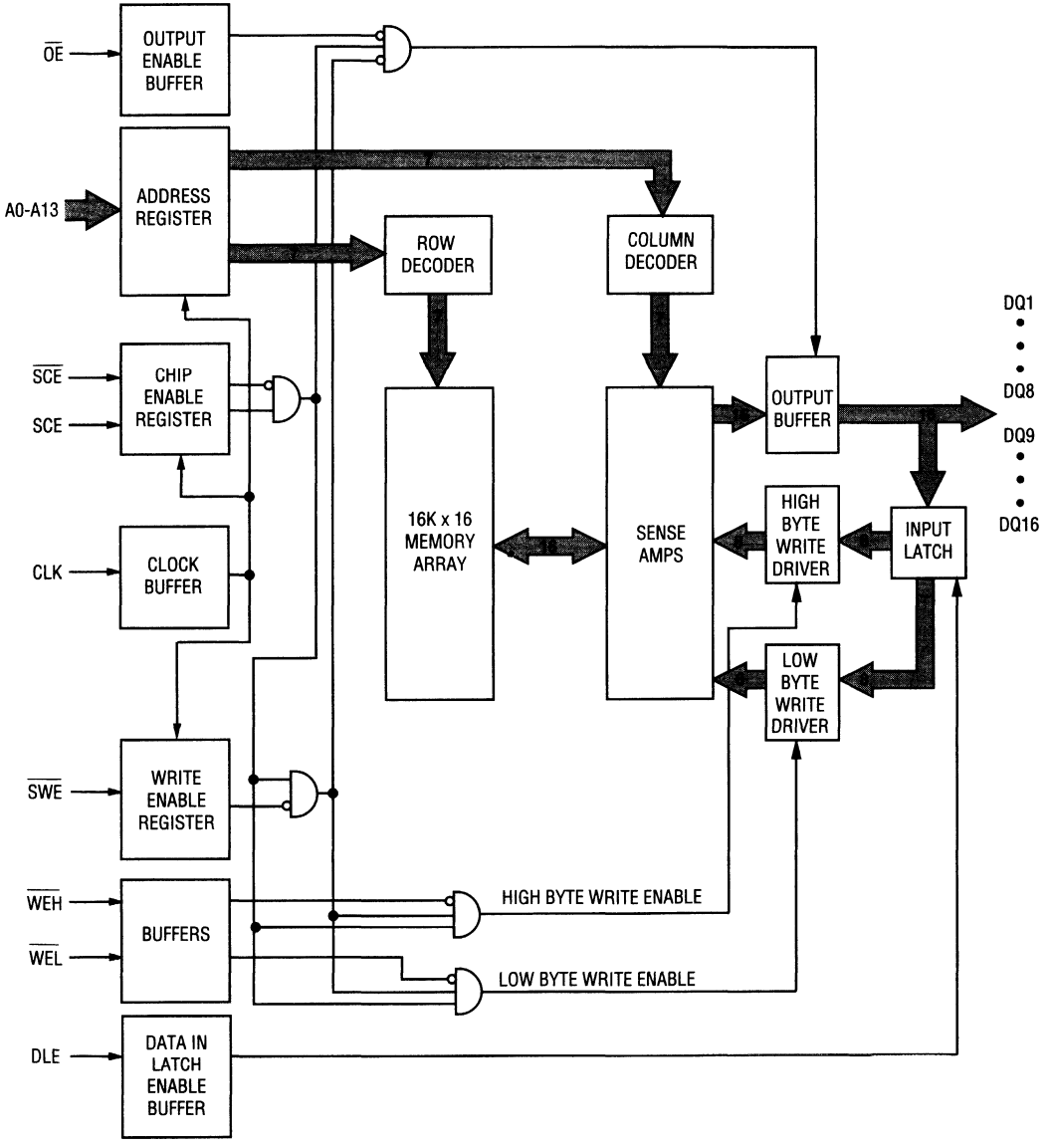
A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present at the inputs is held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58LC1616 operates from a +3.3V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

NEW

3.3 VOLT SYNCHRONOUS SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{SWE}$	Input	Synchronous Write Enable: This input is a synchronous write enable and must meet the setup and hold times around the rising edge of CLK. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	CLK	Input	Clock: This signal registers the address, SCE, $\overline{SCE}$ and $\overline{SWE}$ inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
3, 4	$\overline{WEL}$, $\overline{WEH}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{WEL}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{WEH}$ is LOW, data is written to the upper byte, D9-D16. A WRITE cycle can be aborted if both $\overline{WEL}$ and $\overline{WEH}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{SCE}$,SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{SCE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual-bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around CLK if data is latched.
20, 46	NC	Input/ Output	These pins are no connects (NCs). NCs are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE while being latched.
2, 28	Vcc	Supply	Power Supply: +3.3V ±0.3V
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±0.3V
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{SCE}$	$\overline{SWE}$	$\overline{WEL}$	$\overline{WEH}$	DLE	$\overline{OE}$	DQ
Deselected Cycle	L	X	X	X	X	X	X	High-Z
Deselected Cycle	X	H	X	X	X	X	X	High-Z
Read Cycle	H	L	H	X	X	X	H	High-Z
Read Cycle	H	L	H	X	X	X	L	Q1-Q16
Word Write Cycle DQ1-DQ16 Transparent Data-In	H	L	L	L	L	H	X	D1-D16
Word Write Cycle DQ1-DQ16 Latched Data-In	H	L	L	L	L	L	X	D1-D16
Aborted Write Cycle	H	L	L	H	H	X	X	High-Z
Byte Write Cycle DQ1-DQ8 Transparent Data-In	H	L	L	L	H	H	X	D1-D8
Byte Write Cycle DQ9-DQ16 Transparent Data-In	H	L	L	H	L	H	X	D9-D16
Byte Write Cycle DQ1-DQ8 Latched Data-In	H	L	L	L	H	L	X	D1-D8
Byte Write Cycle DQ9-DQ16 Latched Data-In	H	L	L	H	L	L	X	D9-D16

NOTE:
1. Registered inputs (addresses, $\overline{SWE}$, SCE and $\overline{SCE}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.
4. This device contains circuitry in High-Z during power-up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to Vcc+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V; Vss = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE}$ ≤ V_{IL}; SCE ≥ V_{IH}; f = MAX Vcc = MAX; Outputs Open	I_{CC}	70	100	mA	3
Power Supply Current: Standby	f = MAX; SCE ≤ V_{IL} or $\overline{SCE}$ ≥ V_{IH} Vcc = MAX; Outputs Open	I_{SB1}	15	30	mA	
	$\overline{SCE}$ ≥ Vcc -0.2; SCE ≤ Vss +0.2 Vcc = MAX; V_{IL} ≤ Vss +0.2 V_{IH} ≥ Vcc -0.2; f = 0	I_{SB2}	3	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 3.3V ±0.3V)

		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock							
Clock cycle time	^tKC	20		25		ns	
Clock HIGH time	^tKH	5		5		ns	
Clock LOW time	^tKL	8		8		ns	
Chip Enable							
SCE/$\overline{SCE}$ setup time	^tSCES	3		3		ns	10
SCE/$\overline{SCE}$ hold time	^tSCEH	2		2		ns	10
Address							
Address setup time	^tSAS	3		3		ns	10
Address hold time	^tSAH	2		2		ns	10
READ Cycle							
READ cycle time	^tRC	20		25		ns	11
Clock to output valid	^tKQ		20		25	ns	
Clock to output invalid	^tKQX	6		6		ns	10
Clock to output in Low-Z (WRITE cycle to READ cycle)	^tKQLZ	4		4		ns	6, 7
Clock to output in Low-Z (Idle cycle to READ cycle)	^tKQLZ	2		2		ns	6, 7
Clock to output in High-Z	^tKQHZ	6	12	6	12	ns	6, 7
$\overline{SWE}$ setup time	^tSWNS	3		3		ns	10
$\overline{SWE}$ hold time	^tSWNH	2		2		ns	10
$\overline{OE}$ to output valid	^tOEQ		8		10	ns	
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ	0	8	0	8	ns	6, 7
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	11
$\overline{SWE}$ setup time	^tSWES	3		3		ns	10
$\overline{SWE}$ hold time	^tSWEH	2		2		ns	10
Data setup time	^tDS	7		8		ns	8, 10
Data hold time	^tDH	2		2		ns	8, 10
Data to DLE not setup time	^tDLNS	1		1		ns	9, 10
Data to DLE not hold time	^tDLNH	3		3		ns	9, 10
DLE setup time	^tDLS	7		7		ns	9, 10
DLE hold time	^tDLH	2		2		ns	9, 10
DLE setup time (transparent WRITE cycle)	^tDLW	10		10		ns	9, 10
$\overline{WEL}$ / $\overline{WEH}$ setup time	^tWES	6		7		ns	10
$\overline{WEL}$ / $\overline{WEH}$ hold time	^tWEH	2		2		ns	10
$\overline{WEL}$ / $\overline{WEH}$ not setup time (aborted WRITE)	^tWNS		0		0	ns	10
$\overline{WEL}$ / $\overline{WEH}$ not hold time (aborted WRITE)	^tWNH	2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

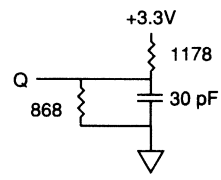


Fig. 1 OUTPUT LOAD EQUIVALENT

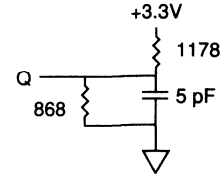


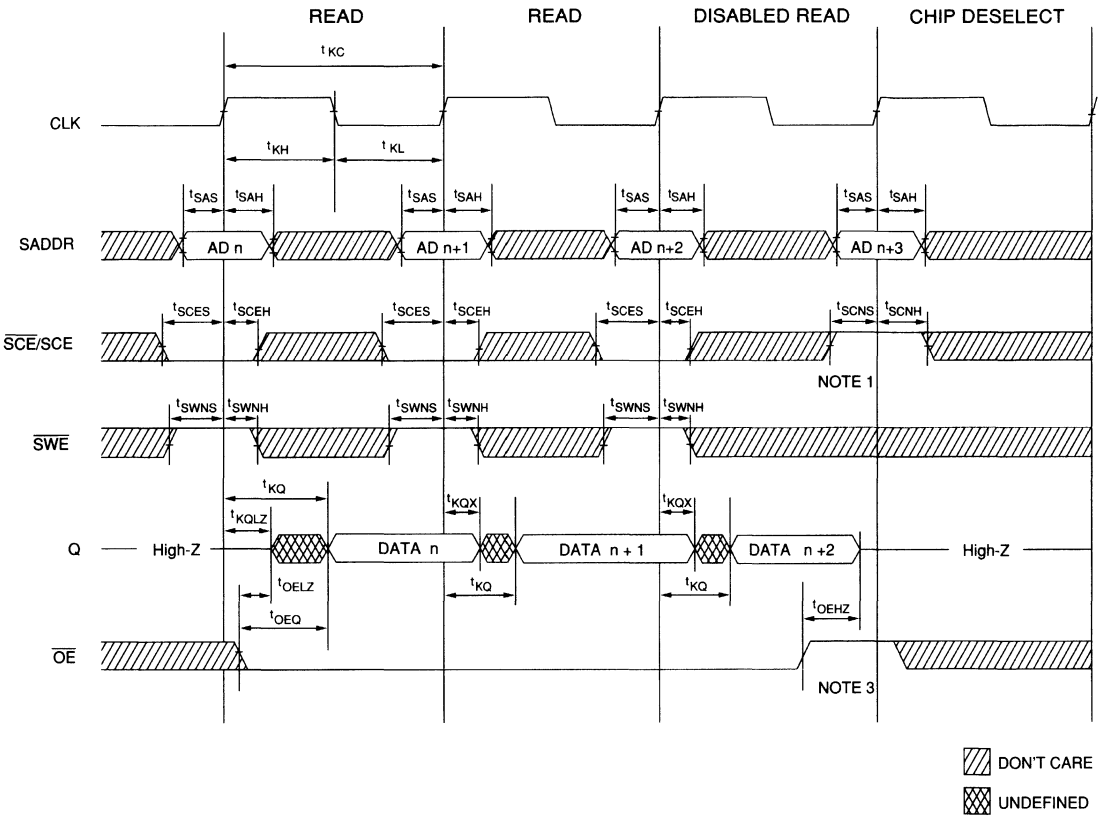
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5 pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}KQHZ$ is less than $^{t}KQLZ$, and $^{t}OEHZ$ is less than $^{t}OELZ$.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock.
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable and data latch enable.
11. $^{t}RC = {}^{t}WC = {}^{t}KC$

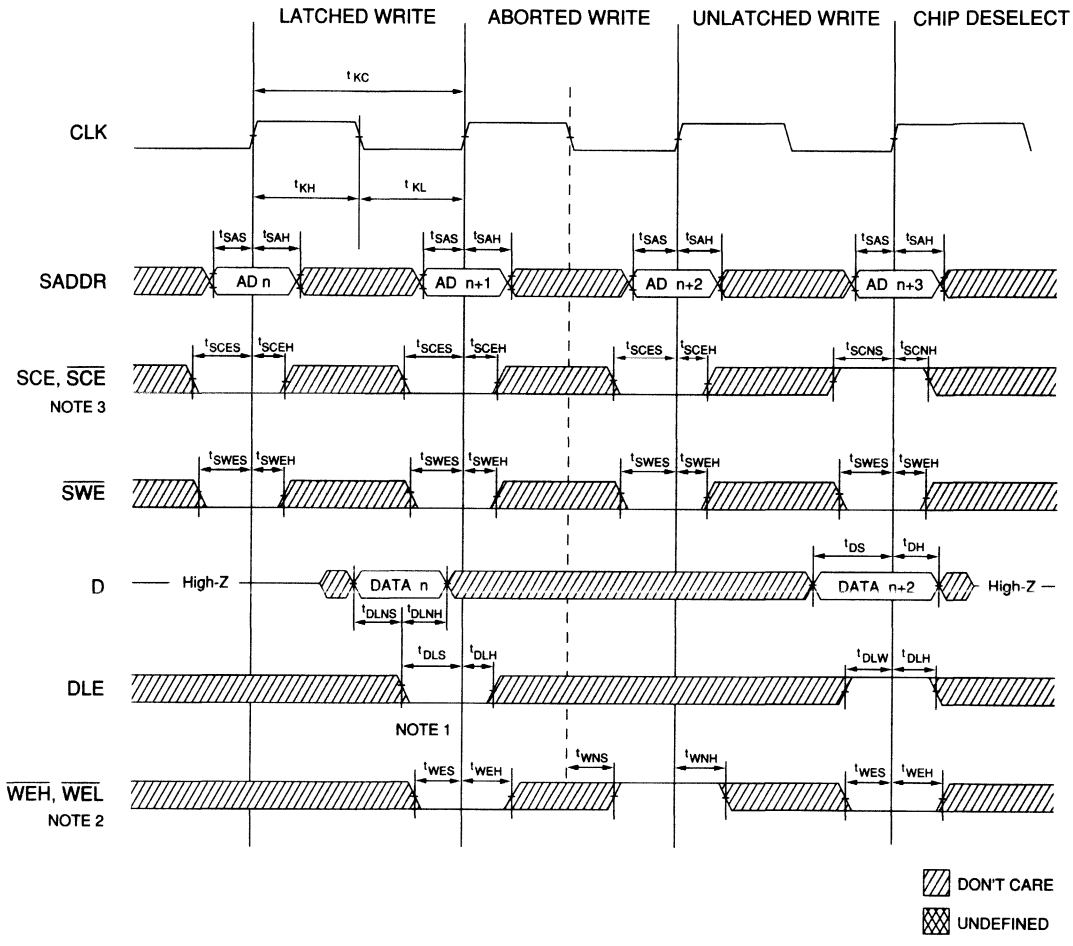
NEW 3.3 VOLT SYNCHRONOUS SRAM

READ TIMING [2]



NOTE: 1. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.
2. $\overline{WEL}$ / $\overline{WEH}$ are "don't care" signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{OE}$) is inactive during a READ cycle.

WRITE TIMING

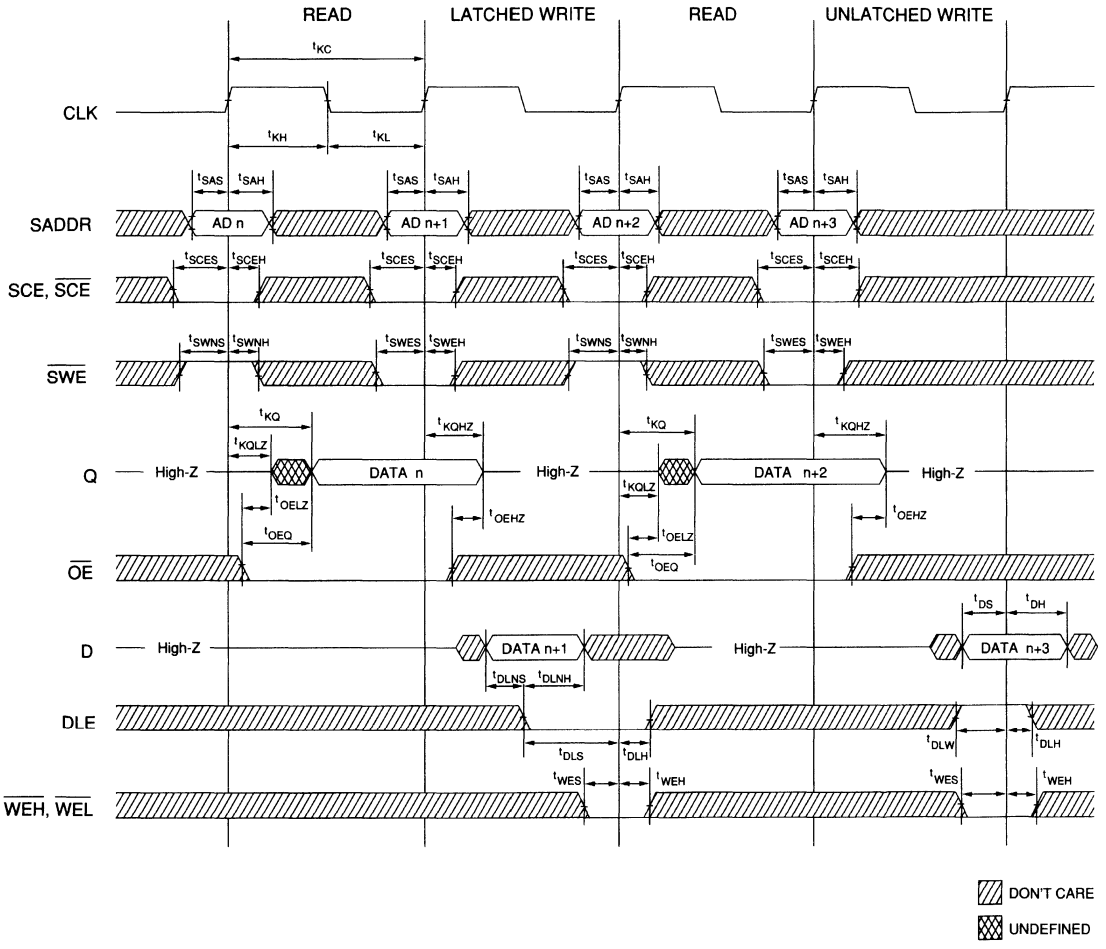


NOTE:
1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{WEH}$, $\overline{WEL}$) are available for use as byte write enables at the system level. They are also available to perform a $\overline{WRITE}$ cycle abort.
3. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.

NEW

3.3 VOLT SYNCHRONOUS SRAM

READ/WRITE TIMING



SYNCHRONOUS SRAM

16K x 18 SRAM

3.3V OPERATION
CLOCKED, REGISTERED INPUTS

NEW 3.3 VOLT SYNCHRONOUS SRAM

FEATURES

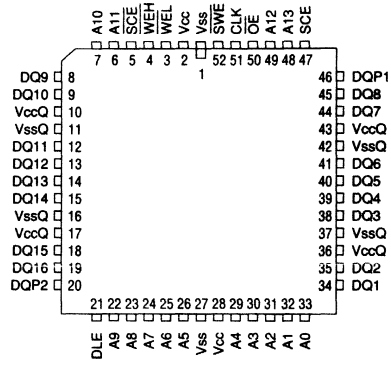
- Fast access times: 20 and 25ns
- Fast $\overline{OE}$: 8 and 10ns
- Single +3.3V ±0.3V power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Parity bits
- Clock controlled registered address, write control and dual $\overline{CE}$s

OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 52-pin PLCC — EJ
  - 52-pin PQFP — LG
- Part Number Example: MT58LC1618LG-20

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC1618 SRAM is designed to operate at 3.3 volts. It integrates a 16K x 18 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{SCE}$, SCE) and the synchronous write enable ($\overline{SWE}$). Asynchronous inputs include the byte write enables ($\overline{WEL}$, $\overline{WEH}$), output enable ($\overline{OE}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{OE}$ during READ cycles, is asynchronous. The entire data word (DQ1-DQ16, DQP1, DQP2) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and those systems that benefit from a wide data bus.

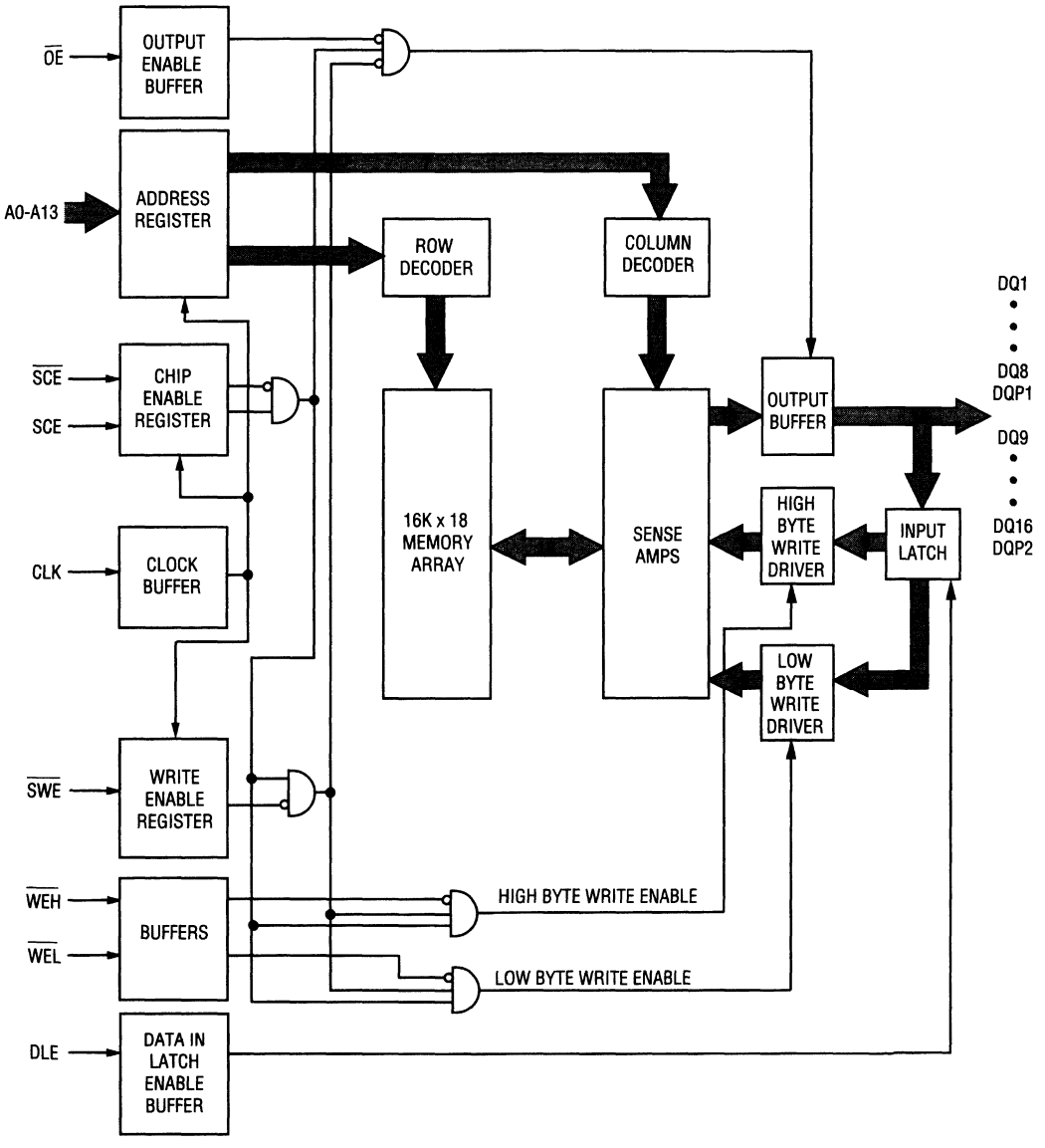
Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 and DQP1 while $\overline{WEH}$ controls DQ9-DQ16 and DQP2. $\overline{WEL}$/$\overline{WEH}$ allow LATE WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{SCE}$) allow on-chip address decoding to be accomplished when the devices are used in a dual-bank mode.

A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present at the input is held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58LC1618 operates from a +3.3V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

NEW
3.3 VOLT SYNCHRONOUS SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{SWE}$	Input	Synchronous Write Enable: This input is a synchronous write enable and must meet the setup and hold times around the rising edge of CLK. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	CLK	Input	Clock: This signal latches the address, SCE, $\overline{SCE}$, and $\overline{SWE}$ inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3, 4	$\overline{WEL}$, $\overline{WEH}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{WEL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{WEH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. A late WRITE cycle can be aborted if both $\overline{WEL}$ and $\overline{WEH}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{SCE}$,SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{SCE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual-bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around CLK if data is latched.
46, 20	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16. Parity data must meet the setup and hold time around DLE while being latched.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE while being latched.
2, 28	Vcc	Supply	Power Supply: +3.3V ±0.3V
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±0.3V
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{SCE}$	$\overline{SWE}$	$\overline{WEL}$	$\overline{WEH}$	DLE	$\overline{OE}$	DQ
Deselected Cycle	L	X	X	X	X	X	X	High-Z
Deselected Cycle	X	H	X	X	X	X	X	High-Z
Read Cycle	H	L	H	X	X	X	H	High-Z
Read Cycle	H	L	H	X	X	X	L	Q1-Q16, QP1, QP2
Word Write Cycle DQ1-DQ16, DQP1, DQP2, Transparent Data-In	H	L	L	L	L	H	X	D1-D16, DP1, DP2
Word Write Cycle DQ1-DQ16, DQP1, DQP2, Latched Data-In	H	L	L	L	L	L	X	D1-D16, DP1, DP2
Aborted Write Cycle	H	L	L	H	H	X	X	High-Z
Byte Write Cycle DQ1-DQ8, DQP1 Transparent Data-In	H	L	L	L	H	H	X	D1-D8, DP1
Byte Write Cycle DQ9-DQ16, DQP2 Transparent Data-In	H	L	L	H	L	H	X	D9-D16, DP2
Byte Write Cycle DQ1-DQ8, DQP1 Latched Data-In	H	L	L	L	H	L	X	D1-D8, DP1
Byte Write Cycle DQ9-DQ16, DQP2 Latched Data-In	H	L	L	H	L	L	X	D9-D16, DP2

NOTE:
1. Registered inputs (addresses, $\overline{SWE}$, SCE, and $\overline{SCE}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.
4. This device contains circuitry to ensure that imputs are in High-Z during power-up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±0.3V; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE}$ ≤ V_{IL}; SCE ≥ V_{IH}; f = MAX V_{CC} = MAX; Outputs Open	I_{CC}	70	100	mA	3
Power Supply Current: Standby	SCE ≤ V_{IL} or $\overline{SCE}$ ≥ V_{IH} V_{CC} = MAX; f = MAX; Outputs Open	I_{SB1}	15	30	mA	
	$\overline{SCE}$ ≥ V_{CC} -0.2; SCE ≤ V_{SS} +0.2 V_{CC} = MAX; V_{IL} ≤ V_{SS} +0.2 V_{IH} ≥ V_{CC} -0.2; f = 0	I_{SB2}	3	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 3.3V	$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 3.3V ±0.3V)

		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock							
Clock cycle time	^tKC	20		25		ns	
Clock HIGH time	^tKH	5		5		ns	
Clock LOW time	^tKL	8		8		ns	
Chip Enable							
SCE/$\overline{SCE}$ setup time	^tSCES	3		3		ns	10
SCE/$\overline{SCE}$ hold time	^tSCEH	2		2		ns	10
Address							
Address setup time	^tSAS	3		3		ns	10
Address hold time	^tSAH	2		2		ns	10
READ Cycle							
READ cycle time	^tRC	20		25		ns	11
Clock to output valid	^tKQ		20		25	ns	
Clock to output invalid	^tKQX	6		6		ns	10
Clock to output in Low-Z (WRITE cycle to READ cycle)	^tKQLZ	4		4		ns	6, 7
Clock to output in Low-Z (Idle cycle to READ cycle)	^tKQLZ	2		2		ns	6, 7
Clock to output in High-Z	^tKQHZ	6	12	6	12	ns	6, 7
$\overline{SWE}$ setup time	^tSWNS	3		3		ns	10
$\overline{SWE}$ hold time	^tSWNH	2		2		ns	10
$\overline{OE}$ to output valid	^tOEQ		8		10	ns	
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ	0	8	0	8	ns	6, 7
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	11
$\overline{SWE}$ setup time	^tSWES	3		3		ns	10
$\overline{SWE}$ hold time	^tSWEH	2		2		ns	10
Data setup time	^tDS	7		8		ns	8, 10
Data hold time	^tDH	2		2		ns	8, 10
Data to DLE not setup time	^tDLNS	1		1		ns	9, 10
Data to DLE not hold time	^tDLNH	3		3		ns	9, 10
DLE setup time	^tDLS	7		7		ns	9, 10
DLE hold time	^tDLH	2		2		ns	9, 10
DLE setup time (transparent WRITE cycle)	^tDLW	10		10		ns	9, 10
$\overline{WEL}$ / $\overline{WEH}$ setup time	^tWES	6		7		ns	10
$\overline{WEL}$ / $\overline{WEH}$ hold time	^tWEH	2		2		ns	10
$\overline{WEL}$ / $\overline{WEH}$ not setup time (aborted WRITE)	^tWNS		0		0	ns	10
$\overline{WEL}$ / $\overline{WEH}$ not hold time (aborted WRITE)	^tWNH	2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

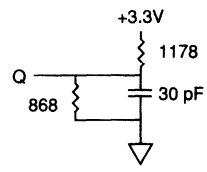


Fig. 1 OUTPUT LOAD EQUIVALENT

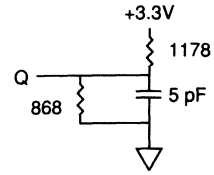
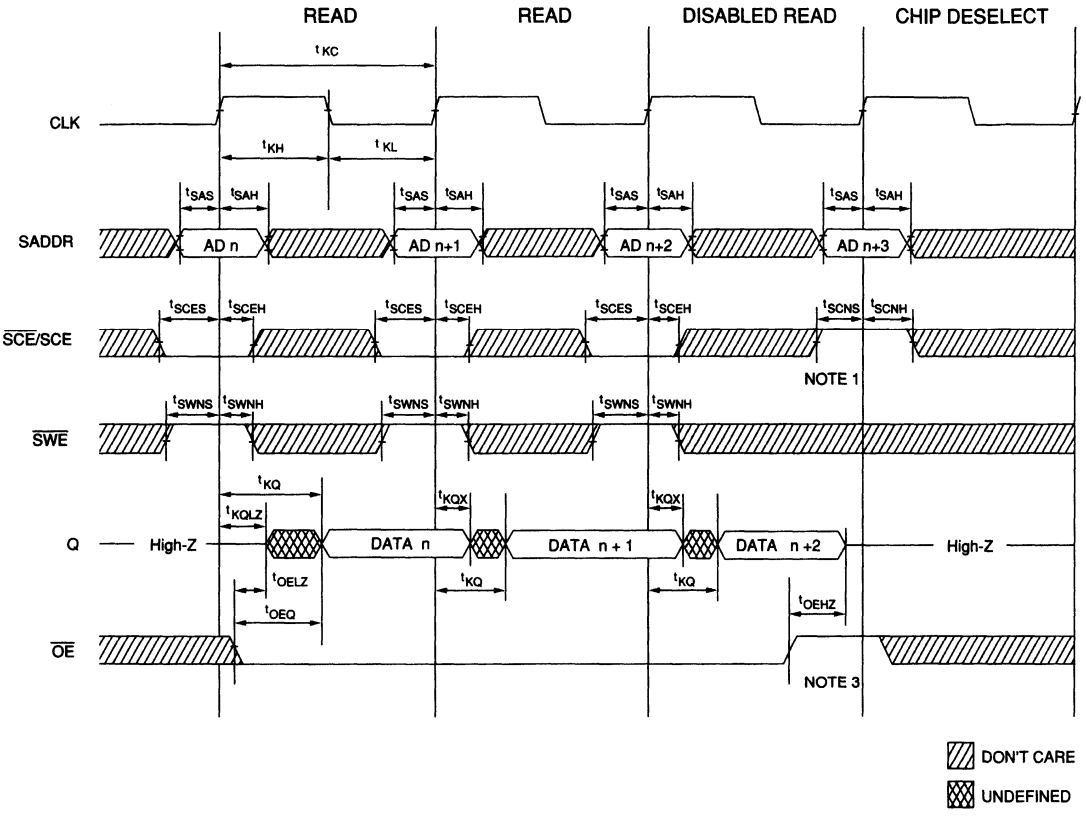


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

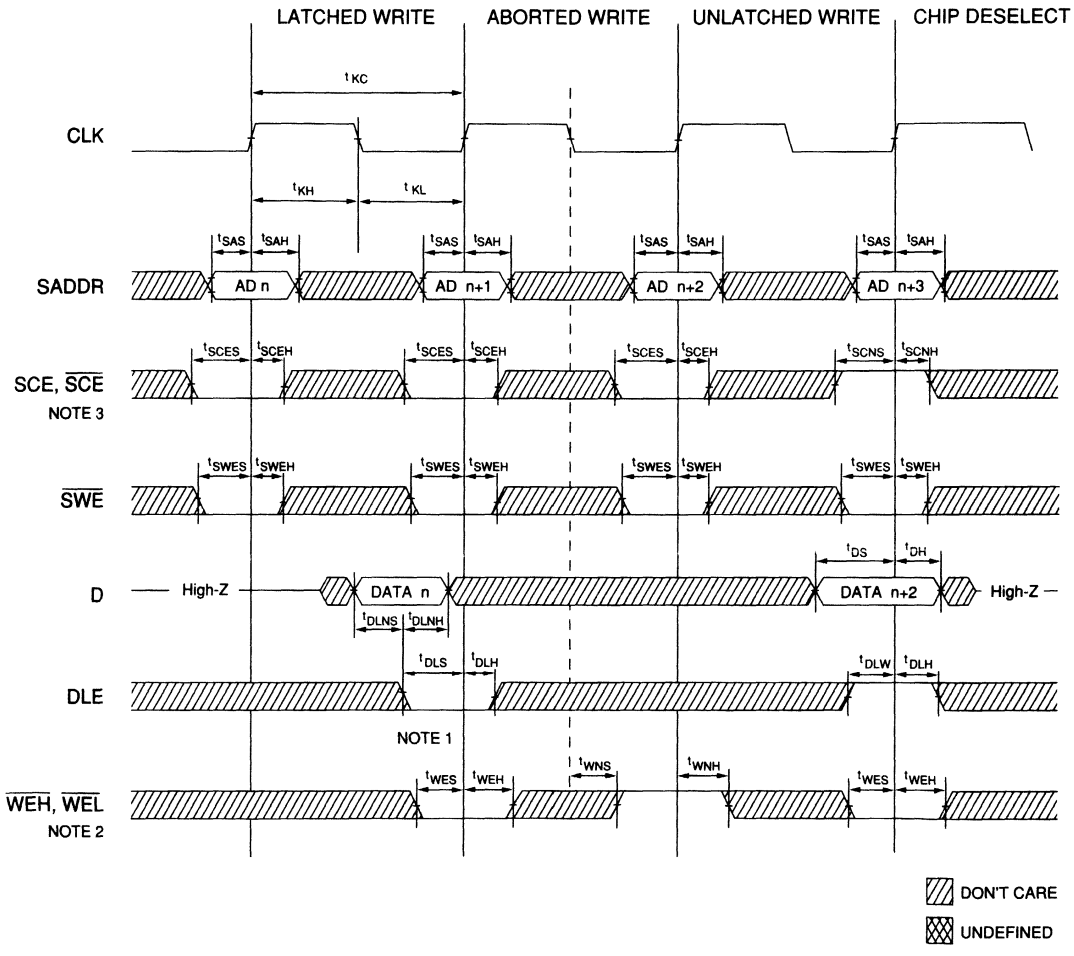
1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}KQHZ is less than ^{t}KQLZ, and ^{t}OEHZ is less than ^{t}OELZ.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock.
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable and data latch enable.
11. ^{t}RC = ^{t}WC = ^{t}KC

READ TIMING [2]



NOTE: 1. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.
2. $\overline{WEL}$ / $\overline{WEH}$ are "don't care" signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{OE}$) is inactive during a READ cycle.

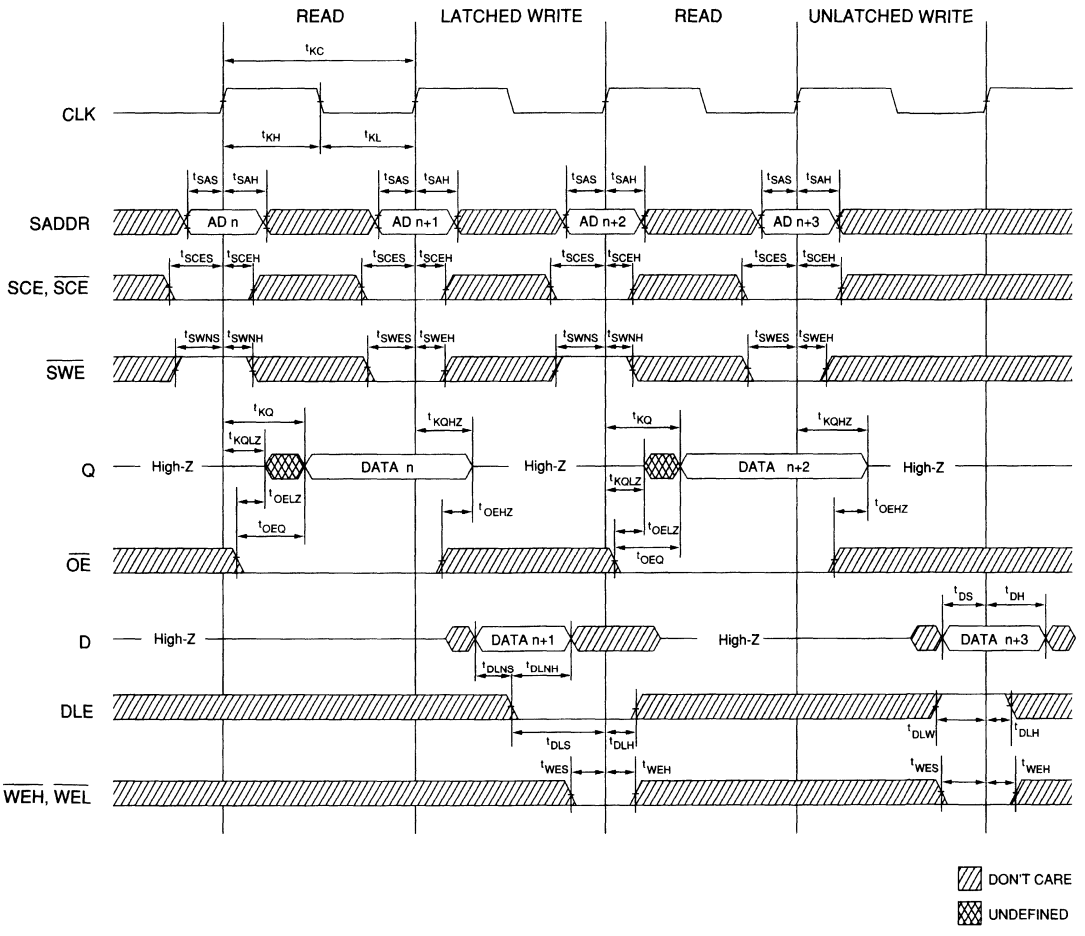
WRITE TIMING



NOTE:
1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{WEH}$, $\overline{WEL}$) are available for use as byte write enables at the system level. They are also available to perform a LATE WRITE cycle abort.
3. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.

NEW 3.3 VOLT SYNCHRONOUS SRAM

READ/WRITE TIMING



MICRON

5V CACHE DATA/LATCHED SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package				Die	Page
				PLCC	PQFP	SOJ	TSOP		
Single 8K x 16 or Dual 4K x 16	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A11)	MT56C0816	20, 25, 35	52	52	-	-		5-1
Single 8K x 16 or Dual 4K x 16	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A12)	MT56C3816	20, 25, 35	52	52	-	-		5-13
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Write Controls, Output Enable	MT5C2516	12, 15, 20, 25	52	52	-	-	CD1 CD2	5-25
Single 8K x 18 or Dual 4K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A11)	MT56C0818	20, 25, 35	52	52	-	-		5-39
Single 8K x 18 or Dual 4K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Synchronous Write Enable	MT56C2818	24	52	52	-	-		5-51
Single 8K x 18 or Dual 4K x 18	Mode, Byte Select, $\overline{CE}$, $\overline{OE}$ Address Latch (A0-A12)	MT56C3818	20, 25, 35	52	52	-	-		5-61
16K x 18	Latched Address and Data, Dual Chip Enables, Byte Write Controls	MT5C2818	12, 15, 20, 25	52	52	-	-	CD1 CD2	5-73
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Enables	MT56C16K16B2	12, 15, 20, 25	52	52	-	-	CD1 CD2	5-87

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

CACHE DATA SRAM

SINGLE 8K x 16 SRAM, DUAL 4K x 16 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

- Operates as two 4K x 16 SRAMs with common addresses and data; also configurable as a single 8K x 16 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 20, 25 and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast $\overline{OE}$: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 cache memory controllers

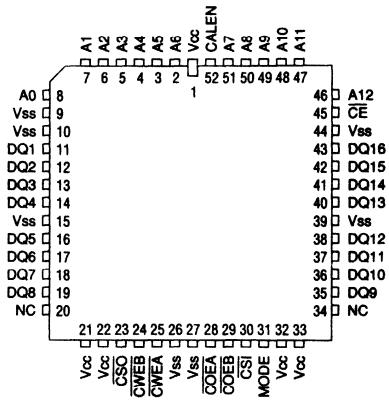
OPTIONS

	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

- Part Number Example: MT56C0816EJ-25

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-4)



GENERAL DESCRIPTION

The MT56C0816 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C0816 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE MODE. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 16-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 16-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

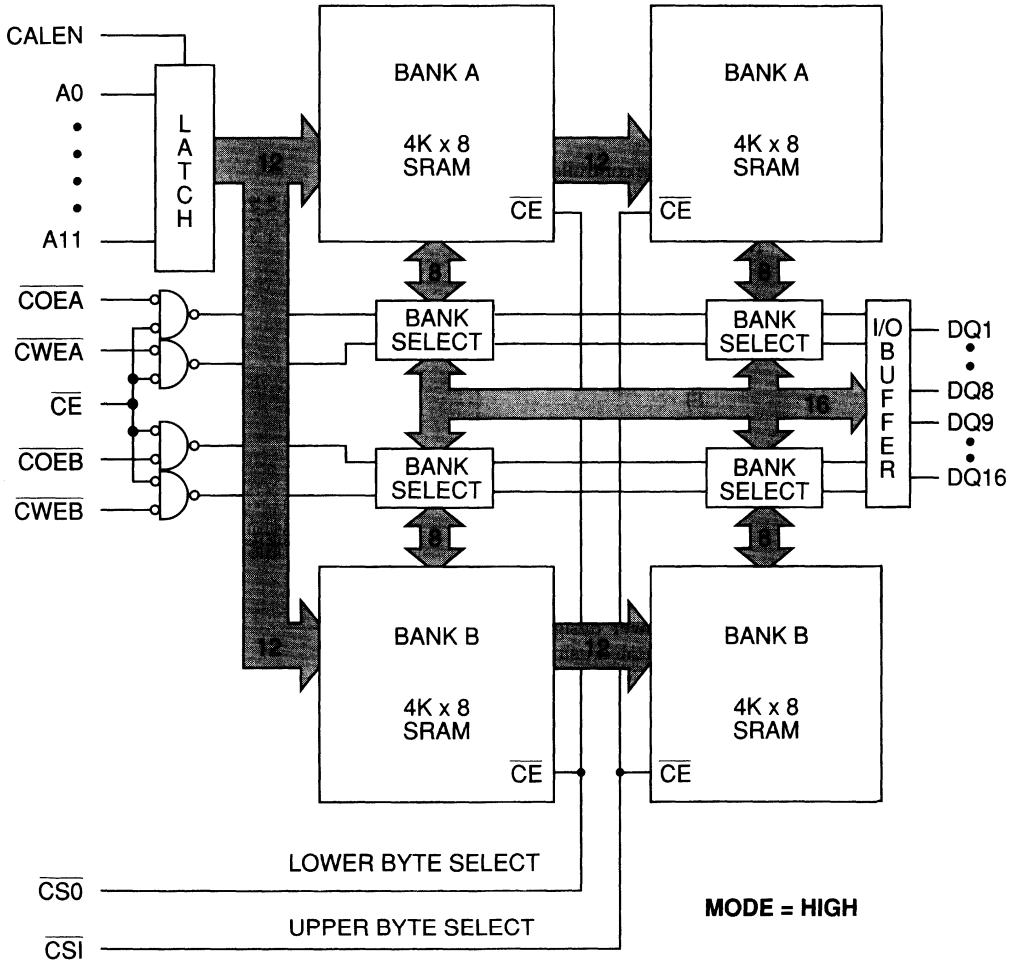
Outputs are enabled on a HIGH-to-LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH-to-LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C0816 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

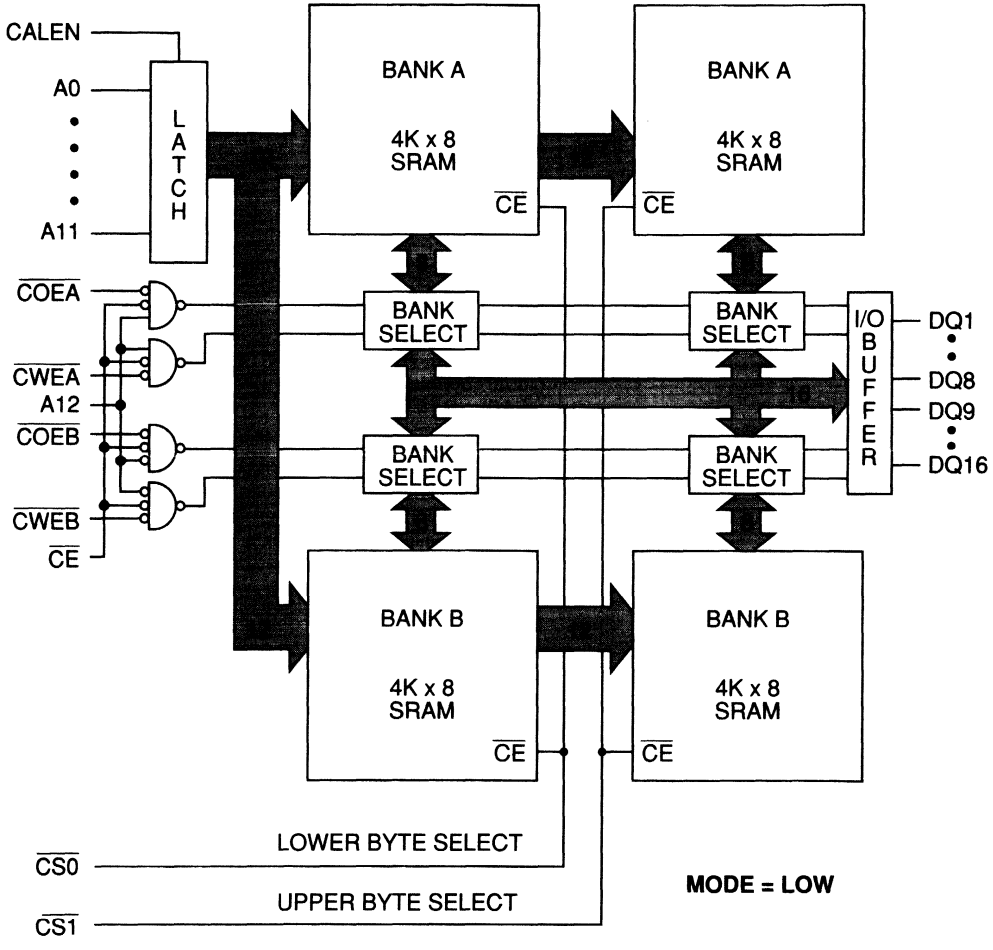
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 16
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 16
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order-address bit in the direct 8K x 16 configuration. It is not used in the dual 4K x 16 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 16 configuration. When the pin is tied LOW, the device is configured as an 8K x 16 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the output.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data WRITE to the addressed memory location. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16, 17, 18, 19, 35, 36, 37, 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 16 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16 bank A	L	H	L	L	H	H	H
READ DQ9- DQ16 bank B	L	H	L	H	L	H	H
READ DQ1- DQ16 bank A	L	L	L	L	H	H	H
READ DQ1- DQ16 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 16 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8	L	L	H	L	L	H	H
READ DQ9-DQ16	L	H	L	L	L	H	H
READ DQ1-DQ16	L	L	L	L	L	H	H
WRITE DQ1-DQ8	L	L	H	X	X	L	L
WRITE DQ9-DQ16	L	H	L	X	X	L	L
WRITE DQ1-DQ16	L	L	L	X	X	L	L

NOTE: 1. $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc +0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-5	5	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-5	5	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty Cycle VIN = GND to Vcc	ICC1	120	220	mA	
Power Supply Current: Average Operating Current	50% Duty Cycle VIN = GND to Vcc	ICC2	65	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc - 0.2V Vcc = MAX VIN ≤ Vss + 0.2V or VIN ≥ Vcc - 0.2V	ISB	2.0	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	CIN	6	pF	3
Output Capacitance	Vcc = 5V	CI/O	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	ØJA	100	°C/W	
Thermal resistance – Junction to Case		ØJC	45	°C/W	
Thermal resistance mounted on 2" x 3" PC board		ØJA	70	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		35		ns	4, 5
Address access time (A0-A11)	^tAA		20		25		35	ns	
A12 address access time	^tA12A		15		17		25	ns	
Chip Enable access time	^tACE		20		20		25	ns	
Chip Select access time	^tACS		20		25		35	ns	
Output Enable access time	^tAOE		8		10		13	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip Select to output Low-Z	^tLZCS	3		3		3		ns	
Output Enable to output Low-Z	^tLZOE	2		2		2		ns	
Chip deselect to output High-Z	^tHZCS		15		15		25	ns	6
Output disable to output High-Z	^tHZOE		10		10		14	ns	6
Address Latch Enable pulse width	^tCALEN	8		8		10		ns	
Address setup to latch LOW	^tASL	4		4		6		ns	
Address hold from latch LOW	^tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	^tWC	20		25		35		ns	
Address valid to end of write	^tAW	15		18		25		ns	
A12 address valid to end of write	^tA12W	15		18		25		ns	
Chip Select to end of write	^tCW	15		18		25		ns	
Data valid to end of write	^tDW	10		10		10		ns	
Data hold from end of write	^tDH	0		0		0		ns	
Write Enable output in High-Z	^tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	^tLZWE	3		3		3		ns	
WRITE pulse width	^tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	^tCP	15		18		25		ns	
Address setup time	^tAS	0		0		0		ns	
WRITE recovery time	^tWR	0		0		0		ns	
Address Latch Enable pulse width	^tCALEN	8		8		10		ns	
Address setup to latch LOW	^tASL	4		4		6		ns	
Address hold from latch LOW	^tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

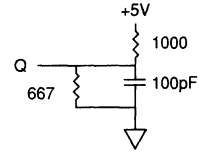


Fig. 1 OUTPUT LOAD EQUIVALENT

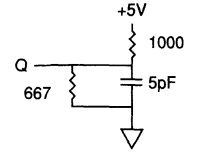


Fig. 2 OUTPUT LOAD EQUIVALENT

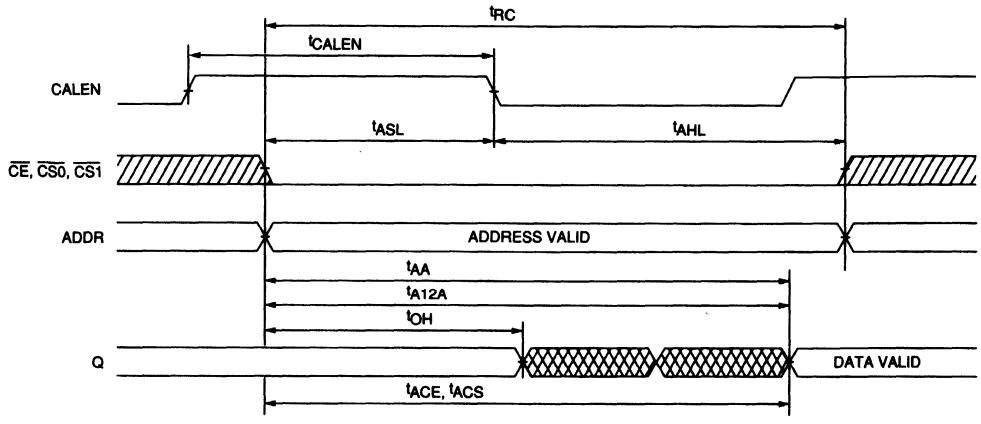
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^tHZCS, ^tHZOE, and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

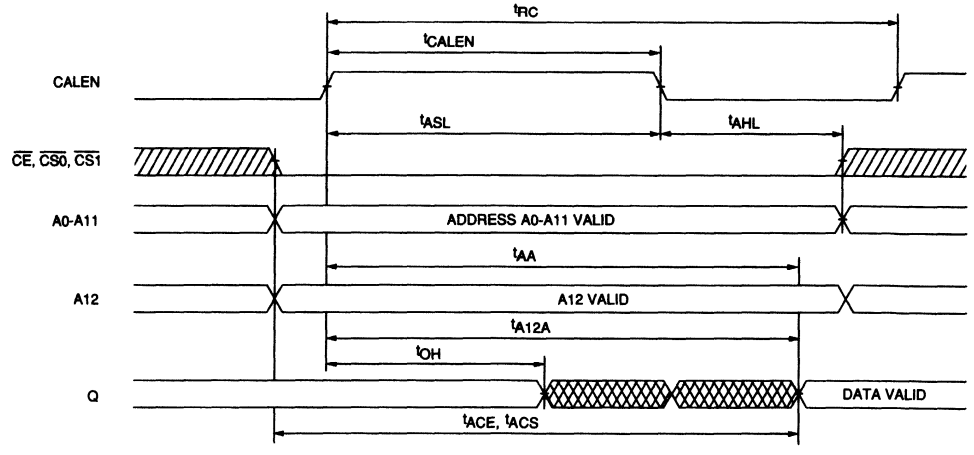
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

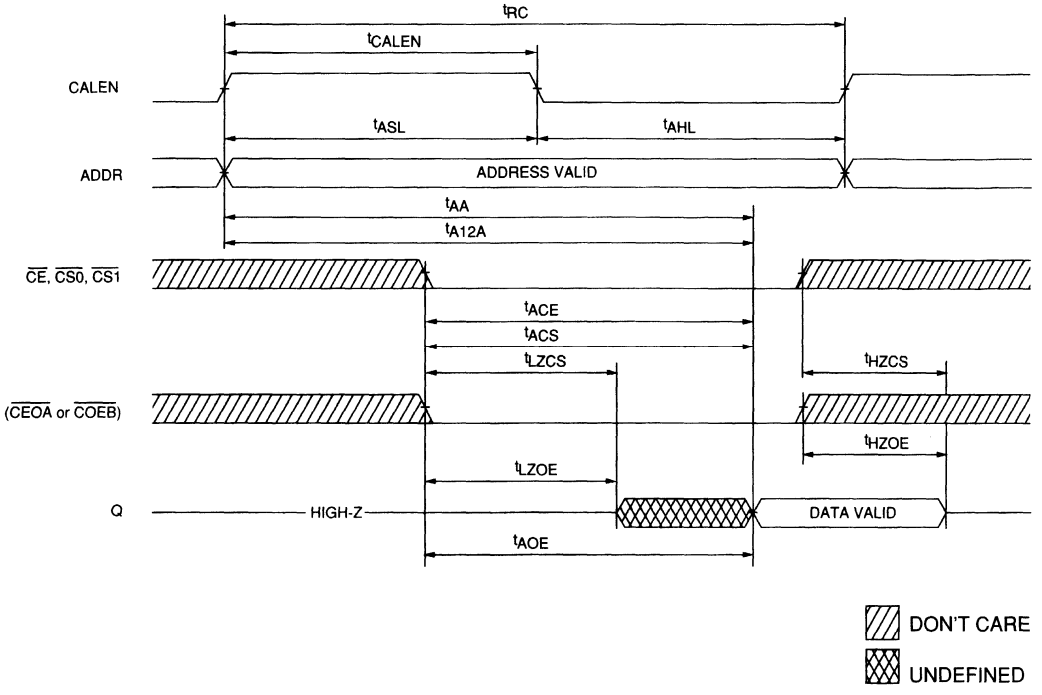


DON'T CARE

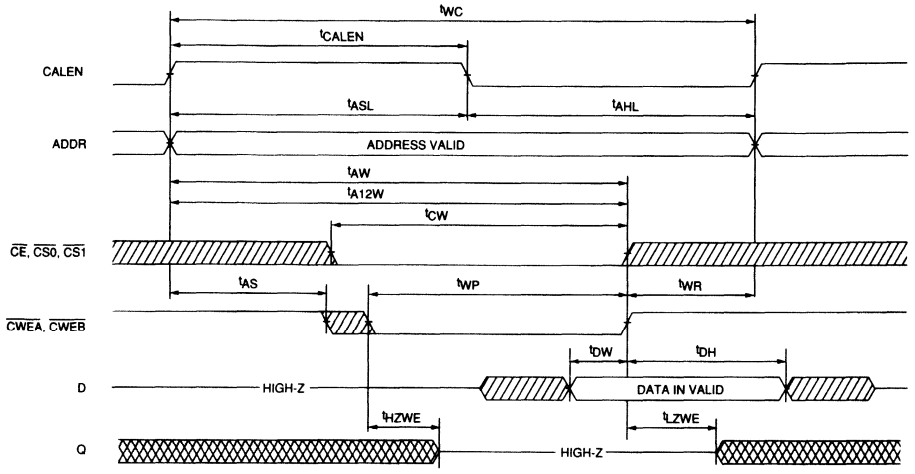
UNDEFINED

READ CYCLE NO. 3

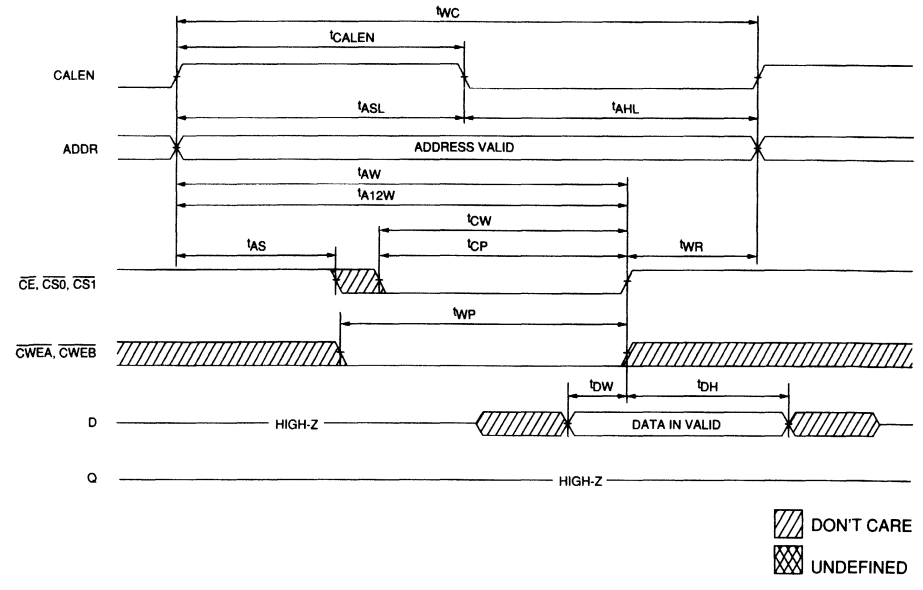
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA SRAM

SINGLE 8K x 16 SRAM, DUAL 4K x 16 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

- Operates as two 4K x 16 SRAMs with common addresses and data; also configurable as a single 8K x 16 SRAM
- Built-in input address latches (A0-A12)
- Separate upper and lower Byte Select
- Fast access times: 20, 25 and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast $\overline{OE}$: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 and 80486 cache memory controllers

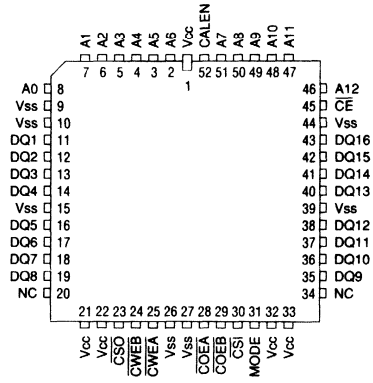
OPTIONS

	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

- Part Number Example: MT56C3816EJ-25

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-4)



GENERAL DESCRIPTION

The MT56C3816 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C3816 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE MODE. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 16-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 16-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

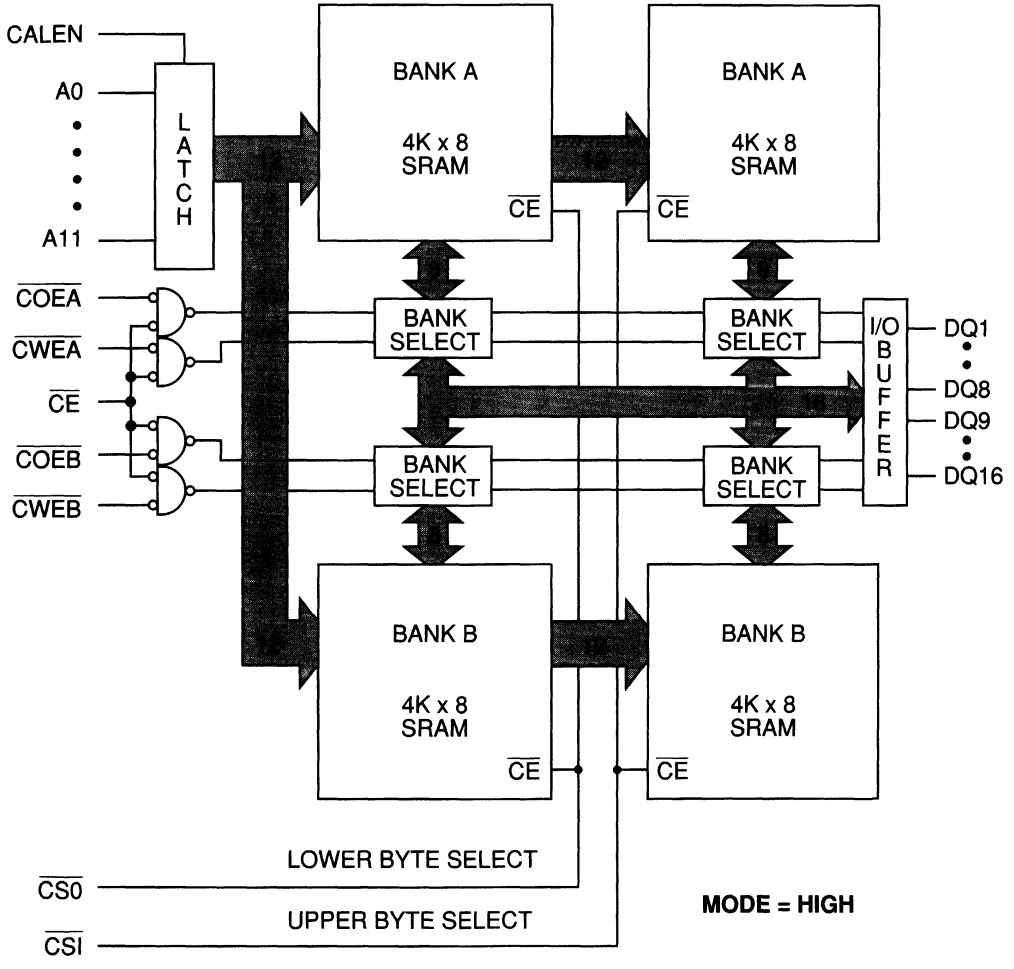
Outputs are enabled on a HIGH-to-LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH-to-LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C3816 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

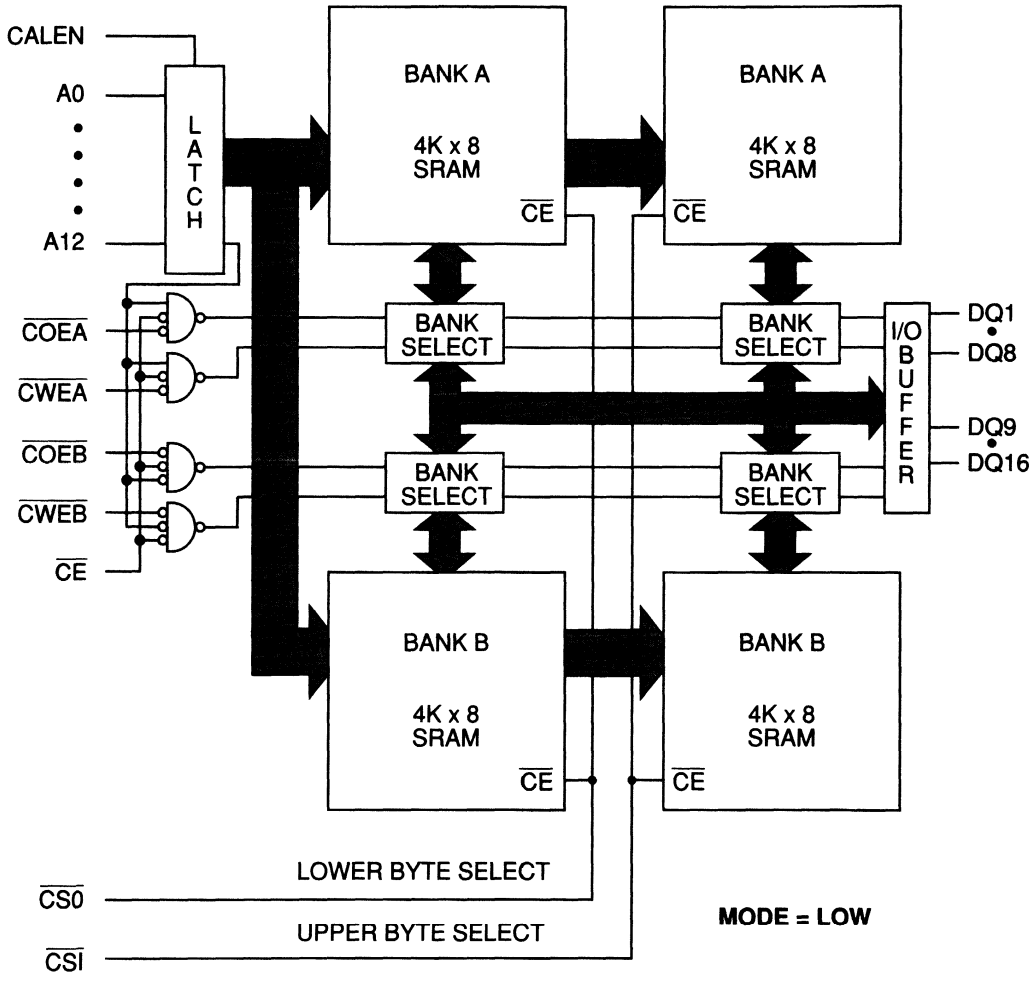
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 16
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 16
(DIRECT MAP)



5 VOLT CACHE DATA/LATCHED SRAM

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order-address bit in the direct 8K x 16 configuration. It is not used in the dual 4K x 16 configuration. This input is latched by the negative edge of CALEN.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A12).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 16 configuration. When the pin is tied LOW, the device is configured as an 8K x 16 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	WRITE ENABLE: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the DIRECT mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16, 17, 18, 19, 35, 36, 37, 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 16 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 16 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8	L	L	H	L	L	H	H
READ DQ9-DQ16	L	H	L	L	L	H	H
READ DQ1-DQ16	L	L	L	L	L	H	H
WRITE DQ1-DQ8	L	L	H	X	X	L	L
WRITE DQ9-DQ16	L	H	L	X	X	L	L
WRITE DQ1-DQ16	L	L	L	X	X	L	L

NOTE: 1. $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

2. $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc+0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-5	5	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-5	5	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc	ICC1	120	220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc	ICC2	65	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc -0.2V Vcc = MAX VIN ≤ Vss +0.2V or VIN ≥ Vcc -0.2V	ISB	2.0	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	CIN	6	pF	3
Output Capacitance	Vcc = 5V	CI/O	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	ΘJA	100	°C/W	
Thermal resistance – Junction to Case		ΘJC	45	°C/W	
Thermal resistance mounted on 2" x 3" PC board		ΘJA	70	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; Vcc = 5V ±5%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A12)	tAA		20		25		35	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write Enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
WRITE pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
WRITE recovery time	tWR	0		0		0		ns	
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

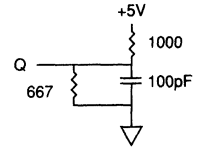


Fig. 1 OUTPUT LOAD EQUIVALENT

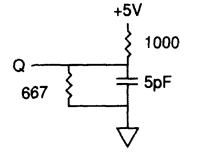


Fig. 2 OUTPUT LOAD EQUIVALENT

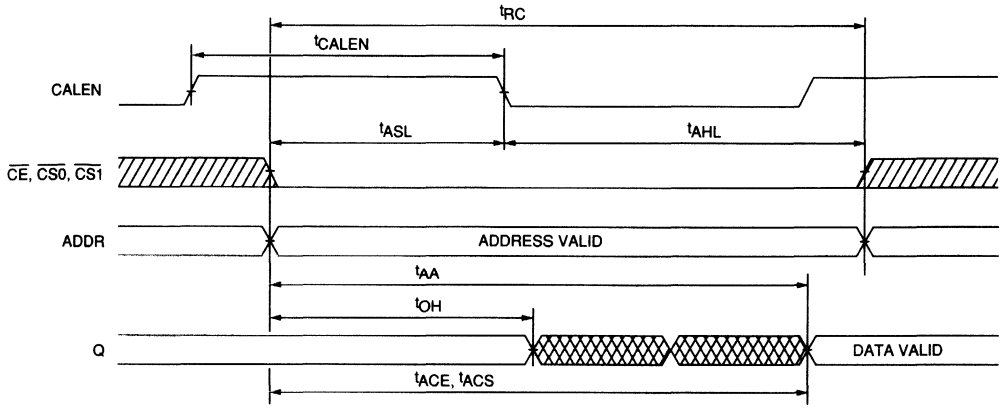
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

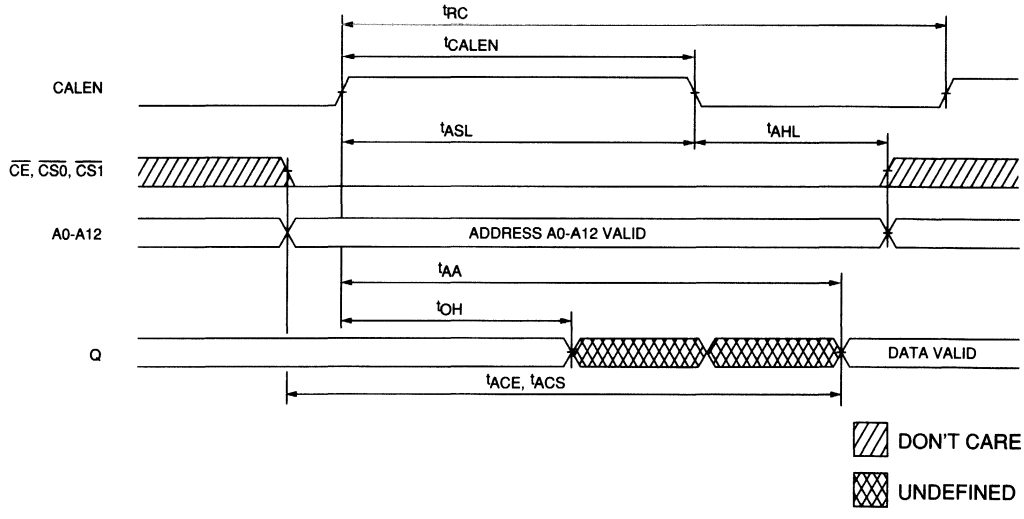
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

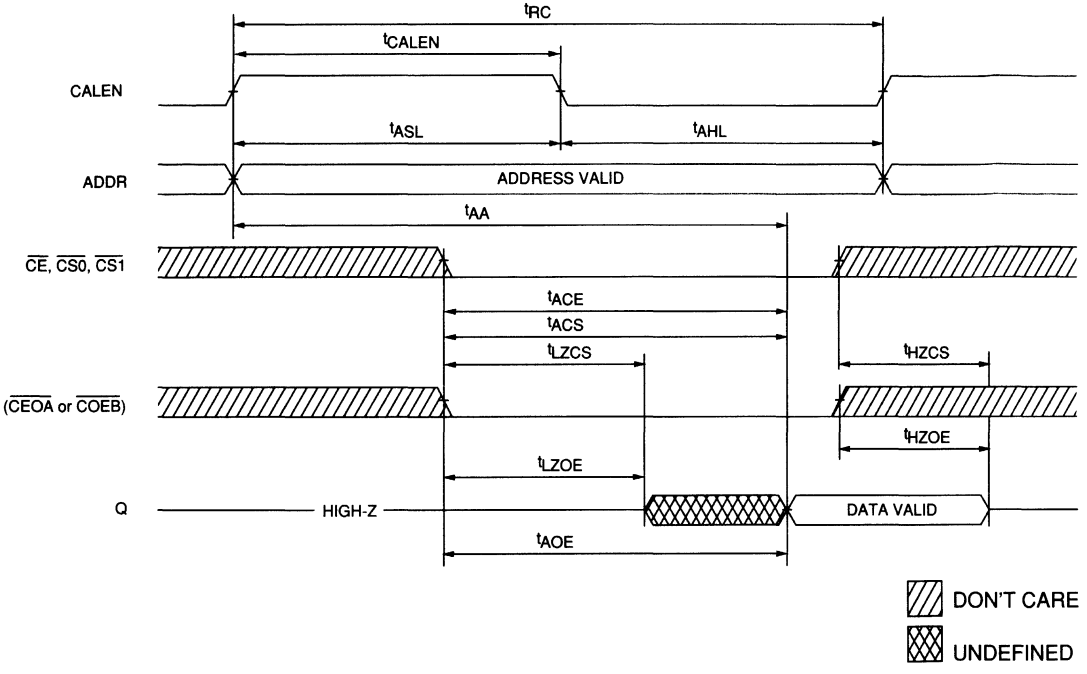
(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

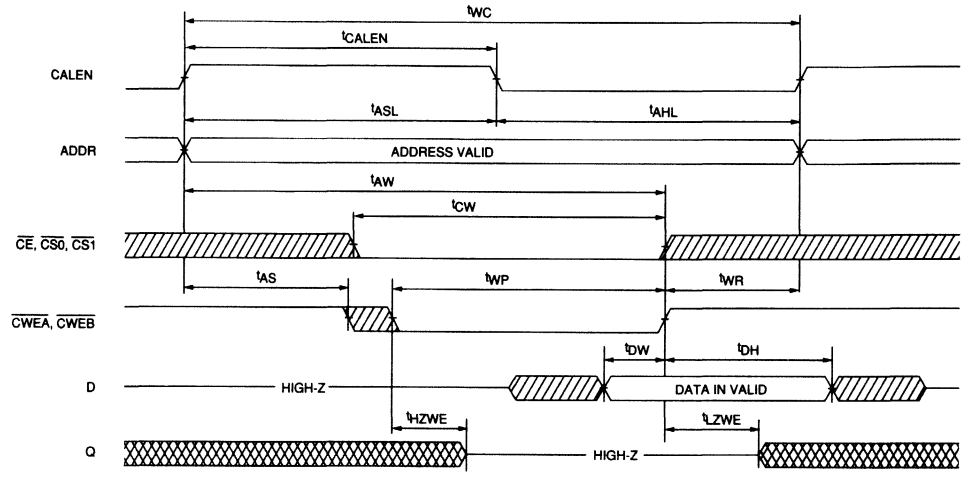


READ CYCLE NO. 3

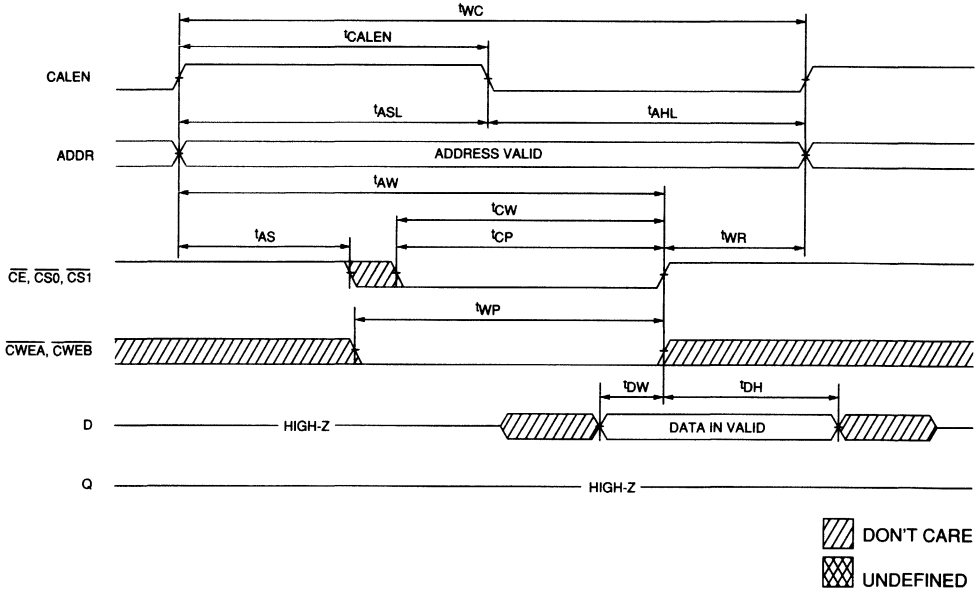
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



LATCHED SRAM

16K x 16 SRAM

WITH ADDRESS/ DATA INPUT LATCHES

FEATURES

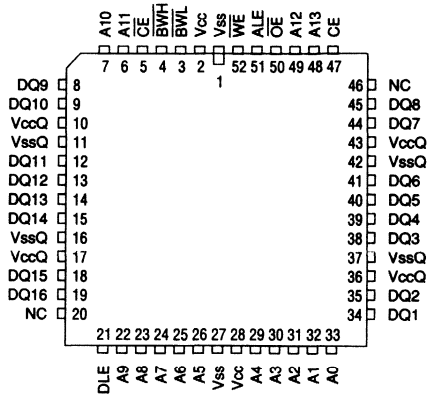
- Fast access times: 12, 15, 20 and 25ns
- Fast $\overline{OE}$: 5, 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Separate data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Address and $\overline{CE}$ input latches

OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 52-pin PLCC — EJ
  - 52-pin PQFP — LG
- Part Number Example: MT5C2516EJ-20

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5C2516 SRAM integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus.

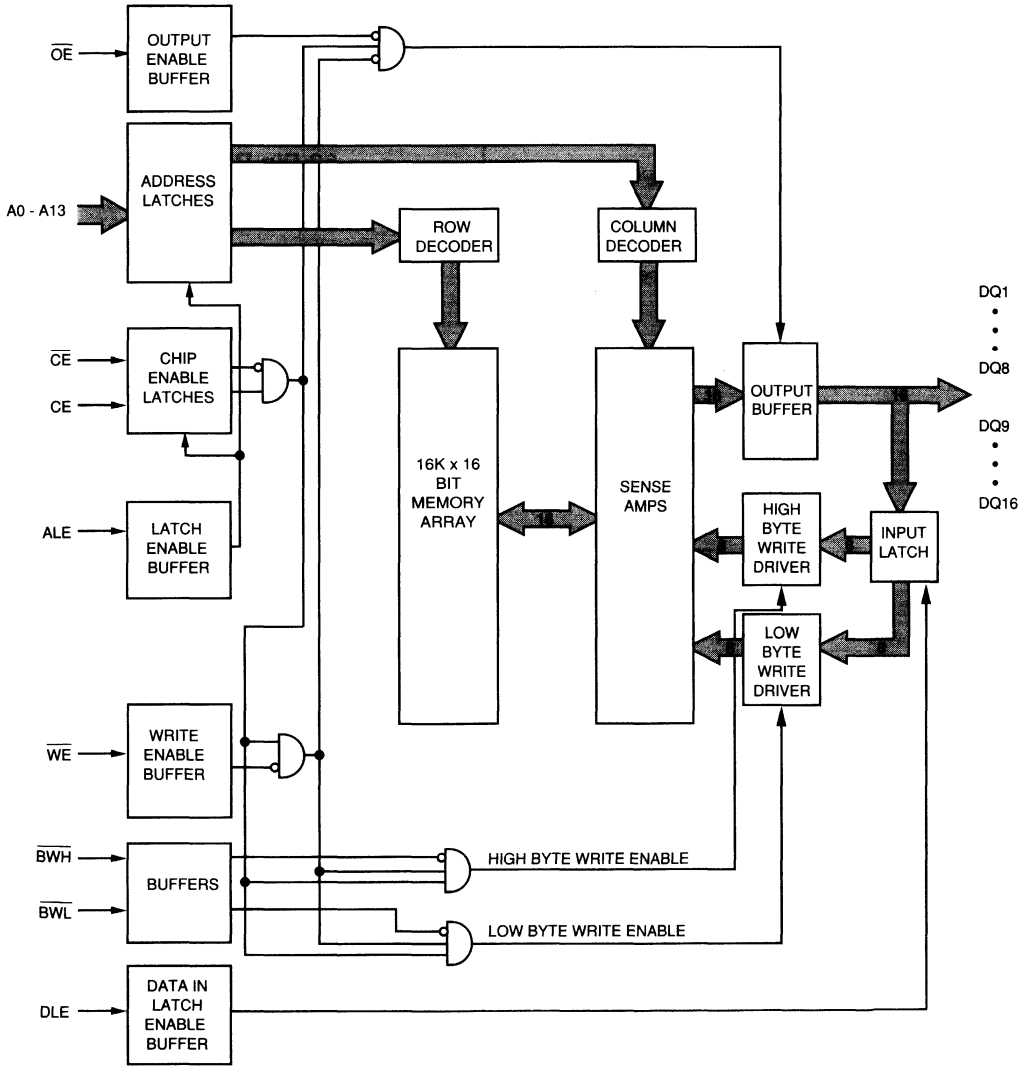
Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8 the lower bits, while $\overline{BWH}$ controls DQ9-DQ16, the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present on the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5C2516 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$, CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
46, 20	NC	Input/ Output	Parity Data I/O: These signals are no connects (NCs). NCs are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the required setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ
Deselected cycle	L	X	X	X	X	X	X	X	High-Z
Deselected cycle	X	H	X	X	X	X	X	X	High-Z
READ	H	L	H	X	X	H	X	H	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16

NOTE:
1. Latched inputs (addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -1V to +7V
Voltage on any pin Relative to V_{SS}/V_{SSQ} .... -1V to V_{CC}+1V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE}$ ≤ V_{IL}; SCE ≥ V_{IH}; f = MAX V_{CC} = MAX; Outputs Open	I_{CC}	150	310	280	250	230	mA	3
Power Supply Current: Standby	f = MAX; SCE ≤ V_{IL}; $\overline{SCE}$ ≥ V_{IH} V_{CC} = MAX; Outputs Open	I_{SB1}	50	80	75	70	65	mA	
	$\overline{SCE}$ ≥ V_{CC} -0.2; SCE ≤ V_{SS} +0.2 V_{CC} = MAX; V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	15	15	15	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	ØJA	60	°C/W	
Thermal resistance – Junction to Case		ØJC	9	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 5V ±10%)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Address Latch											
Latch cycle time	^tLC	12		15		20		25		ns	
Latch HIGH time	^tLEH	5		5		5		5		ns	
Address/Chip Enable setup (latched access)	^tLS	2		2		2		2		ns	
Address/Chip Enable hold	^tLH	3		3		3		3		ns	
Address/Chip Enable setup (unlatched access)	^tLHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		2		2		ns	6, 7
Latch HIGH to output in High-Z	^tHZL	2	8	2	8	2	9	2	10	ns	6, 7
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	6, 7
Chip disable to output in High-Z	^tHZCE	2	8	2	8	2	9	2	10	ns	6, 7
Output Enable access time	^tAOE		5		6		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE	2	5	2	6	2	8	2	10	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		13		15		20		ns	
Address valid to end of write	^tAW	10		13		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	10		13		15		20		ns	
Data setup time	^tDS	4		6		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	6, 7
Write Enable to output in High-Z	^tHZWE	0	8	0	8	0	9	0	10	ns	6, 7
Byte Write Enable setup time	^tBWS	4		6		8		10		ns	
Byte Write Enable hold time	^tBWH	2		2		2		2		ns	
Byte Write disable setup time (Write abort)	^tBWDS	0		0		0		0		ns	
Data setup to DLE LOW	^tDLS	1		1		1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		3		3		ns	9
DLE HIGH to end of write	^tDLW	5		6		8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		0		0		ns	
ALE HIGH setup to Write Enable LOW	^tLWS	0		0		0		0		ns	
ALE HIGH to end of write	^tLW	10		13		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

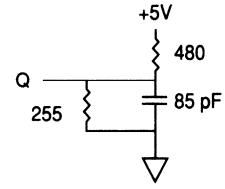


Fig. 1 OUTPUT LOAD EQUIVALENT

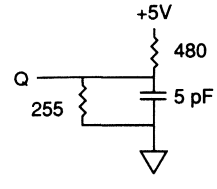
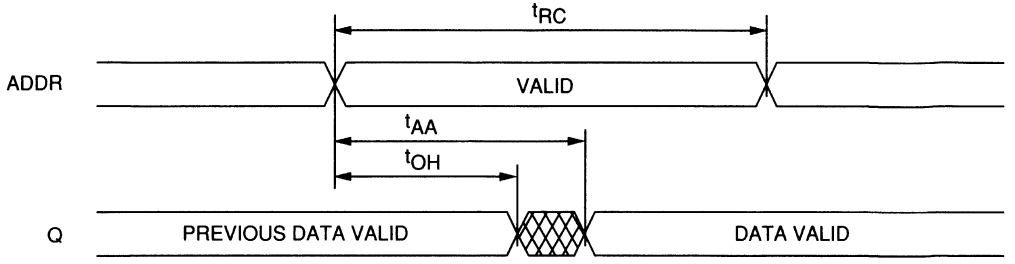


Fig. 2 OUTPUT LOAD EQUIVALENT

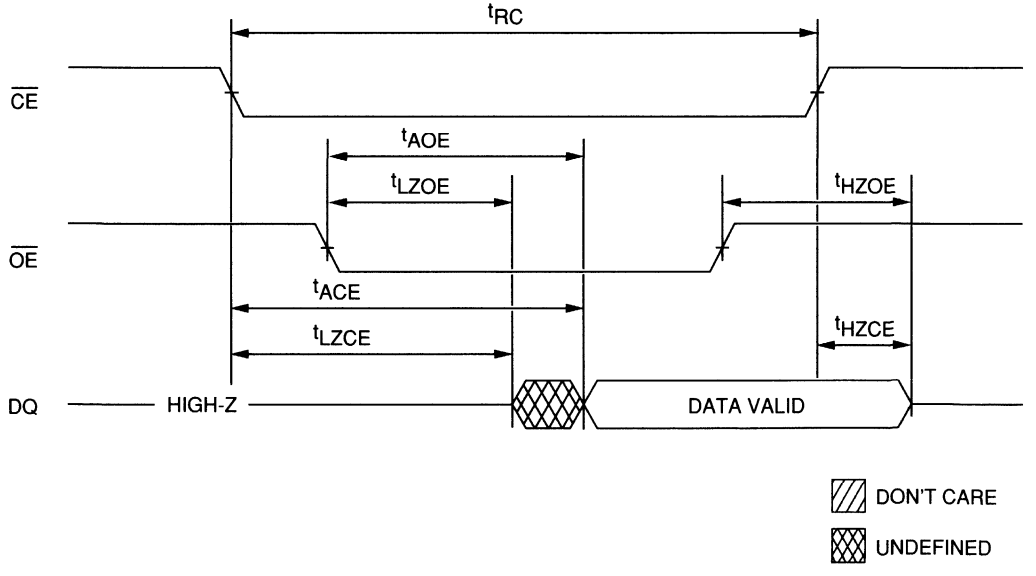
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZOE is less than ^{t}LZOE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable and chip enable can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to, or coincident with, the latest occurring chip enable.
14. CE timing is the same as timing. The wave form is inverted.
15. If output enable is inactive (HIGH) the output will be in High-Z instead of undefined.

READ CYCLE NO. 1 [11, 12]

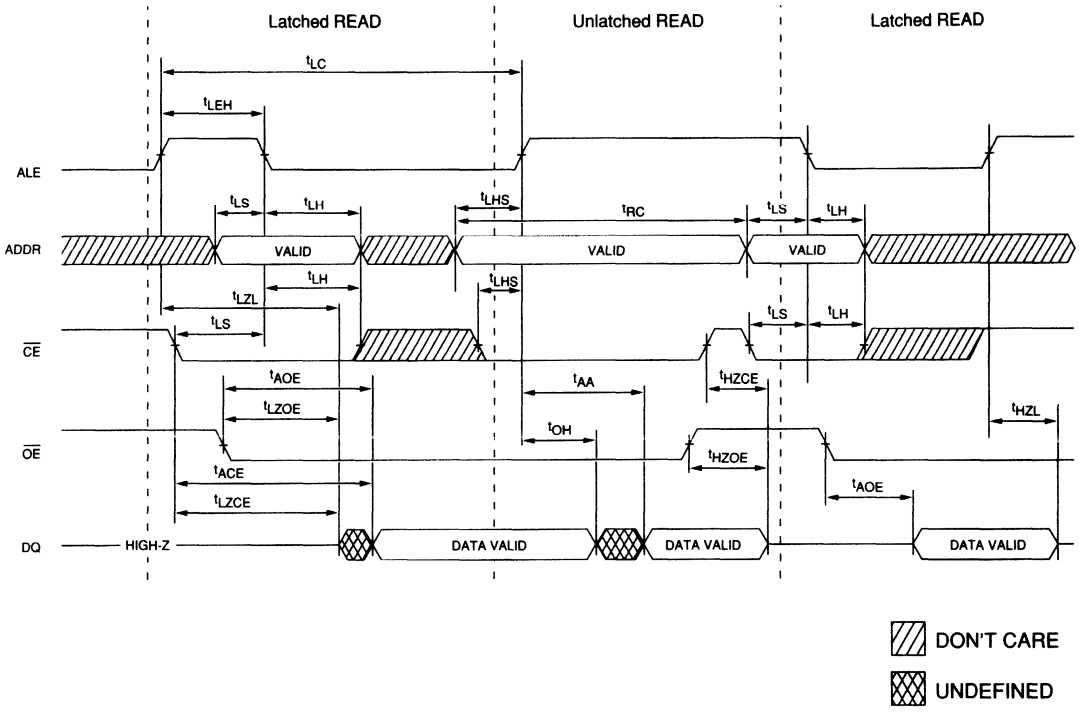


READ CYCLE NO. 2 [7, 11, 13, 14]



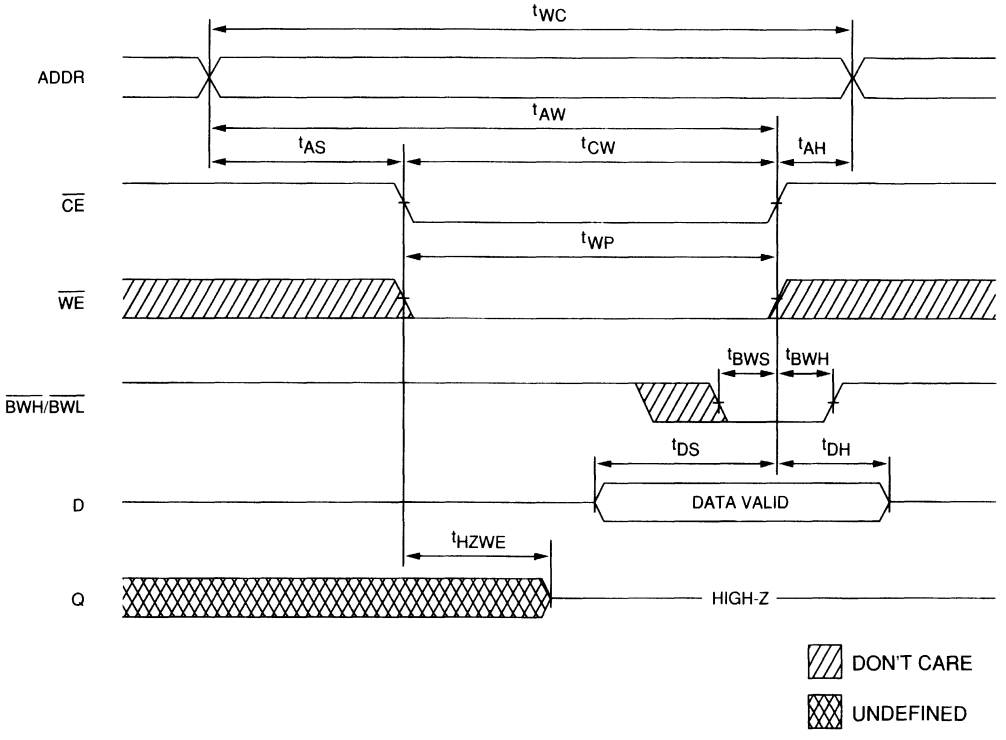
READ CYCLE NO. 3 [7, 11, 14]

(DLE = HIGH)



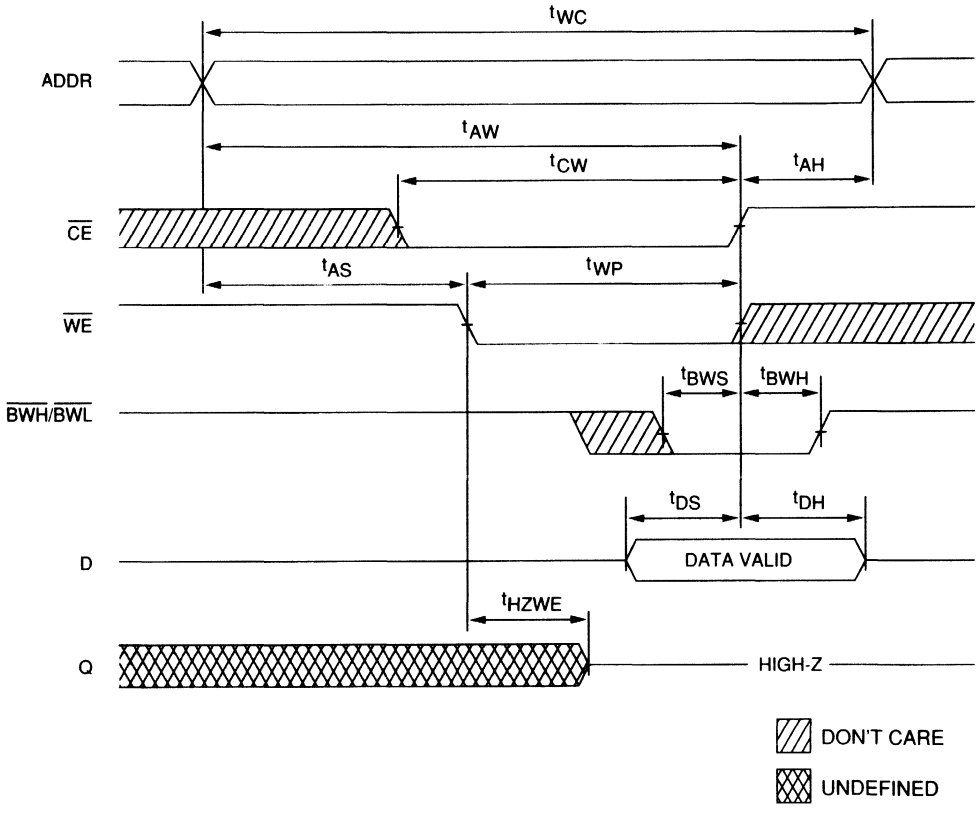
WRITE CYCLE NO. 1 [10, 14, 15]

Chip Enable Controlled
(ALE = DLE = HIGH)

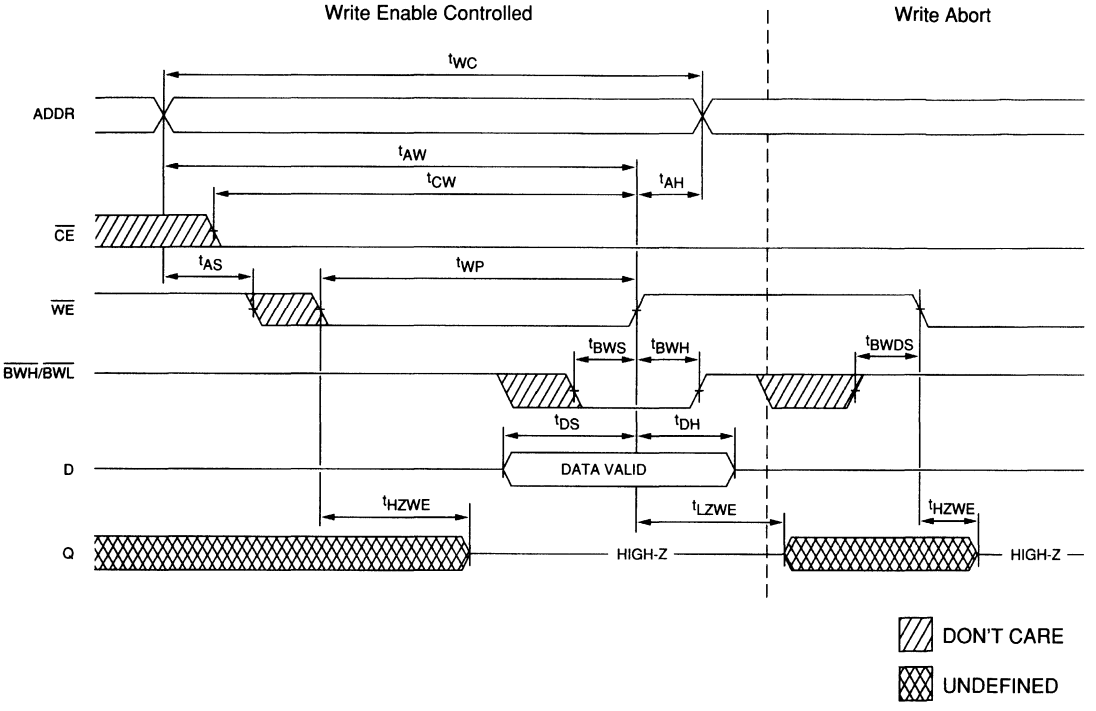


WRITE CYCLE NO. 2 [10, 14, 15]

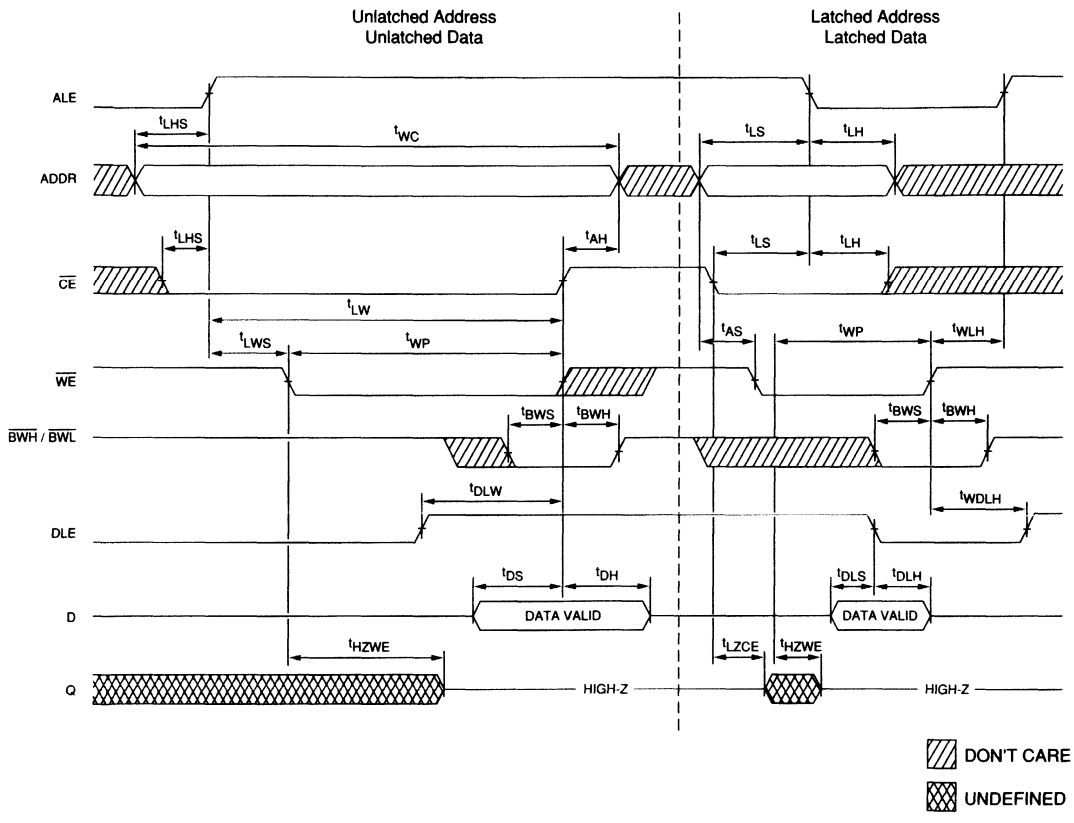
Write Enable Initiated / Chip Enable Terminated
(ALE = DLE = HIGH)



WRITE CYCLE NO. 3 [7, 10, 14, 15]
(ALE = DLE = HIGH)



WRITE CYCLE NO. 4 [7, 10, 14, 15]



CACHE DATA SRAM

SINGLE 8K x 18 SRAM, DUAL 4K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

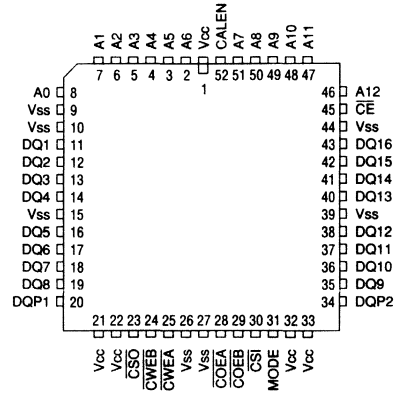
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 20ns, 25ns and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast $\overline{OE}$: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 cache memory controllers
- Parity bits provided for large cache applications such as secondary cache for the 80486 microprocessors

OPTIONS — MARKING

- Timing
  - 20ns access (40 MHz) — -20
  - 25ns access (33 MHz) — -25
  - 35ns access (25 MHz) — -35
- Packages
  - 52-pin PLCC — EJ
  - 52-pin PQFP — LG
- Part Number Example: MT56C0818EJ-25

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-4)



GENERAL DESCRIPTION

The MT56C0818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C0818 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE modes. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

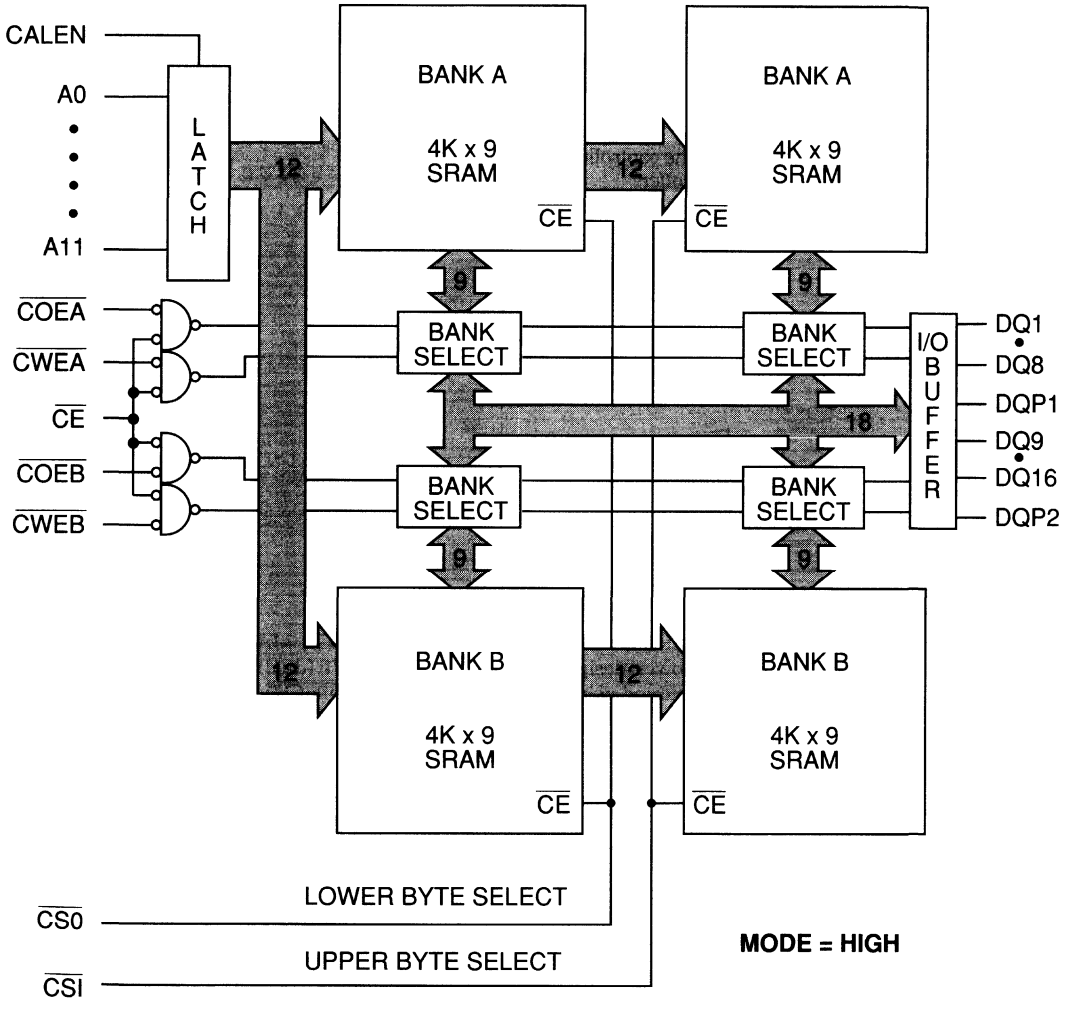
Outputs are enabled on a HIGH-to-LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH-to-LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C0818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

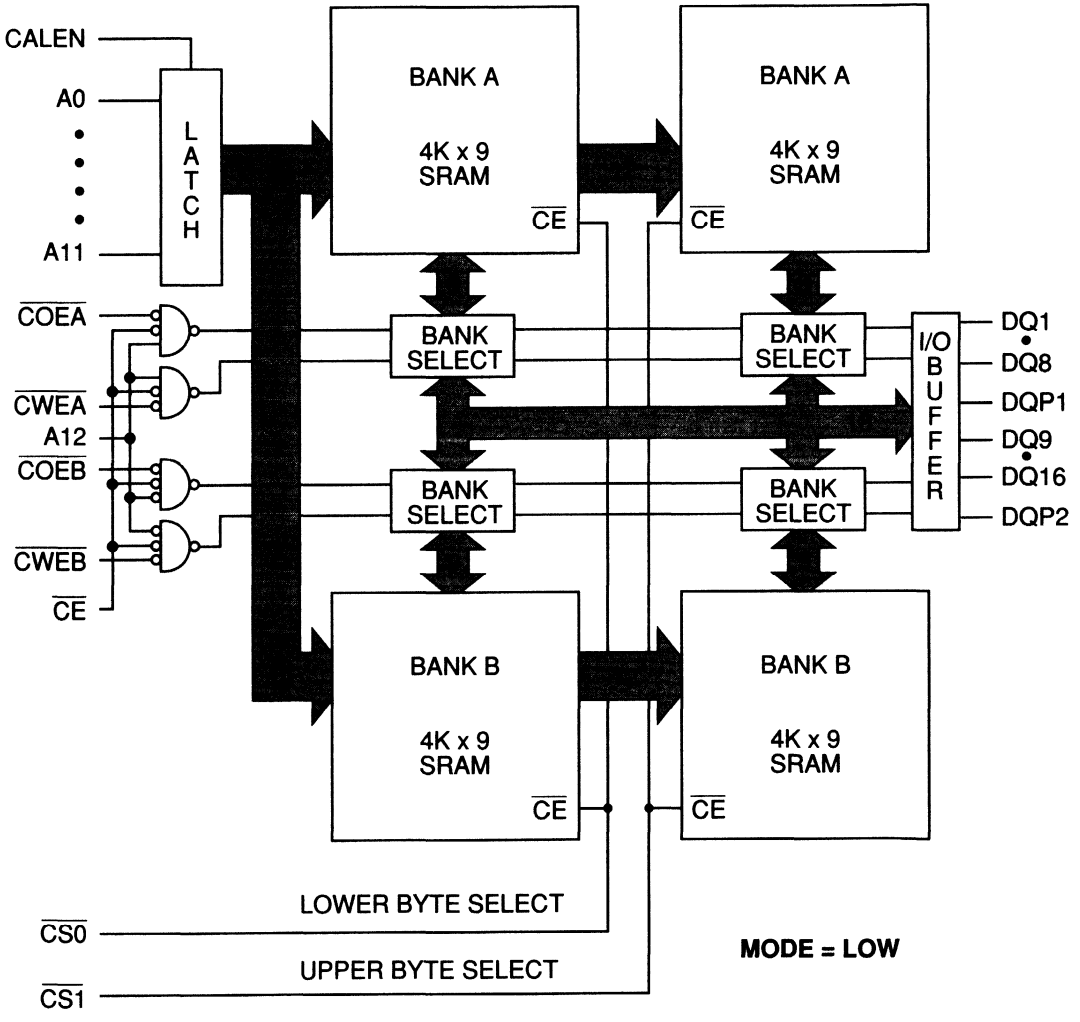
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 18
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order-address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16, 17, 18, 19, 35, 36, 37, 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
20, 34	DQP1 DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
1, 21, 22, 32, 33	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8. DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE:
1. $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		V_{CC}	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	$V_{I/O}$ = GND to V_{CC} Output(s) Disabled	I_{LO}	-5	5	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% duty cycle V_{IN} = GND to V_{CC}	I_{CC1}	130	220	mA	
Power Supply Current: Average Operating Current	50% duty cycle V_{IN} = GND to V_{CC}	I_{CC2}	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ V_{CC} - 0.2V V_{CC} = MAX $V_{IN} \le V_{SS}$ + 0.2V $V_{IN} \ge V_{CC}$ - 0.2V	I_{SB}	2.0	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_{IN}	6	pF	3
Output Capacitance	V_{CC} = 5V	$C_{I/O}$	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	⍬JA	100	°C/W	
Thermal resistance – Junction to Case		⍬JC	45	°C/W	
Thermal resistance mounted on 2" x 3" PC board		⍬JA	70	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C, Vcc = 5V ±5%)

DESCRIPTION	SYM	-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A11)	tAA		20		25		35	ns	
A12 address access time	tA12A		15		17		25	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
A12 address valid to end of write	tA12W	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write Enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
WRITE pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
WRITE recovery time	tWR	0		0		0		ns	
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

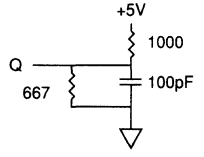


Fig. 1 OUTPUT LOAD EQUIVALENT

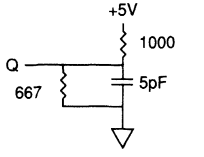


Fig. 2 OUTPUT LOAD EQUIVALENT

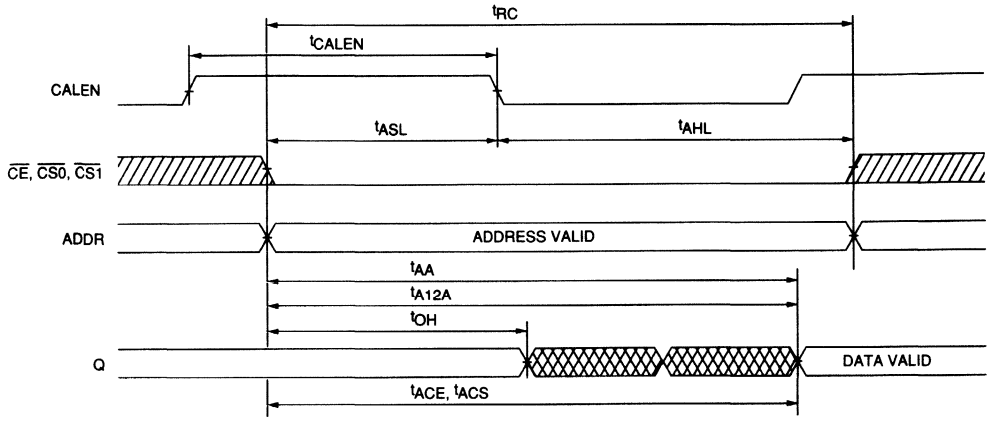
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

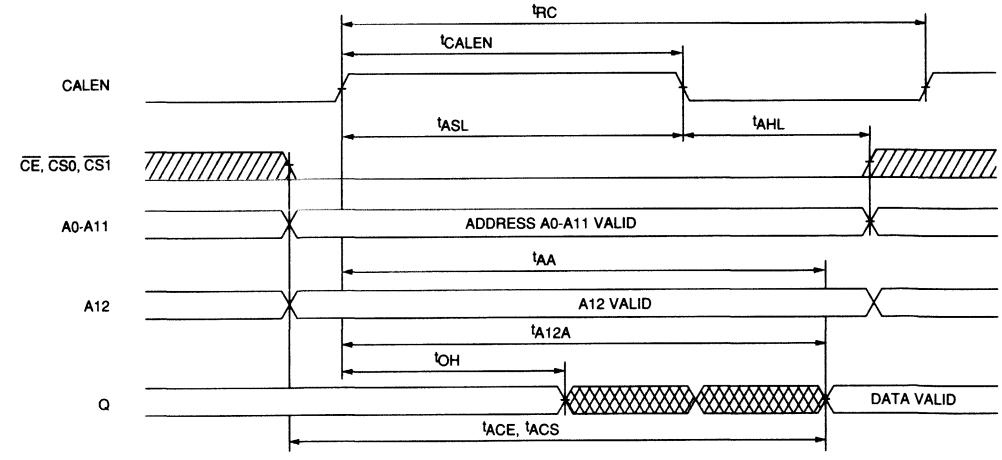
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

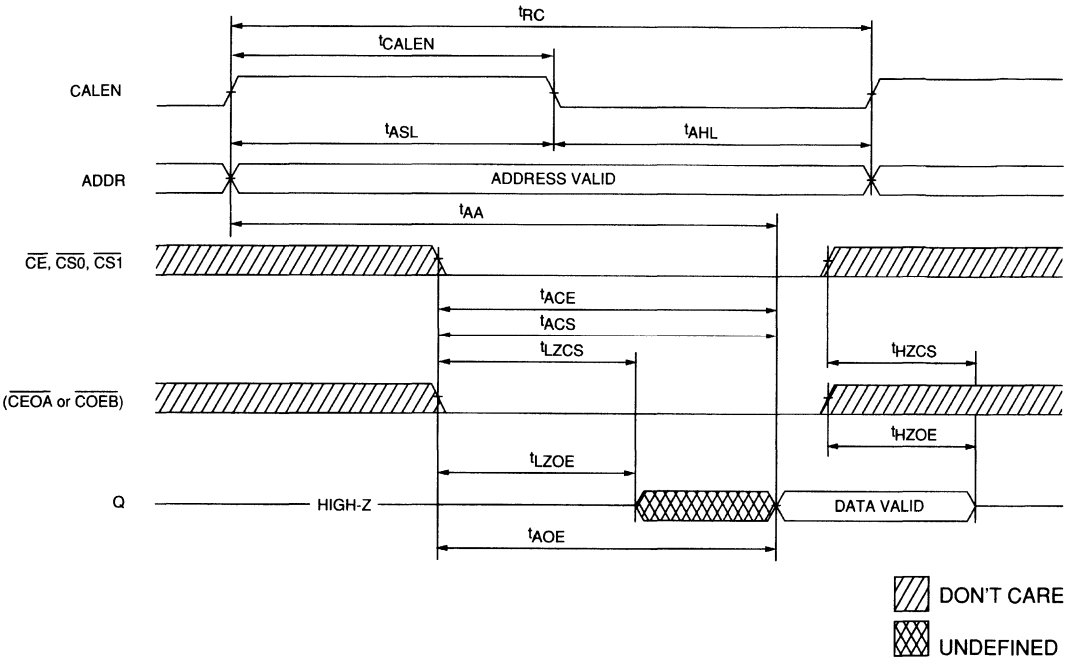


DON'T CARE

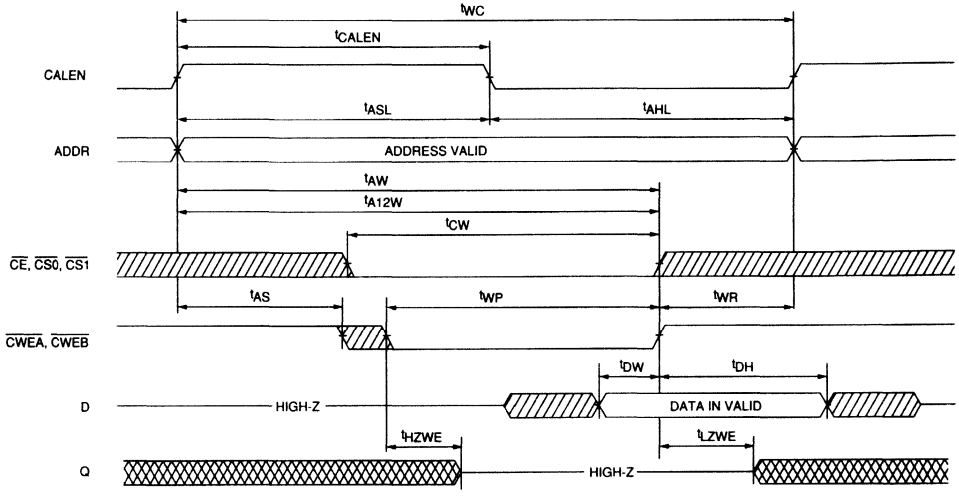
UNDEFINED

READ CYCLE NO. 3

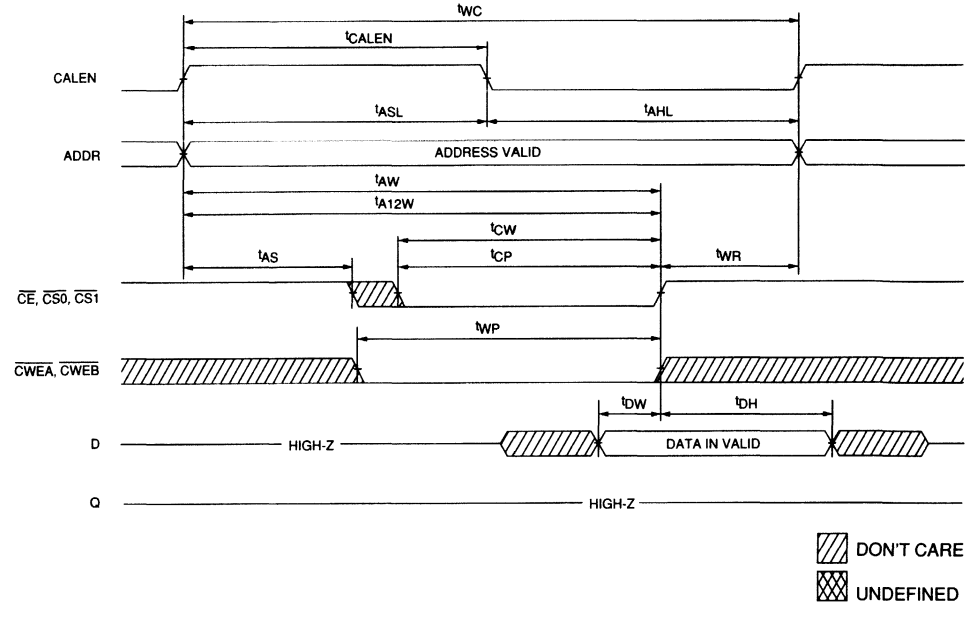
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA SRAM

SINGLE 8K x 18 SRAM, DUAL 4K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

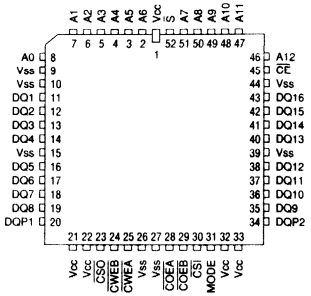
- Automatic WRITE cycle completion
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Automatically controlled input address latches
- Built-in input data latches
- Separate upper and lower Byte Select
- Fast access times: 24ns allows operation with 25 MHz, 33 MHz or 66MHz DX2 microprocessor systems
- Fast $\overline{OE}$: 8ns
- Parity bits provided for large cache applications such as secondary cache for the 80486 microprocessor
- Directly compatible with the Intel 82485 cache controller

OPTIONS — MARKING

- Timing
  24ns access (33 MHz) — -24
- Packages
  52-pin PLCC — EJ
  52-pin PQFP — LG
- Part Number Example: MT56C2818EJ-24

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-4)



GENERAL DESCRIPTION

The MT56C2818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C2818 is a highly integrated cache data memory building block. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Strobe ($\overline{S}$) controls the on-chip address and data latches. During READ and WRITE cycles the address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{S}$. The addresses are "locked out" during this time.

$\overline{S}$ has no effect on the data latch during a READ cycle. During a WRITE cycle, data is latched on the rising edge of $\overline{S}$. The rising edge of $\overline{S}$ also initiates the completion of the WRITE cycle.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations. Power consumption may be reduced by keeping either $\overline{CE}$ inactive (HIGH), or $\overline{CS0}$ and $\overline{CS1}$ inactive (HIGH) as much as possible.

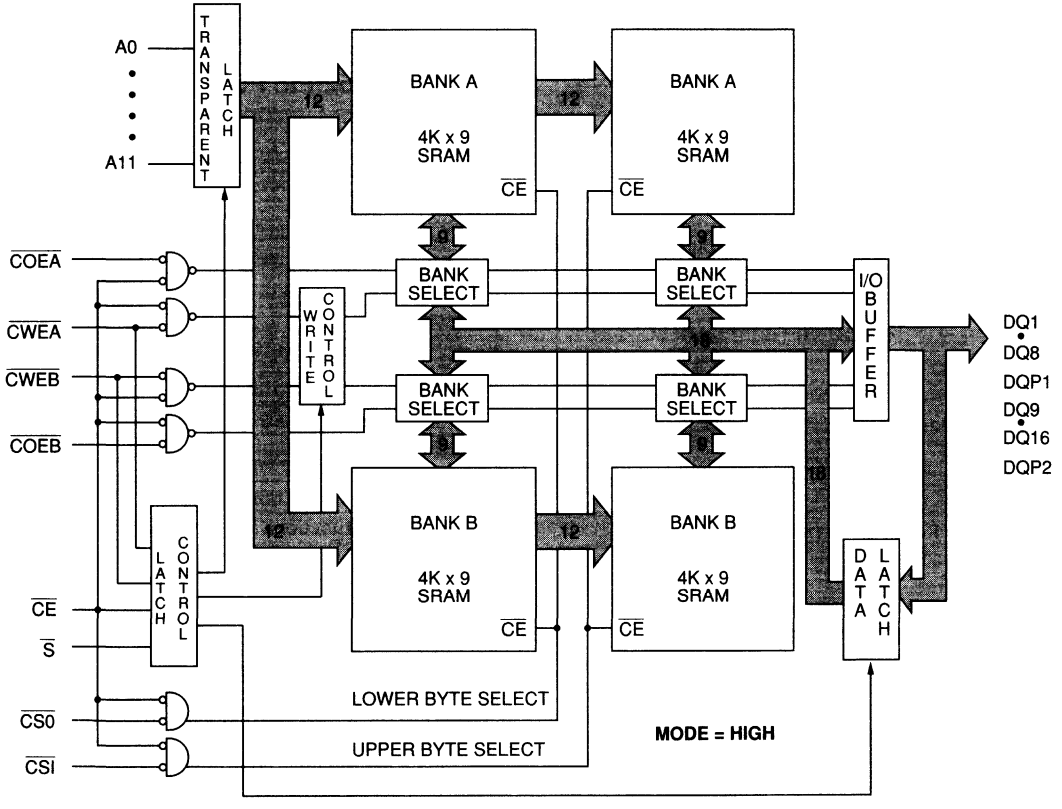
Outputs are enabled on a HIGH-to-LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH-to-LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C2818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

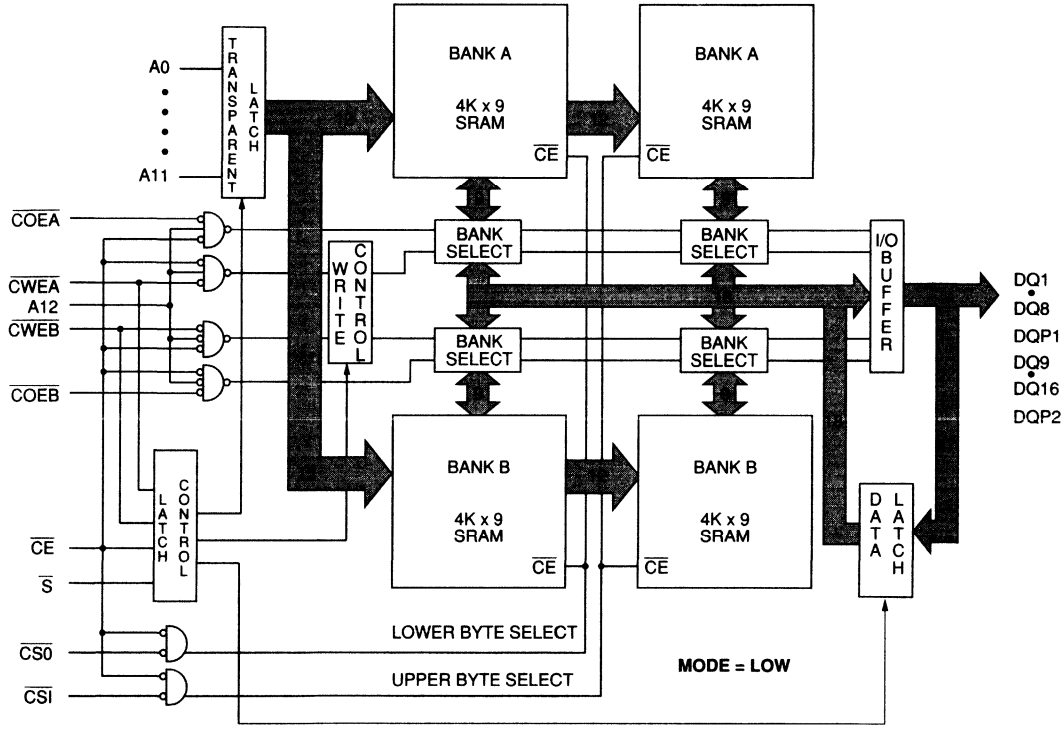
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM
($\overline{COEA}$ = $\overline{COEB}$; $\overline{CWEA}$ = $\overline{CWEB}$)

8K x 18
(DIRECT MAP)



5 VOLT CACHE DATA/LATCHED SRAM

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: A0-A11 are always sampled (transparent latch) except for the time ^{t}WAH and ^{t}ALO following the rising edge of $\overline{S}$.
46	A12	Input	Address Input: This input is the high order-address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	$\overline{S}$	Input	Strobe: This signal controls the internal data and address latches. The address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{S}$. The addresses are "locked out" during this time period. $\overline{S}$ does not affect the data latch during a READ cycle. During a WRITE cycle the rising edge of $\overline{S}$ latches the data. The rising edge also initiates the termination of the WRITE cycle.
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled. Significant power savings can be achieved by keeping $\overline{CS0}$ and $\overline{CS1}$ inactive as much as possible.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank "A" and bank "B" for READ or WRITE operations. Significant power savings can be achieved by keeping $\overline{CE}$ inactive as much as possible.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank "A" or "B". Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
20, 34	DQP1, DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
11, 12, 13, 14, 16, 17, 18, 19, 35, 36, 37, 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8, DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

TRUTH TABLE

8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: When mode pin is LOW, $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	Vcc +0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	$V_{I/O}$ = GND to Vcc Output(s) Disabled	I_{LO}	-5	5	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS		SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty Cycle V_{IN} = GND to Vcc		I_{CC1}	145	220	mA	
Power Supply Current: Average Operating Current	50% Duty Cycle V_{IN} = GND to Vcc		I_{CC2}	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS1}$ ≥ Vcc -0.2V and $\overline{CS0}$ ≥ Vcc -0.2V Vcc = MAX; f = 0 V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V	CE ≤ Vcc -0.2V	I_{SB1}	2.0	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 5V	C_I	6	pF	3
Input/Output Capacitance		$C_{I/O}$	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	ØJA	100	°C/W	
Thermal resistance – Junction to Case		ØJC	45	°C/W	
Thermal resistance mounted on 2" x 3" PC board		ØJA	70	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 8) ($0°C \le T_A \le +70°C$, V_{CC} = 5V ±5%)

DESCRIPTION	SYM	-24 MIN	-24 MAX	UNITS	NOTES
READ Cycle					
READ cycle time	tRC	24		ns	4, 5
Address access time (A0-A11)	tAA		24	ns	4, 5
A12 address access time	tA12A		17	ns	
Chip Enable access time	tACE		23	ns	
Chip Select access time	tACS		23	ns	
Output Enable access time	tAOE		8	ns	
Output hold from address change	tOH	3		ns	
Chip Select/Chip Enable to output Low-Z	tLZCS	3		ns	
Output Enable to output Low-Z	tLZOE	2		ns	
Chip deselect/chip disable to output High-Z	tHZCS		15	ns	6
Output disable to output High-Z	tHZOE	2	10	ns	6
WRITE Cycle					
WRITE cycle time	tWC	24		ns	
$\overline{S}$ strobe HIGH level width	tSWH	11		ns	7
$\overline{S}$ strobe LOW level width	tSWL	11		ns	7
WRITE, Chip Enable/Write Enable to $\overline{S}$ strobe setup	tWSS	10		ns	7
WRITE, Chip Enable/Write Enable to $\overline{S}$ strobe hold	tWSH	2		ns	7
WRITE, address setup to $\overline{S}$ strobe	tWAS	13		ns	7
WRITE, address hold to $\overline{S}$ strobe	tWAH	2		ns	7
Address latch closed	tALO		8	ns	7
Chip Select to $\overline{S}$ strobe setup	tCSS	13		ns	7
Chip Select to $\overline{S}$ strobe hold	tCSH	2		ns	7
Data to $\overline{S}$ strobe setup	tDSS	5		ns	7
Data to $\overline{S}$ strobe hold	tDSH	3		ns	7
Write Enable to output in High-Z	tHZWE		15	ns	6
Write Enable to output in Low-Z	tLZWE	8		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load (see notes 6 and 8).	Reference Figure 1

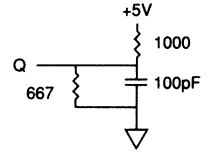


Fig. 1 OUTPUT LOAD EQUIVALENT

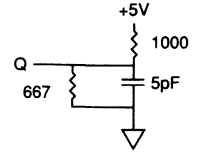


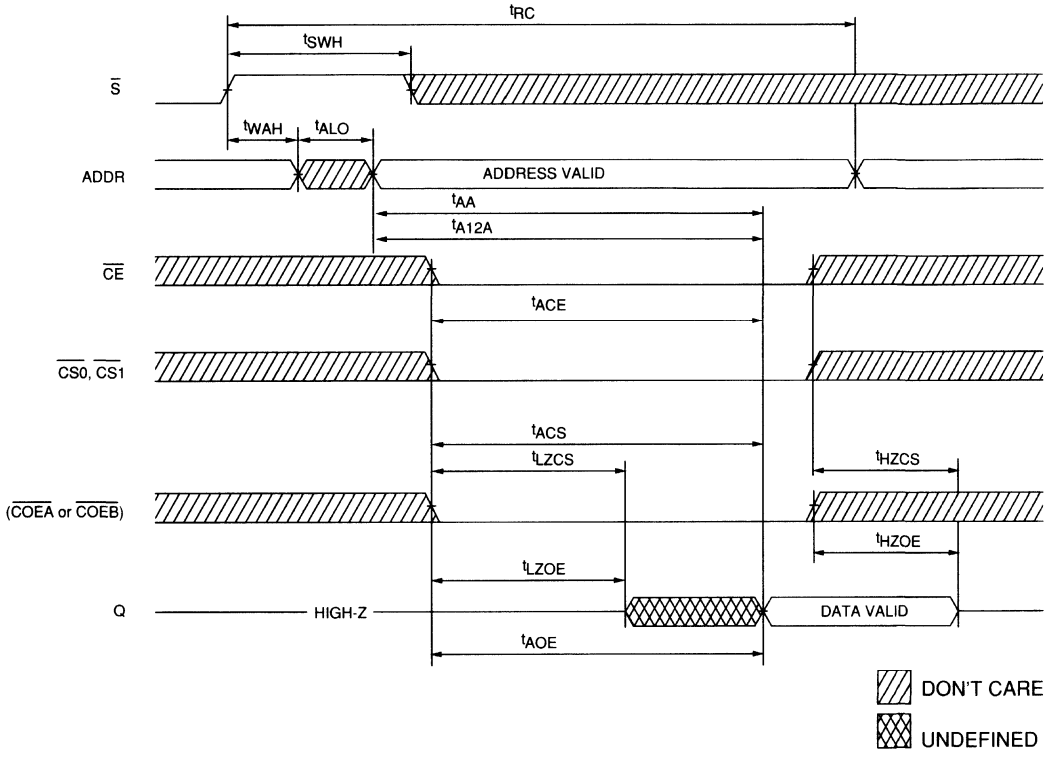
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. Self-timed WRITE parameter.
8. Output timing should be derated by 1ns for each additional 30pf of capacitive loading.

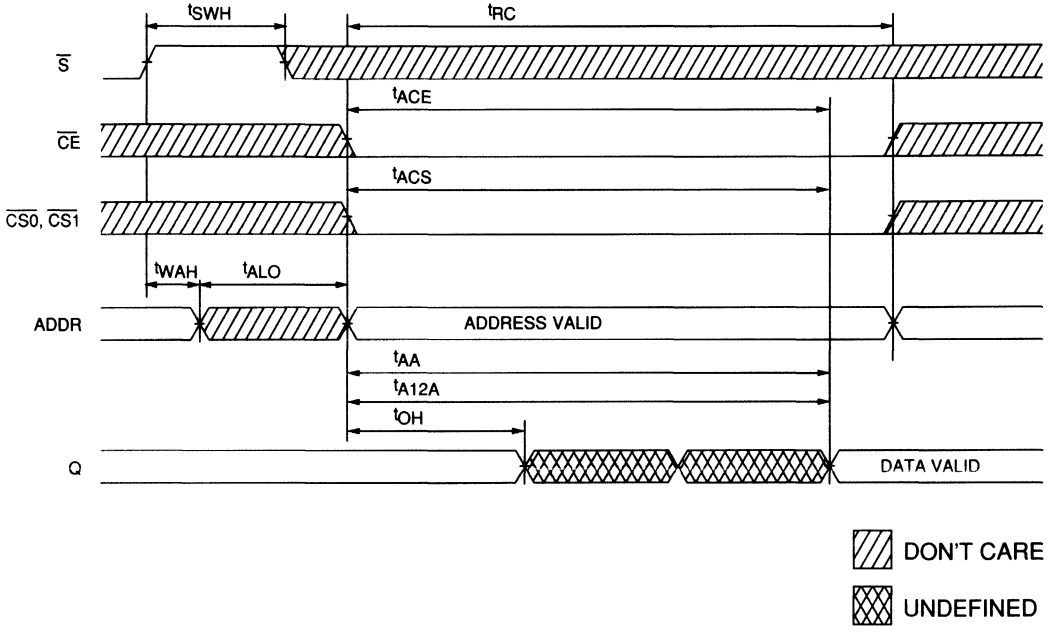
READ CYCLE NO. 1

($\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH})

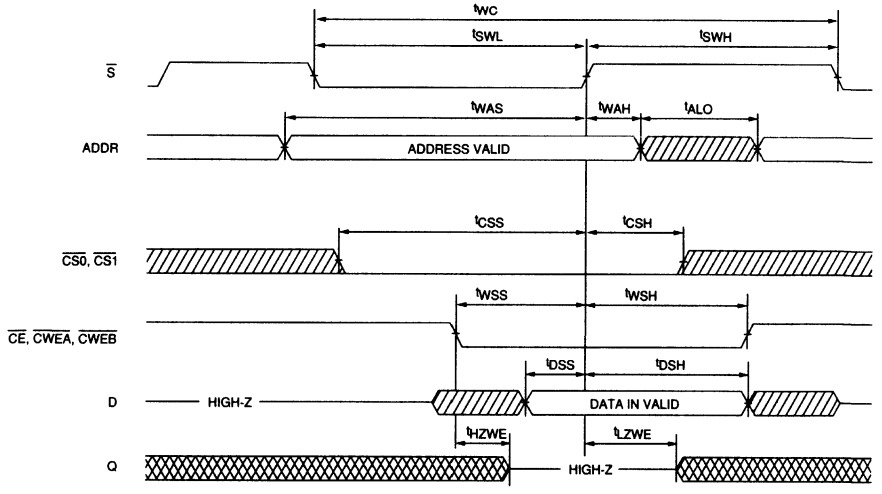


READ CYCLE NO. 2

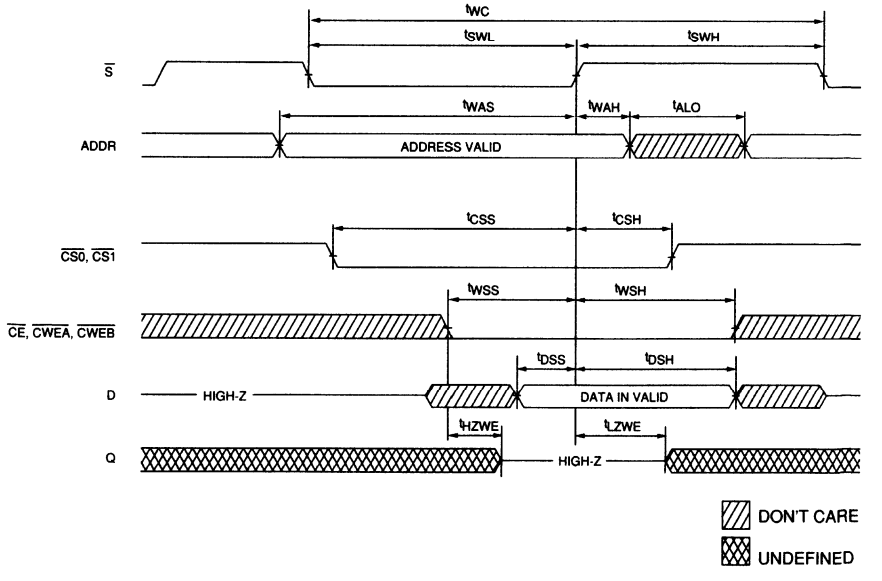
($\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL})
($\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH})



WRITE CYCLE NO. 1
(Write Enable/Chip Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA SRAM

SINGLE 8K x 18 SRAM, DUAL 4K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

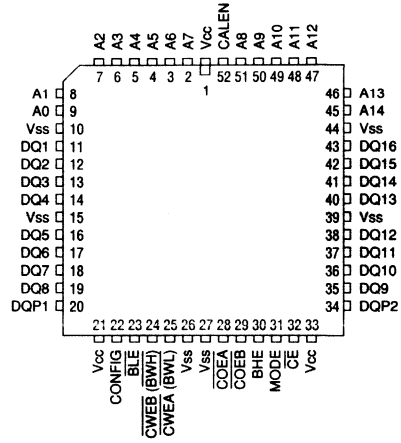
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches (A0-A12)
- Separate upper and lower Byte Select
- Fast access times: 20, 25 and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast $\overline{OE}$: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 and 80486 cache memory controllers
- Parity bits provided for large cache applications such as secondary cache for the 80486 microprocessors

OPTIONS — MARKING

- Timing
  - 20ns access (40 MHz) — -20
  - 25ns access (33 MHz) — -25
  - 35ns access (25 MHz) — -35
- Packages
  - 52-pin PLCC — EJ
  - 52-pin PQFP — LG
- Part Number Example: MT56C3818EJ-25

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-4)



GENERAL DESCRIPTION

The MT56C3818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C3818 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

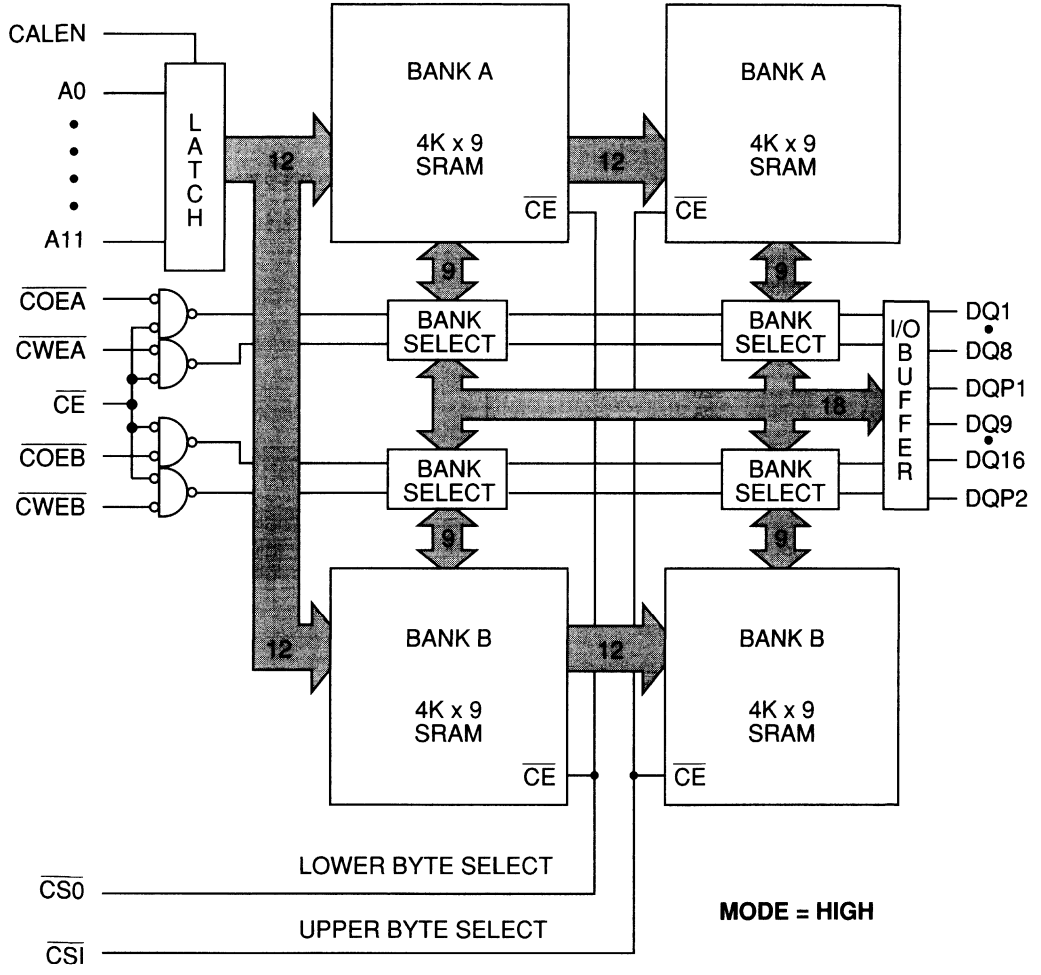
Outputs are enabled on a HIGH-to-LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH-to-LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C3818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

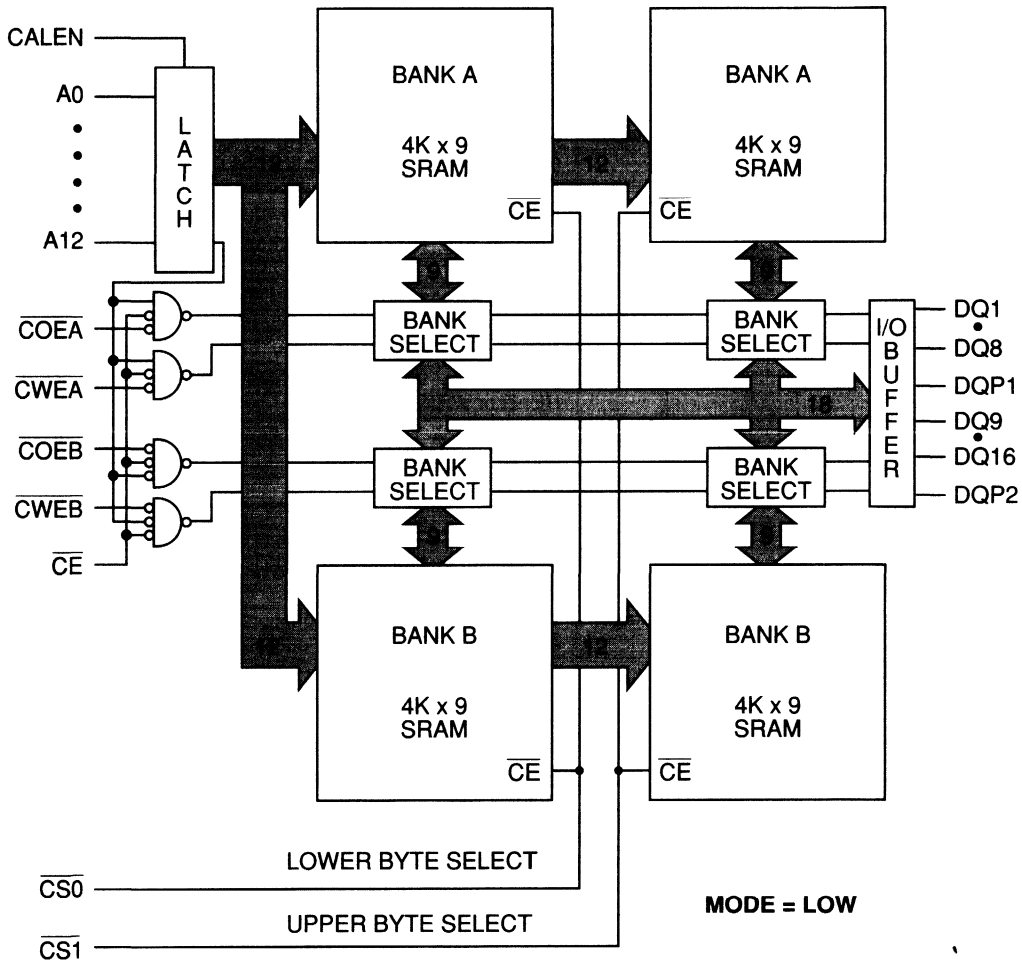
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 18
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order-address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration. This input is latched by the negative edge of CALEN.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A12).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16, 17, 18, 19, 35, 36, 37, 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
20, 34	DQP1 DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
1, 21, 22, 32, 33	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8,DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1 -DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8, DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: 1. $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		V_{CC}	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	V_{CC} +0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	$V_{I/O}$ = GND to Vcc Output(s) Disabled	I_{LO}	-5	5	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty Cycle V_{IN} = GND to Vcc	I_{CC1}	130	220	mA	
Power Supply Current: Average Operating Current	50% Duty Cycle V_{IN} = GND to Vcc	I_{CC2}	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc -0.2V Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V	I_{SB}	2.0	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	3
Output Capacitance	Vcc = 5V	$C_{I/O}$	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	⍜JA	100	°C/W	
Thermal resistance – Junction to Case		⍜JC	45	°C/W	
Thermal resistance mounted on 2" x 3" PC board		⍜JA	70	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C, Vcc = 5V ±5%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A12)	tAA		20		25		35	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write Enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
WRITE pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
WRITE recovery time	tWR	0		0		0		ns	
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

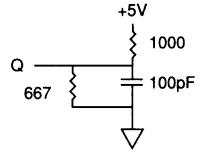


Fig. 1 OUTPUT LOAD EQUIVALENT

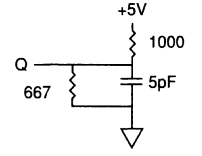


Fig. 2 OUTPUT LOAD EQUIVALENT

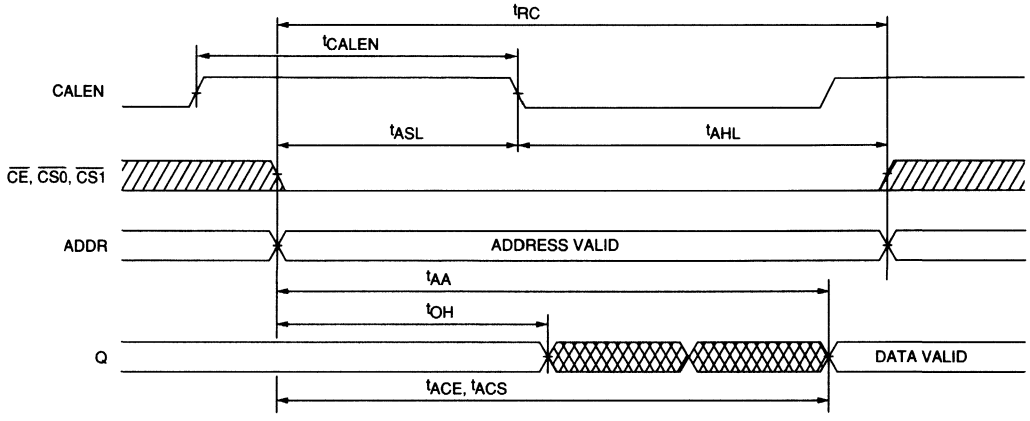
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

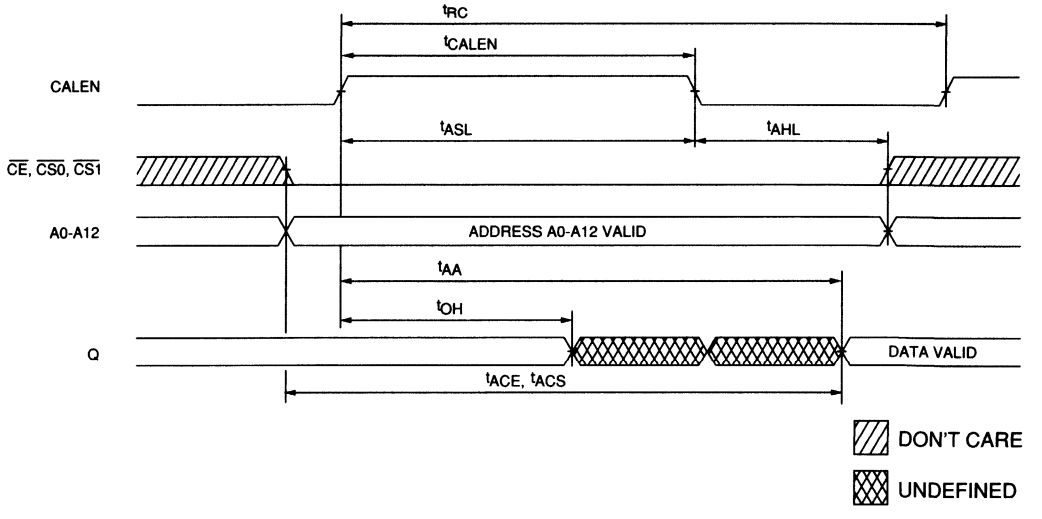
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

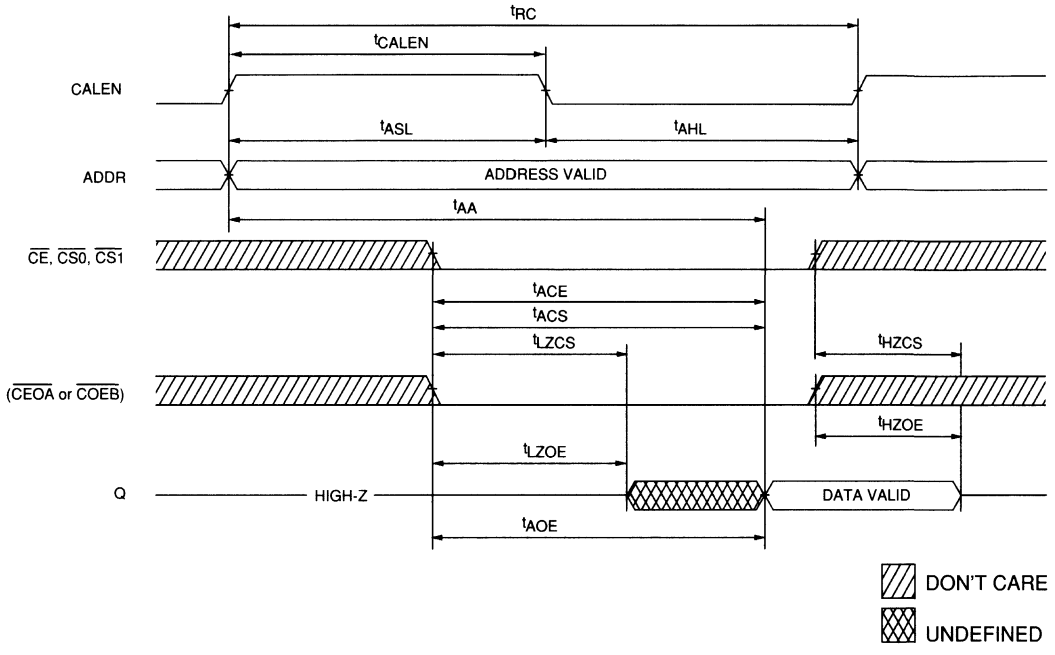
(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

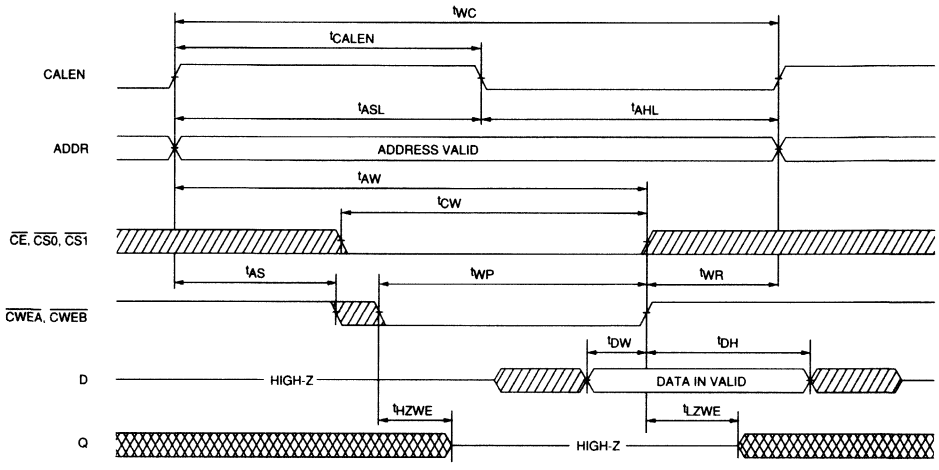


READ CYCLE NO. 3

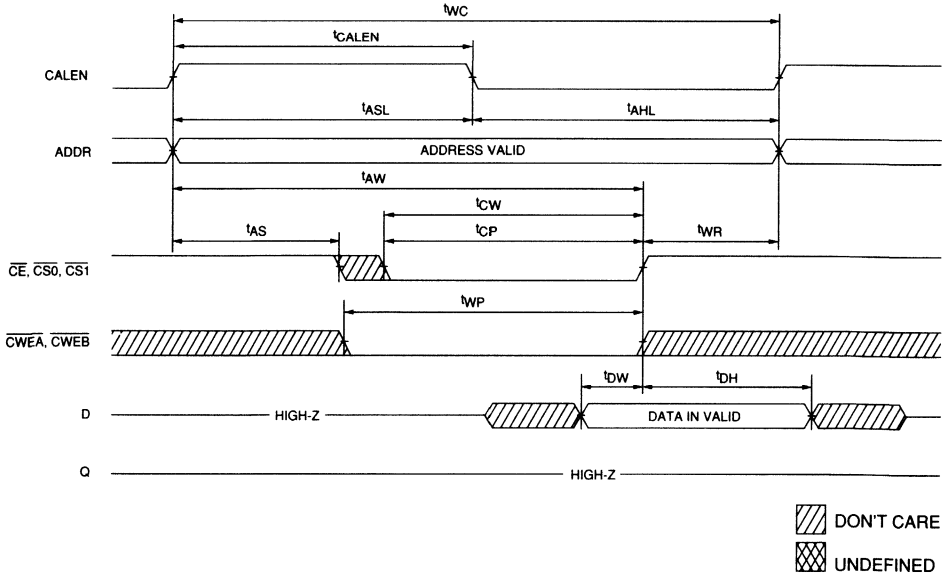
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



LATCHED SRAM

16K x 18 SRAM

WITH ADDRESS/ DATA INPUT LATCHES

FEATURES

- Fast access times: 12, 15, 20 and 25ns
- Fast Output Enable: 5, 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Separate data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Parity bits
- Address and $\overline{CE}$ input latches

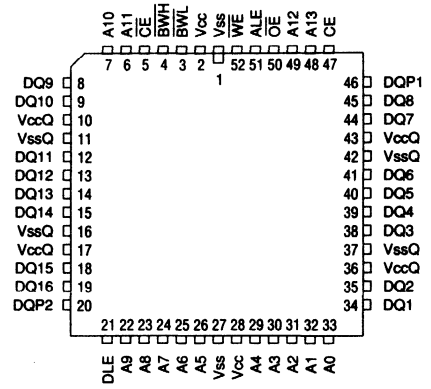
OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

- Part Number Example: MT5C2818EJ-12

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5C2818 SRAM integrates a 16K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus. Parity bits are provided for added data integrity.

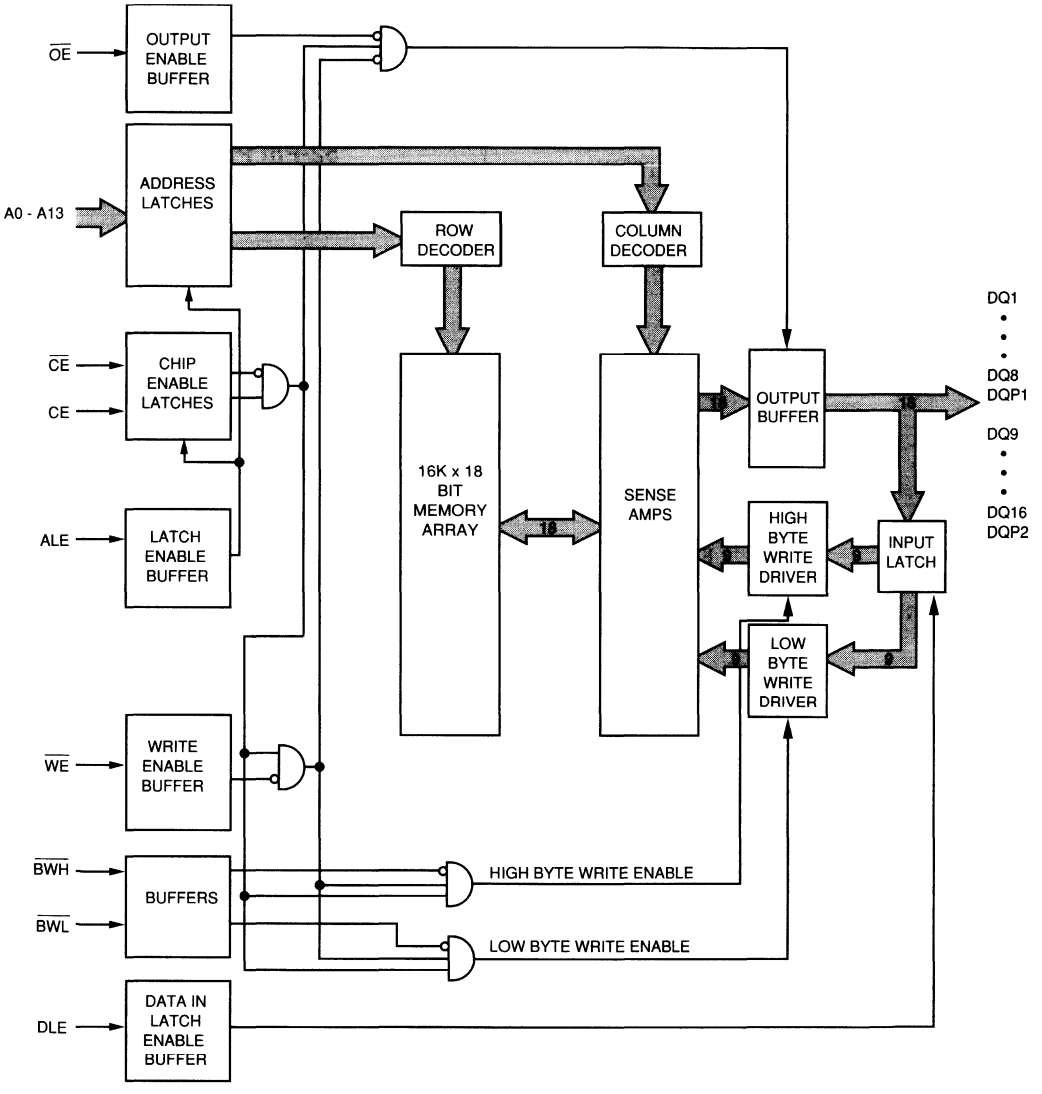
Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8 and DQP1, the lower bits, while $\overline{BWH}$ controls DQ9-DQ16 and DQP2, the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present in the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5C2818 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$, CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
46, 20	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ	DQP
Deselected cycle	L	X	X	X	X	X	X	X	High-Z	High-Z
Deselected cycle	X	H	X	X	X	X	X	X	High-Z	High-Z
READ	H	L	H	X	X	H	X	H	High-Z	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16	QP1, QP2
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16	QP1, QP2
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16	DP1, DP2
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16	DP1, DP2
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16	DP2
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16	DP2

NOTE:
1. Latched inputs (addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -1V to +7V
Voltage on any pin Relative to V_{SS}/V_{SSQ} .... -1V to V_{CC}+1V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE}$ ≤ V_{IL}; SCE ≥ V_{IH}; f = MAX V_{CC} = MAX; Outputs Open	I_{CC}	150	310	280	250	230	mA	3
Power Supply Current: Standby	f = MAX; SCE ≤ V_{IL}; $\overline{SCE}$ ≥ V_{IH} V_{CC} = MAX; Outputs Open	I_{SB1}	50	80	75	70	65	mA	
	$\overline{SCE}$ ≥ V_{CC} -0.2; SCE ≤ V_{SS} +0.2 V_{CC} = MAX; V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	15	15	15	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient Suspended in Air	Still Air	ØJA	60	°C/W	
Thermal resistance – Junction to Case		ØJC	9	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = V_{CC}Q = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Address Latch											
Latch cycle time	^tLC	12		15		20		25		ns	
Latch HIGH time	^tLEH	5		5		5		5		ns	
Address/Chip Enable setup (latched access)	^tLS	2		2		2		2		ns	
Address/Chip Enable hold	^tLH	3		3		3		3		ns	
Address/Chip Enable setup (unlatched access)	^tLHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		2		2		ns	6, 7
Latch HIGH to output in High-Z	^tHZL	2	8	2	8	2	9	2	10	ns	6, 7
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	6, 7
Chip disable to output in High-Z	^tHZCE	2	8	2	8	2	9	2	10	ns	6, 7
Output Enable access time	^tAOE		5		6		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE	2	5	2	6	2	8	2	10	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		13		15		20		ns	
Address valid to end of write	^tAW	10		13		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	10		13		15		20		ns	
Data setup time	^tDS	4		6		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	6, 7
Write Enable to output in High-Z	^tHZWE	0	8	0	8	0	9	0	10	ns	6, 7
Byte Write Enable setup time	^tBWS	4		6		8		10		ns	
Byte Write Enable hold time	^tBWH	2		2		2		2		ns	
Byte Write disable setup time (Write abort)	^tBWDS	0		0		0		0		ns	
Data setup to DLE LOW	^tDLS	1		1		1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		3		3		ns	9
DLE HIGH to end of write	^tDLW	5		6		8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		0		0		ns	
ALE HIGH setup to Write Enable LOW	^tLWS	0		0		0		0		ns	
ALE HIGH to end of write	^tLW	10		13		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

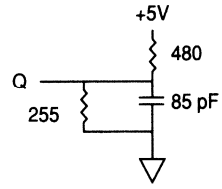


Fig. 1 OUTPUT LOAD EQUIVALENT

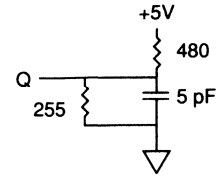
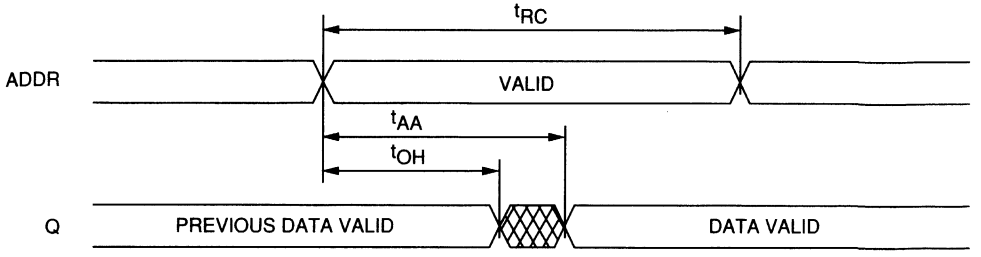


Fig. 2 OUTPUT LOAD EQUIVALENT

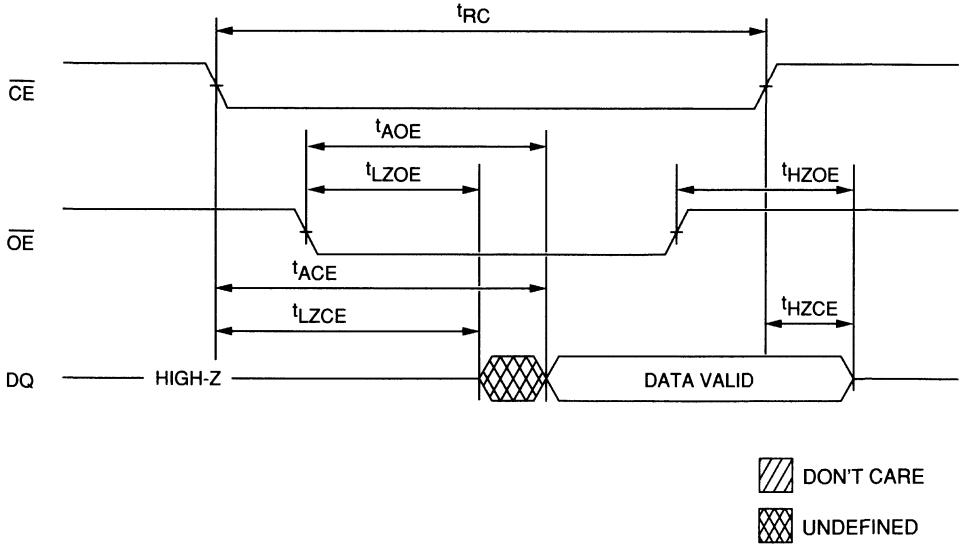
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZOE is less than ^{t}LZOE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable and chip enable can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to, or coincident with, the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.
15. If output enable is inactive (HIGH), the output will be in High-Z instead of undefined.

READ CYCLE NO. 1 [11, 12]

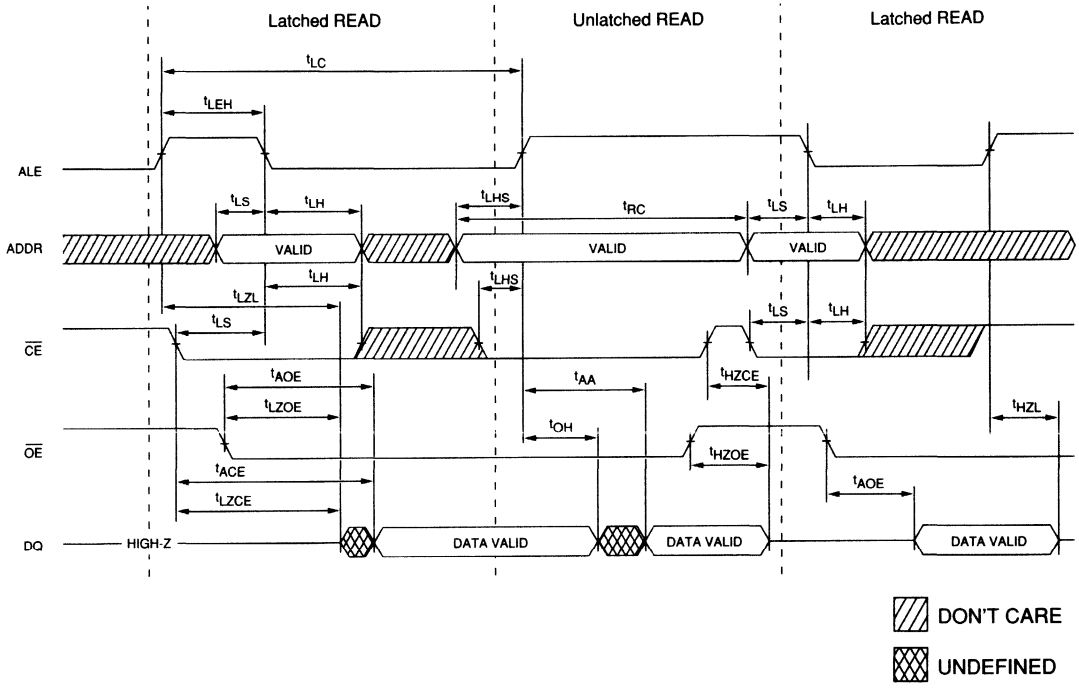


READ CYCLE NO. 2 [7, 11, 13, 14]



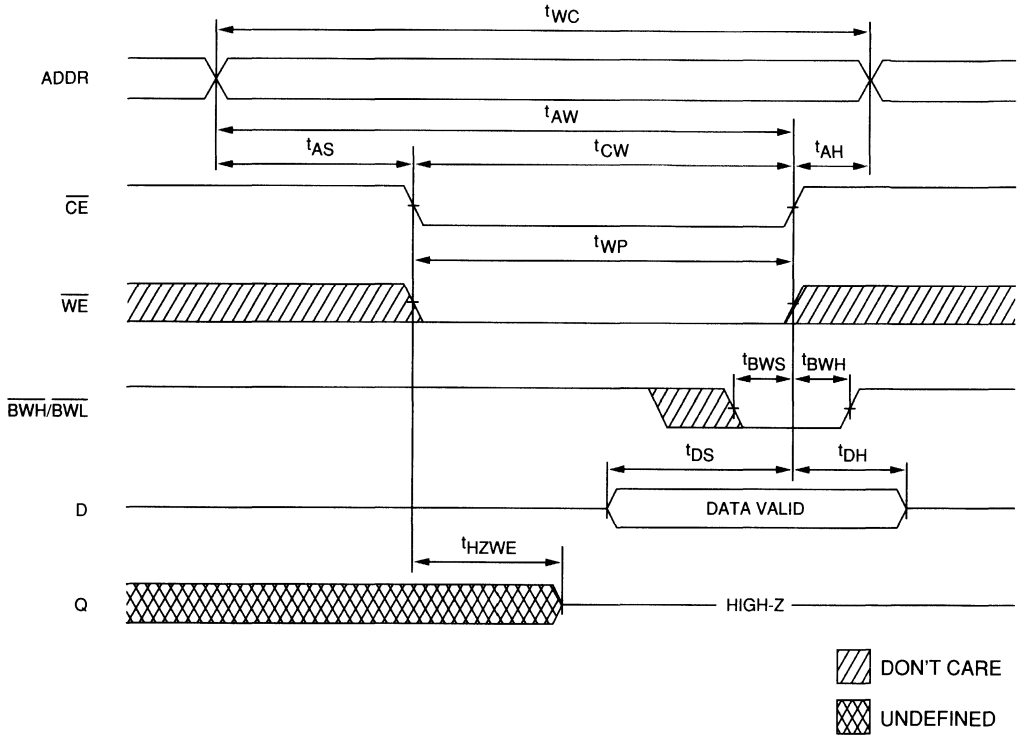
READ CYCLE NO. 3 [7, 11, 14]

(DLE = HIGH)



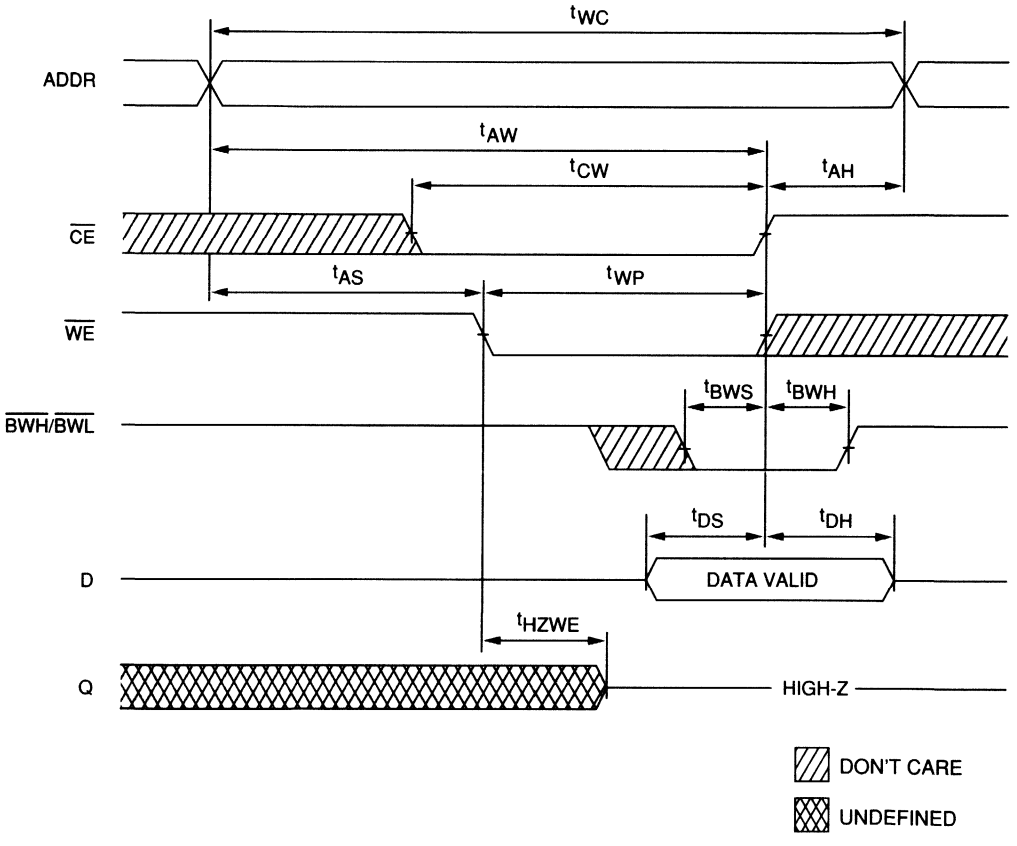
WRITE CYCLE NO. 1 [10, 14, 15]

Chip Enable Controlled
(ALE = DLE = HIGH)

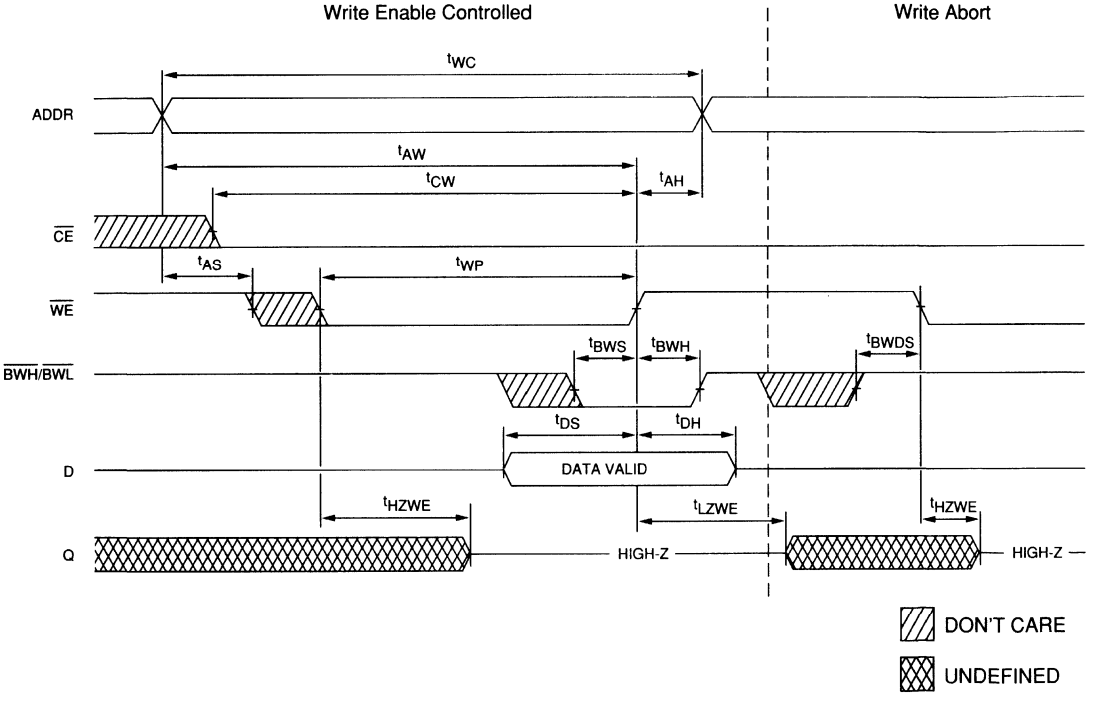


WRITE CYCLE NO. 2 [10, 14, 15]

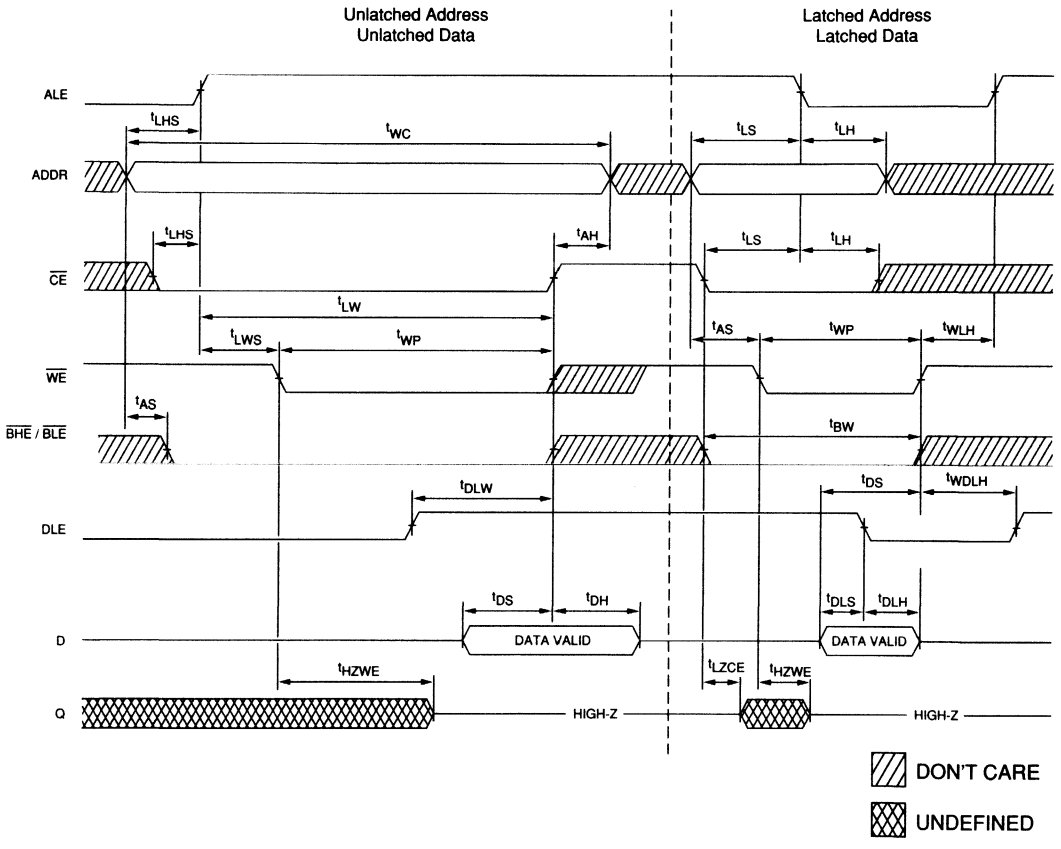
Write Enable Initiated/Chip Enable Terminated
(ALE = DLE = HIGH)



WRITE CYCLE NO. 3 [7, 10, 14, 15]
(ALE = DLE = HIGH)



WRITE CYCLE NO. 4 [7, 10, 14, 15]



LATCHED SRAM

16K x 16 SRAM

WITH ADDRESS/ DATA INPUT LATCHES, BYTE ENABLES

NEW

5 VOLT CACHE DATA/LATCHED SRAM

FEATURES

- Fast access times: 12, 15, 20 and 25ns
- Fast $\overline{OE}$: 5, 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Separate data input latch
- Common data inputs and data outputs
- Dual Byte Enables for BYTE READ/WRITE capability and device power down
- Direct connection to 386SL
- Dual $\overline{CE}$ for simplified memory expansion
- Address and $\overline{CE}$ input latches

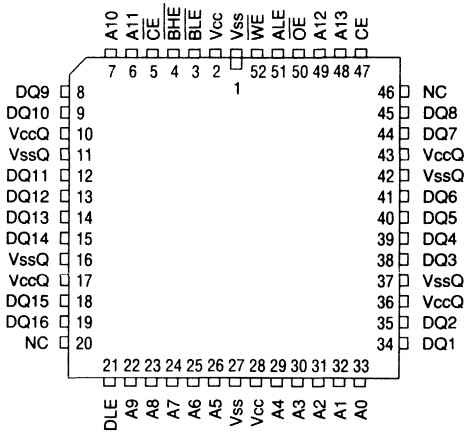
OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

- Part Number Example: MT56C16K16B2EJ-25

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT56C16K16B2 SRAM integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte enables and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus requiring separate byte enables.

Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual byte enables ($\overline{BHE}$ and $\overline{BLE}$) allow individual bytes to be controlled. $\overline{BLE}$ controls DQ1-DQ8 the lower bits. $\overline{BHE}$ controls DQ9-DQ16 the upper bits. When $\overline{BHE}$ and $\overline{BLE}$ are HIGH, the device is powered down.

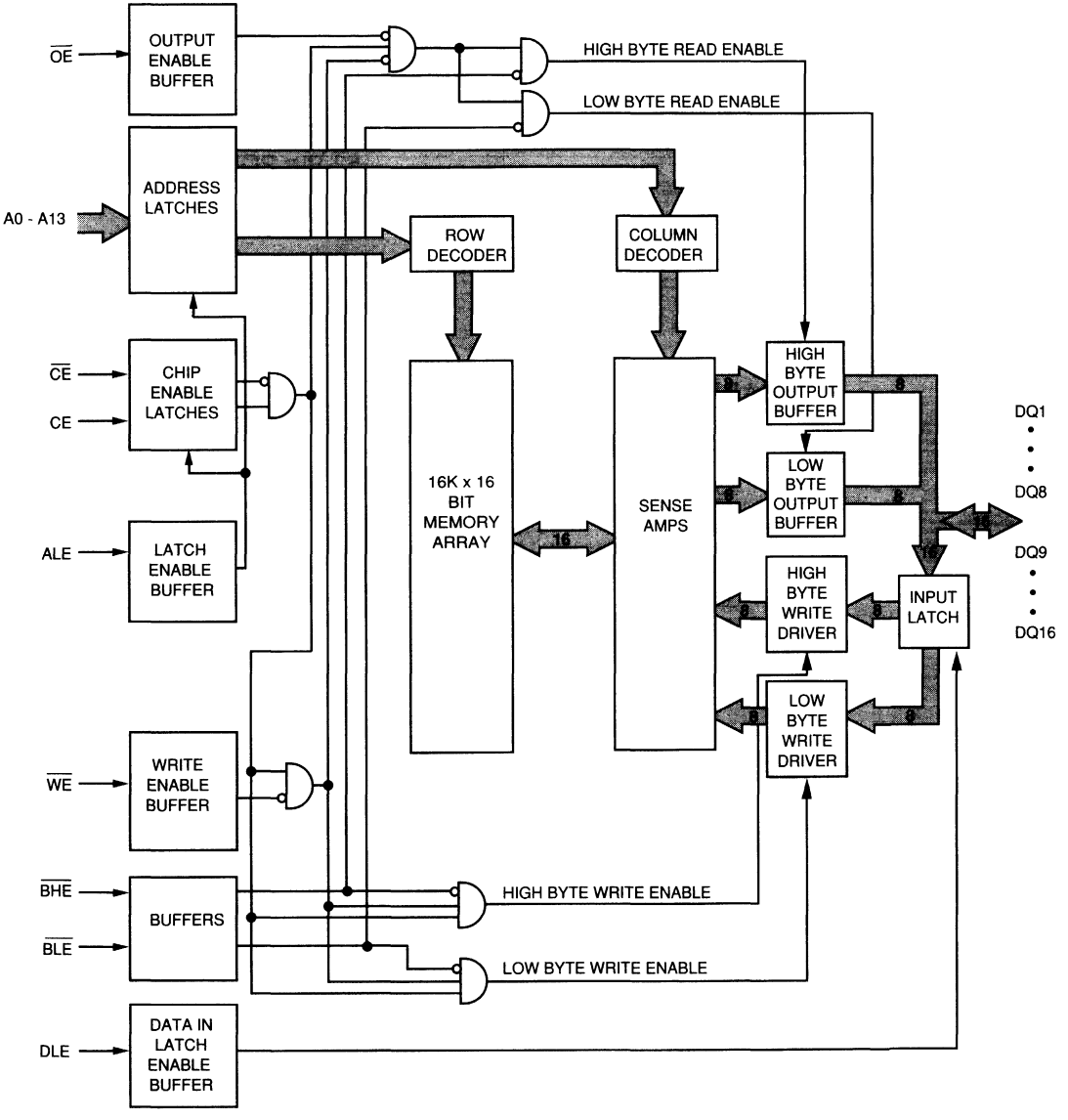
A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present on the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times and shortening the amount of time that valid data must be present.

The MT56C16K16B2 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

NEW

5 VOLT CACHE DATA/LATCHED SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BLE}$ $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be selected, permitting direct connection in systems that provide separate chip selects for high and low bytes. When $\overline{BLE}$ is LOW, the lower byte, D1-D8, is enabled. When $\overline{BHE}$ is LOW, the upper byte, D9-D16, is enabled. The device will be in low power standby mode when both Byte Enables are inactive (HIGH) or when either Chip Enable is inactive.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration. The device will be in low power standby mode when either Chip Enable is inactive (CE= LOW or $\overline{CE}$=HIGH) or both Byte Enables are inactive.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
46, 20	NC	-	No connect: These signals are no connects (NCs). NCs are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the required setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION		CE	$\overline{CE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	ALE	DLE	$\overline{OE}$	DQ
Deselected (low power standby)		L	X	X	X	X	X	X	X	High-Z
Deselected (low power standby)		X	H	X	X	X	X	X	X	High-Z
Deselected (low power standby)		X	X	X	H	H	X	X	X	High-Z
READ		H	L	H	L	L	H	X	H	High-Z
WORD READ		H	L	H	L	L	H	X	L	Q1-Q16
LATCHED WORD READ		H	L	H	L	L	L	X	L	Q1-Q16
BYTE READ	(DQ1-DQ8)	H	L	H	L	H	H	X	L	D1-D8
LATCHED BYTE READ	(DQ1-DQ8)	H	L	H	L	H	L	X	L	D1-D8
BYTE READ	(DQ9-DQ16)	H	L	H	H	L	H	X	L	D9-D16
LATCHED BYTE READ	(DQ9-DQ16)	H	L	H	H	L	L	X	L	D9-D16
WORD WRITE transparent data-in	(DQ1-DQ16)	H	L	L	L	L	H	H	X	D1-D16
LATCHED WORD WRITE transparent data-in	(DQ1-DQ16)	H	L	L	L	L	L	H	X	D1-D16
WORD WRITE latched data-in	(DQ1-DQ16)	H	L	L	L	L	H	L	X	D1-D16
LATCHED WORD WRITE latched data-in	(DQ1-DQ16)	H	L	L	L	L	L	L	X	D1-D16
BYTE WRITE transparent data-in	(DQ1-DQ8)	H	L	L	L	H	H	H	X	D1-D8
LATCHED BYTE WRITE transparent data-in	(DQ1-DQ8)	H	L	L	L	H	L	H	X	D1-D8
BYTE WRITE transparent data-in	(DQ9-DQ16)	H	L	L	H	L	H	H	X	D9-D16
LATCHED BYTE WRITE transparent data-in	(DQ9-DQ16)	H	L	L	H	L	L	H	X	D9-D16
BYTE WRITE latched data-in	(DQ1-DQ8)	H	L	L	L	H	H	L	X	D1-D8
LATCHED BYTE WRITE latched data-in	(DQ1-DQ8)	H	L	L	L	H	L	L	X	D1-D8
BYTE WRITE latched data-in	(DQ9-DQ16)	H	L	L	H	L	H	L	X	D9-D16
LATCHED BYTE WRITE latched data-in	(DQ9-DQ16)	H	L	L	H	L	L	L	X	D9-D16

NOTE:
1. Latched inputs (Addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -1V to +7V
Voltage on any pin Relative to V_{SS}/V_{SSQ} .... -1V to V_{CC}+1V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Output Buffer Supply Voltage	5V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ ≤ V_{IL}; CE ≥ V_{IH} V_{CC} = MAX; Outputs Open f = MAX = 1/ ^tRC	I_{CC}	150	310	280	250	230	mA	3
Power Supply Current: Standby	CE ≤ V_{IL}; $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ ≥ V_{IH}; V_{CC} = MAX; Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	50	80	75	70	65	mA	
	$\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ ≥ V_{CC} -0.2; CE ≤ V_{SS} +0.2 V_{CC} = MAX; V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	15	15	15	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

NEW 5 VOLT CACHE DATA/LATCHED SRAM

NEW

5 VOLT CACHE DATA/LATCHED SRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = VccQ = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Address Latch											
Latch cycle time	^tLC	12		15		20		25		ns	
Latch HIGH time	^tLEH	5		5		5		5		ns	
Address/Chip Enable setup to latch LOW	^tLS	2		2		2		2		ns	
Address/Chip Enable hold from latch LOW	^tLH	3		3		3		3		ns	
Address/Chip Enable setup to latch HIGH	^tLHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		2		2		ns	6, 7
Latch HIGH to output in High-Z	^tHZL	2	8	2	8	2	9	2	10	ns	6, 7
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	6, 7
Chip disable to output in High-Z	^tHZCE	2	8	2	8	2	9	2	10	ns	6, 7
Output Enable access time	^tAOE		5		6		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE	2	5	2	6	2	8	2	10	ns	6, 7
Byte Enable access time	^tABE		12		15		20		25	ns	
Byte Enables to output in Low-Z	^tLZBE	2		2		2		2		ns	6, 7
Byte Disables to output in High-Z	^tHZBE	2	8	2	8	2	10	2	10	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		13		15		20		ns	
Address valid to end of write	^tAW	10		13		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	10		13		15		20		ns	
Data setup time	^tDS	4		6		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	6, 7
Write Enable to output in High-Z	^tHZWE	0	8	0	8	0	9	0	10	ns	6, 7
Byte Enable to end of write	^tBW	10		13		15		20		ns	
Data setup to DLE LOW	^tDLS	1		1		1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		3		3		ns	9
DLE HIGH to end of write	^tDLW	5		6		8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		0		0		ns	
ALE HIGH setup time to Write Enable LOW	^tLWS	0		0		0		0		ns	
ALE HIGH to end of write	^tLW	10		13		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

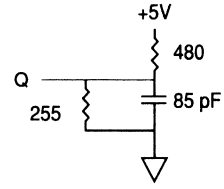


Fig. 1 OUTPUT LOAD EQUIVALENT

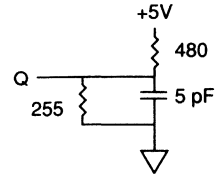


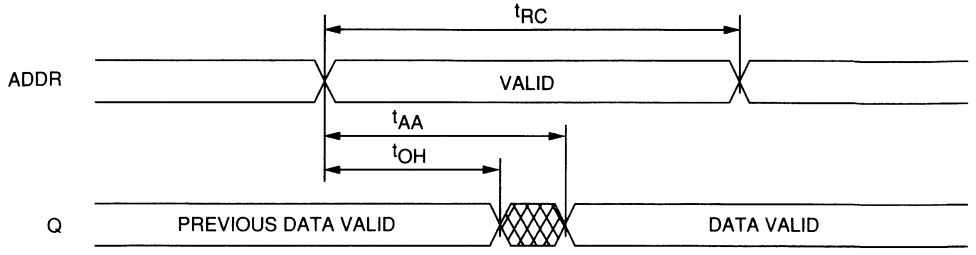
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

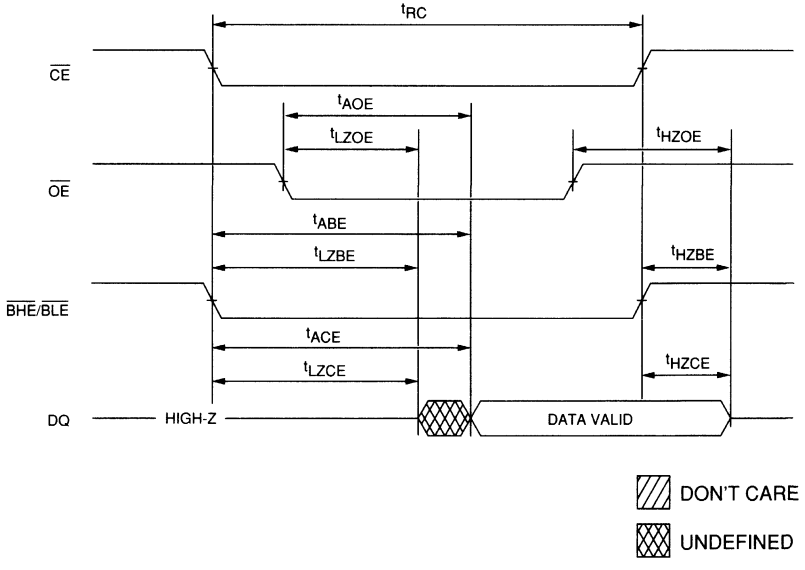
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, $^{t}HZOE$ is less than $^{t}LZOE$, and $^{t}HZBE$ is less than $^{t}LZBE$.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to, or coincident with, the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.
15. If output enable is inactive (HIGH) the output will be in High-Z instead of undefined.
16. $\overline{BHE}$ and $\overline{BLE}$ are LOW.

NEW 5 VOLT CACHE DATA/LATCHED SRAM

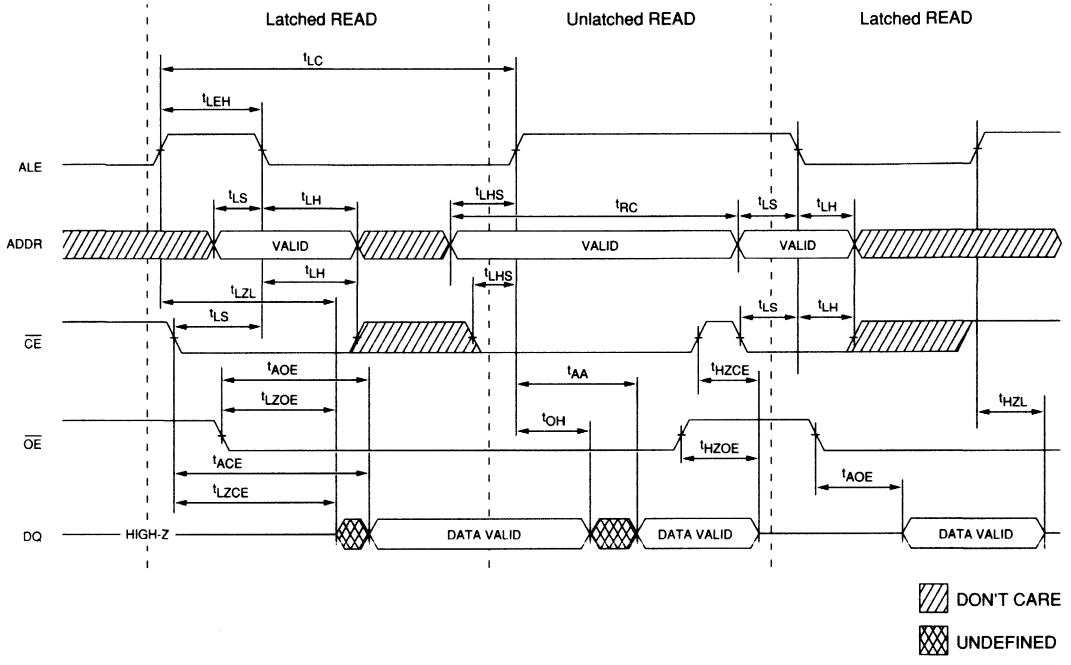
READ CYCLE NO. 1 [11, 12, 16]
(ALE = DLE = HIGH)



READ CYCLE NO. 2 [7, 11, 13, 14]
(ALE = DLE = HIGH)



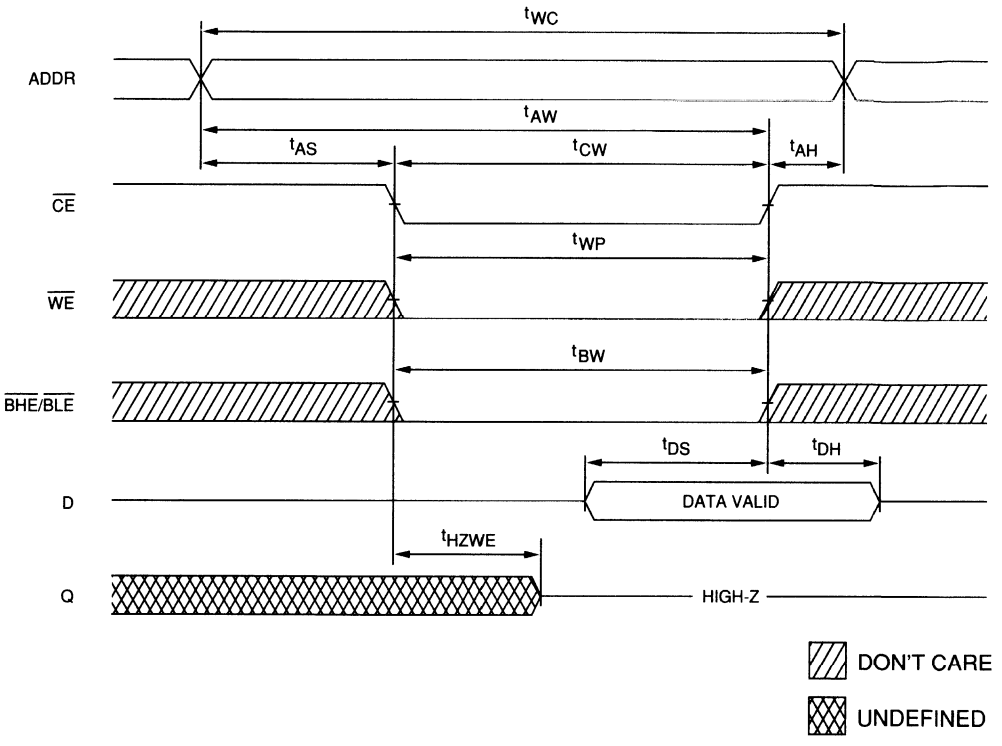
READ CYCLE NO. 3 [7, 11, 14, 16]



NEW 5 VOLT CACHE DATA/LATCHED SRAM

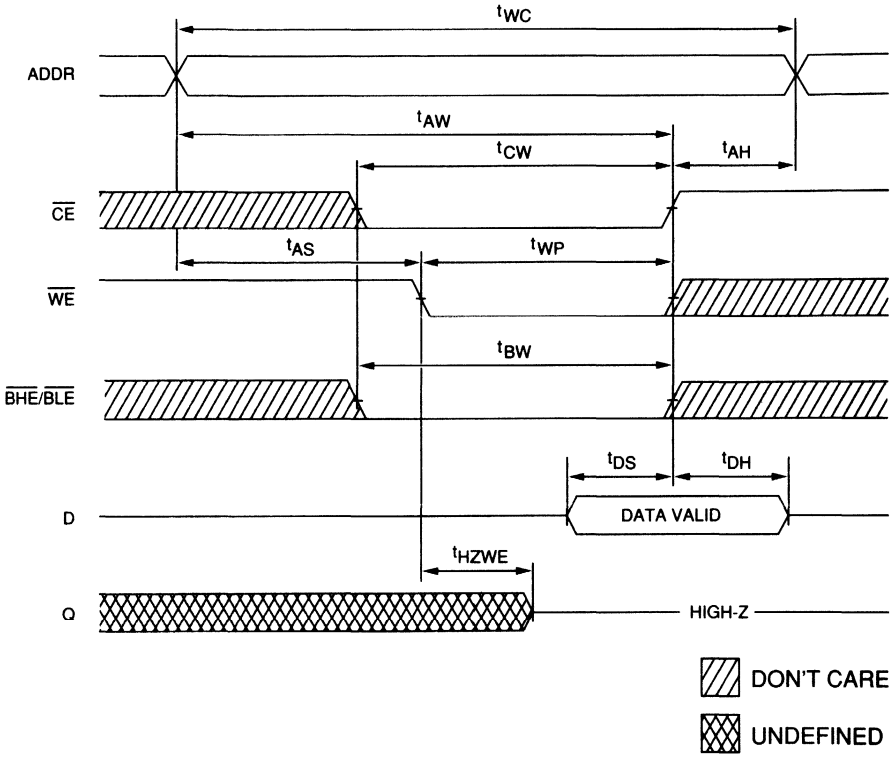
WRITE CYCLE NO. 1 [10, 14, 15]

Chip Enable Controlled
(ALE = DLE = HIGH)



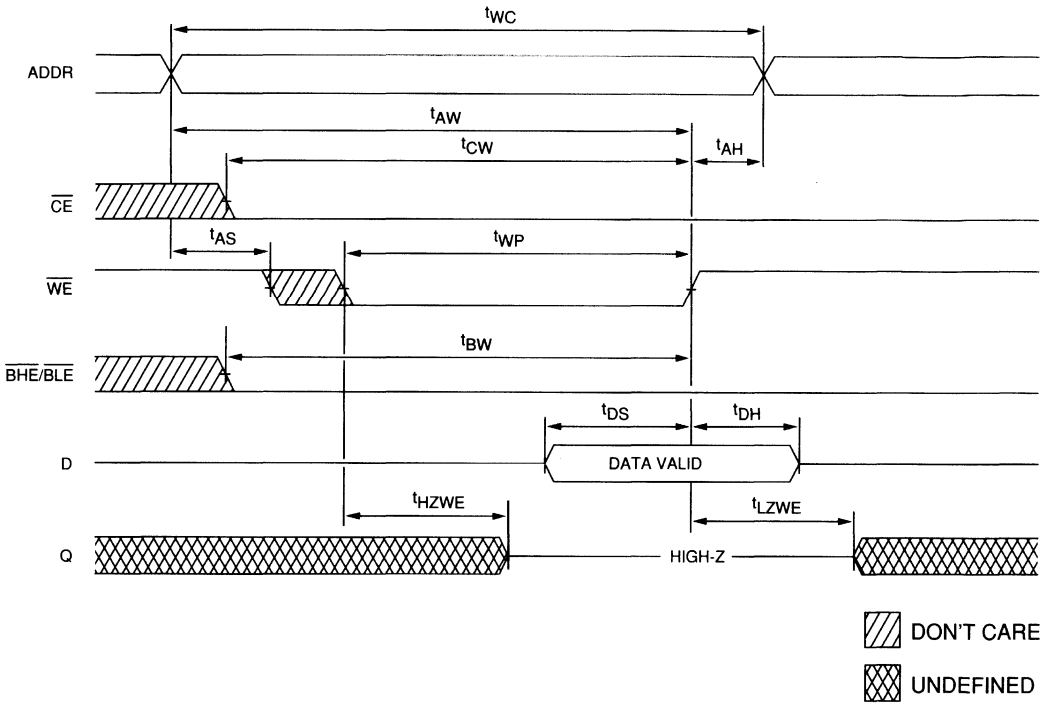
WRITE CYCLE NO. 2 [10, 14, 15]

Write Enable Initiated / Chip Enable Terminated
(ALE = DLE = HIGH)



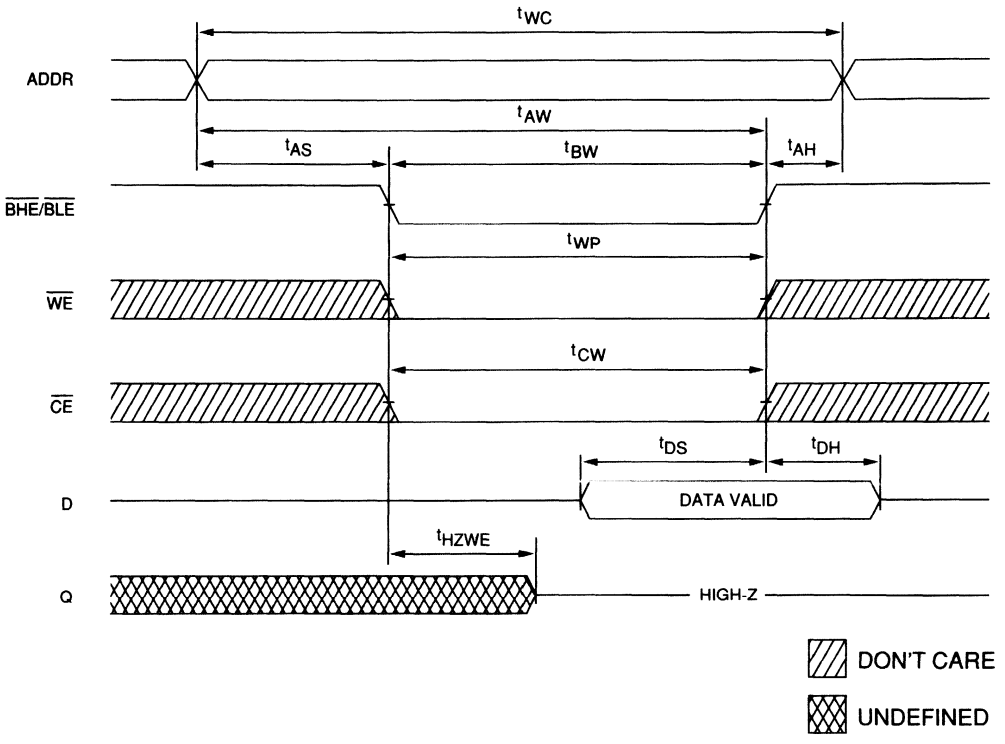
WRITE CYCLE NO. 3 [7, 10, 14, 15]

Write Enable Controlled
(ALE = DLE = HIGH)



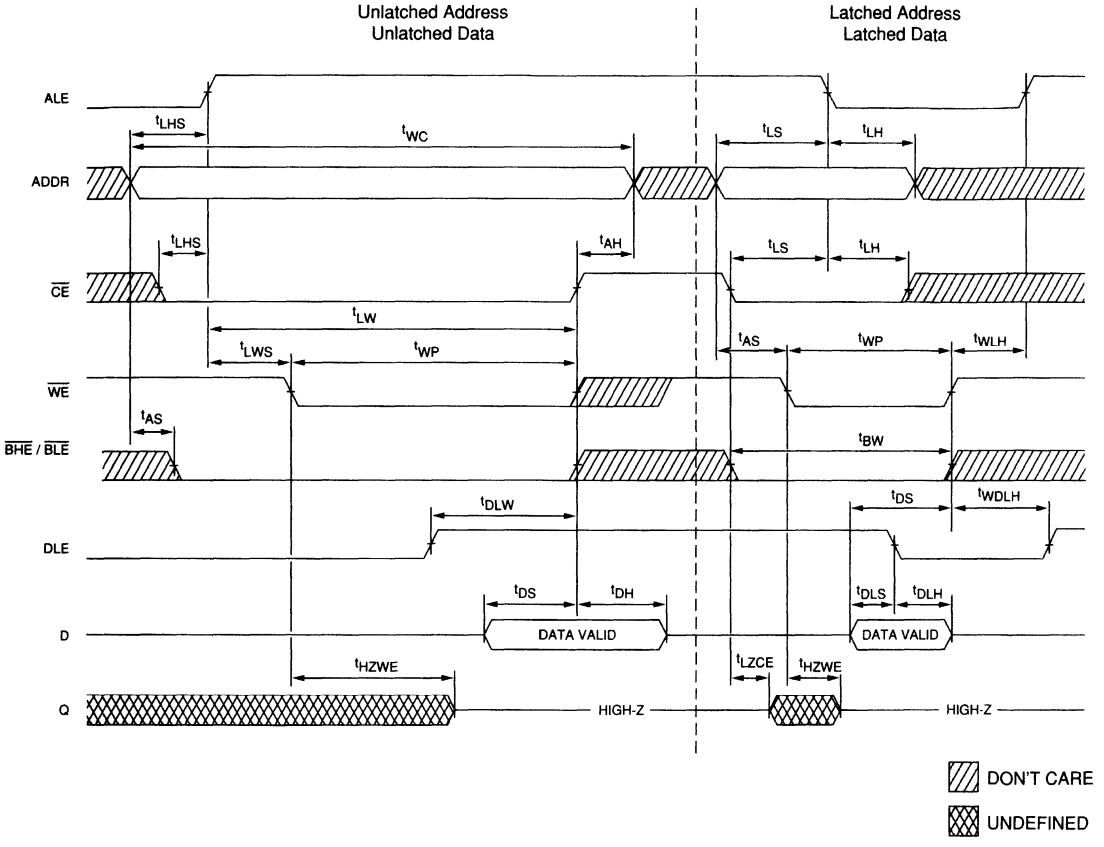
WRITE CYCLE NO. 4 [10, 14, 15]

Byte Enable Controlled
(ALE = DLE = HIGH)



NEW 5 VOLT CACHE DATA/LATCHED SRAM

WRITE CYCLE NO. 5 [7, 10, 14, 15]



MICRON

3.3V CACHE DATA/LATCHED SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package				Die	Page
				PLCC	PQFP	SOJ	TSOP		
16K x 16	Latched Address and Data, Dual Chip Enables, Output Enable, Byte Write Controls	MT5LC2516	20, 25	52	52	-	-	CD1 CD2	6-1
16K x 18	Latched Address and Data, Dual Chip Enables, Byte Write Controls Byte Write Controls	MT5LC2818	20, 25	52	52	-	-	CD1 CD2	6-15
16K x 16	Latched Address and Data, Dual Chip Enables, Byte Enables	MT56LC16K16C3	20, 25	52	52	-	-	CD1 CD2	6-29

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.
2. CD1 - Functionally probed die.
3. CD2 - Speed graded die; specifications may differ from package component data sheets.

LATCHED SRAM

16K x 16 SRAM

3.3V OPERATION
ADDRESS/DATA INPUT LATCHES

NEW
3.3 VOLT CACHE DATA/LATCHED SRAM

FEATURES

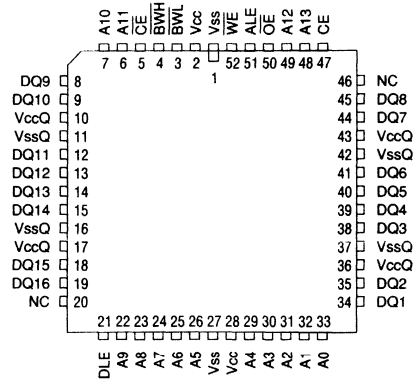
- Fast access times: 20 and 25ns
- Fast $\overline{OE}$: 8 and 10ns
- Single +3.3V ±0.3V power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Separate data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Address and $\overline{CE}$ input latches

OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 52-pin PLCC — EJ
  - 52-pin PQFP — LG
- Part Number Example: MT5LC2516EJ-25

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5LC2516 SRAM is designed to operate at 3.3 volts. It integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus. Parity bits are provided for added data integrity.

Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

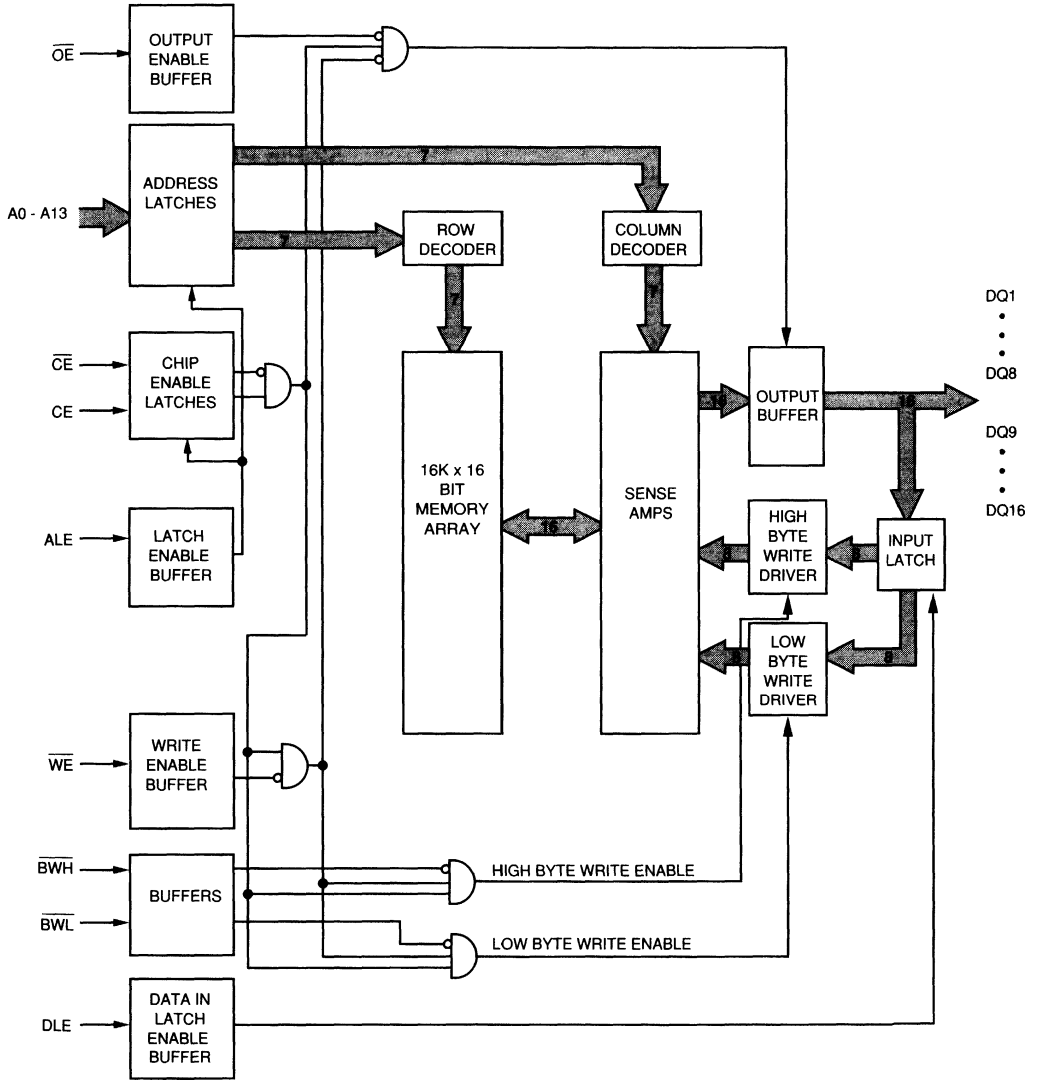
Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8, the lower bits. While $\overline{BWH}$ controls DQ9-DQ16, the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present in the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5LC2516 operates from a +3.3V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow for improved noise immunity.

NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
20, 46	NC	Input/ Output	No Connection: These signals are no connects (NCs). NCs are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +3.3V ±0.3V
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±0.3V
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ
Deselected cycle	L	X	X	X	X	X	X	X	High-Z
Deselected	X	H	X	X	X	X	X	X	High-Z
READ	H	L	H	X	X	H	X	H	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16

NOTE:
1. Latched inputs (Addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±0.3V; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}, CE ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	70	100	mA	3
Power Supply Current: Standby	CE ≤ V_{IL}, $\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	15	30	mA	
	$\overline{CE}$ ≥ V_{CC} - 0.2V; CE ≤ V_{SS} +0.2V V_{CC} = MAX; V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	3	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = V_{CCQ} = 3.3V \pm 0.3V$)

DESCRIPTION	SYM	-20 MIN	-20 MAX	-25 MIN	-25 MAX	UNITS	NOTES
Address Latch							
Latch cycle time	^tLC	20		25		ns	
Latch HIGH time	^tLEH	5		5		ns	
Address/Chip Enable setup to latch LOW	^tLS	2		2		ns	
Address/Chip Enable hold from latch LOW	^tLH	3		3		ns	
Address/Chip Enable setup to latch HIGH	^tLHS	0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		ns	6, 7
Latch HIGH to output in High-Z	^tHZL	2	12	2	12	ns	6, 7
READ Cycle							
READ cycle time	^tRC	20		25		ns	
Address access time	^tAA		20		25	ns	
Chip Enable access time	^tACE		20		25	ns	
Output hold from address change	^tOH	4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		ns	6, 7
Chip disable to output in High-Z	^tHZCE	2	12	2	12	ns	6, 7
Output Enable access time	^tAOE		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE	0	8	0	10	ns	6, 7
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	
Chip Enable to end of write	^tCW	15		20		ns	
Address valid to end of write	^tAW	15		20		ns	
Address setup time	^tAS	0		0		ns	
Address hold from end of write	^tAH	3		3		ns	
WRITE pulse width	^tWP	15		20		ns	
Data setup time	^tDS	8		10		ns	
Data hold time	^tDH	0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		4		ns	6, 7
Write Enable to output in High-Z	^tHZWE	0	10	0	10	ns	6, 7
Byte Write Enable setup time	^tBWS	8		10		ns	
Byte Write Enable hold time	^tBWH	2		2		ns	
Byte Write disable setup time	^tBWDS	0		0		ns	
Data setup to DLE LOW	^tDLS	1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		ns	9
DLE HIGH to end of write	^tDLW	8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		ns	
ALE HIGH setup time to write enable LOW	^tLWS	0		0		ns	
ALE HIGH to end of write	^tLW	15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

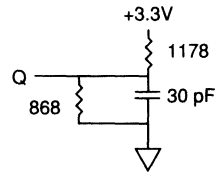


Fig. 1 OUTPUT LOAD EQUIVALENT

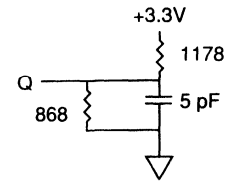
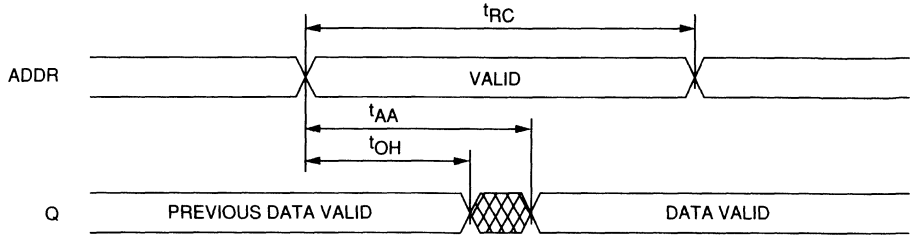


Fig. 2 OUTPUT LOAD EQUIVALENT

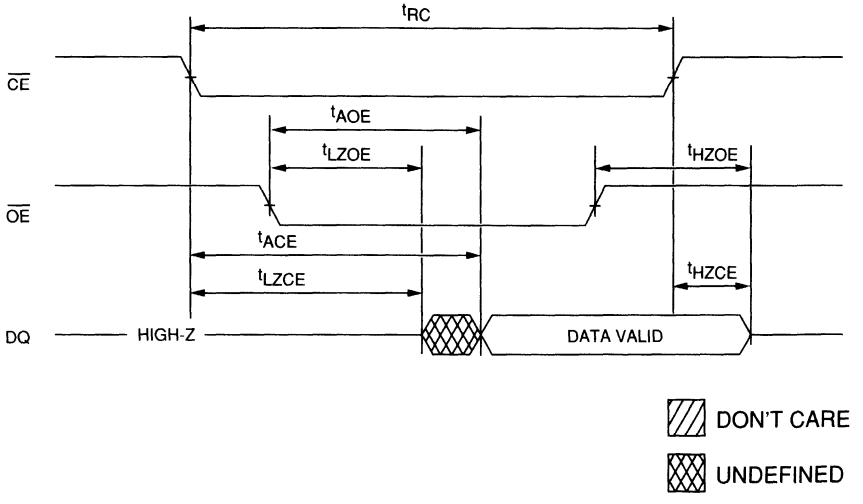
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5 pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, $^{t}HZOE$ is less than $^{t}LZOE$, and $^{t}HZWE$ is less than $^{t}LZWE$.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable and chip enable can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to, or coincident with, the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.
15. If output enable is inactive (HIGH), the output will be in High-Z (not undefined).

READ CYCLE NO. 1 [11, 12]

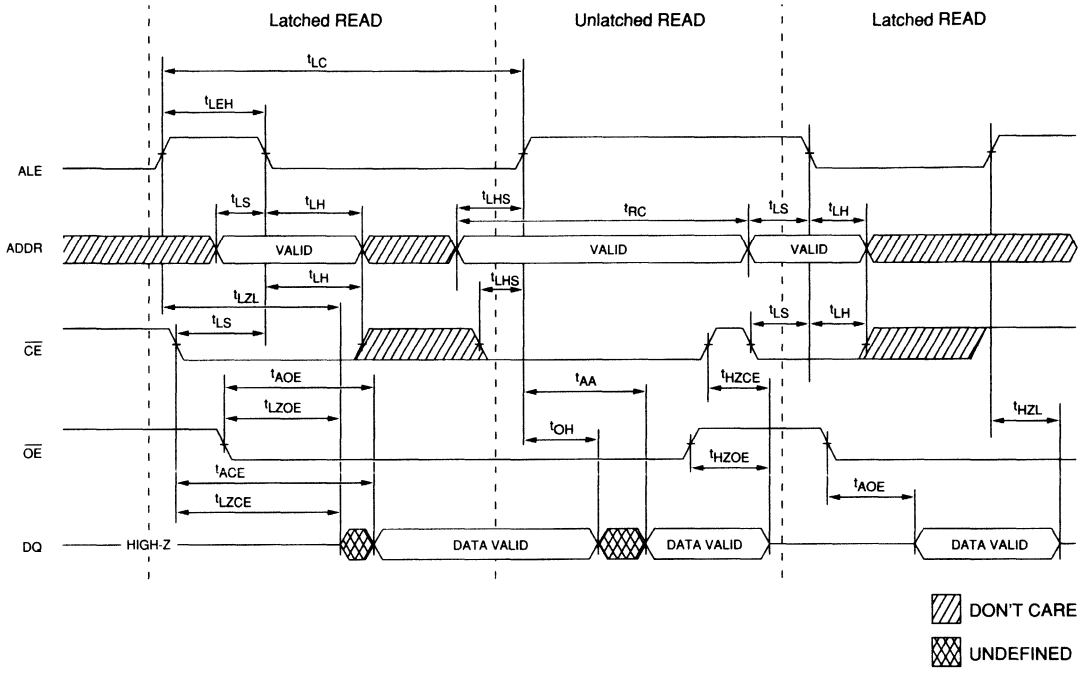


READ CYCLE NO. 2 [7, 11, 13, 14]



READ CYCLE NO. 3 [7, 11, 14]

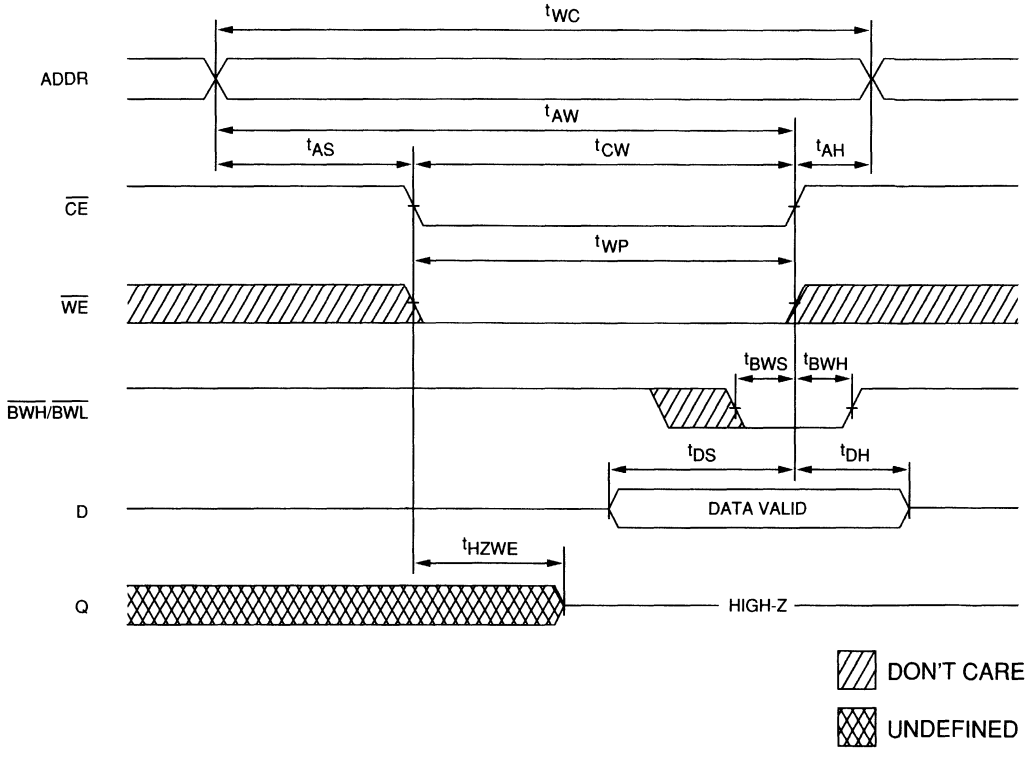
(DLE = HIGH)



NEW ■ 3.3 VOLT CACHE DATA/LATCHED SRAM

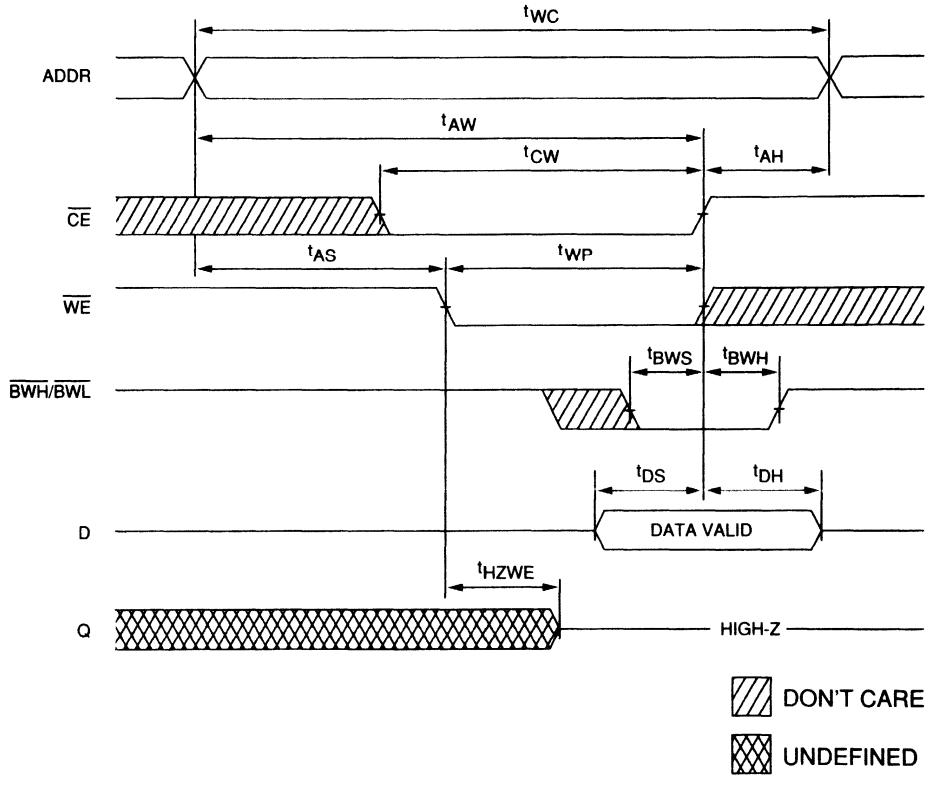
WRITE CYCLE NO. 1 [10, 14, 15]

Chip Enable Controlled
(ALE = DLE = HIGH)



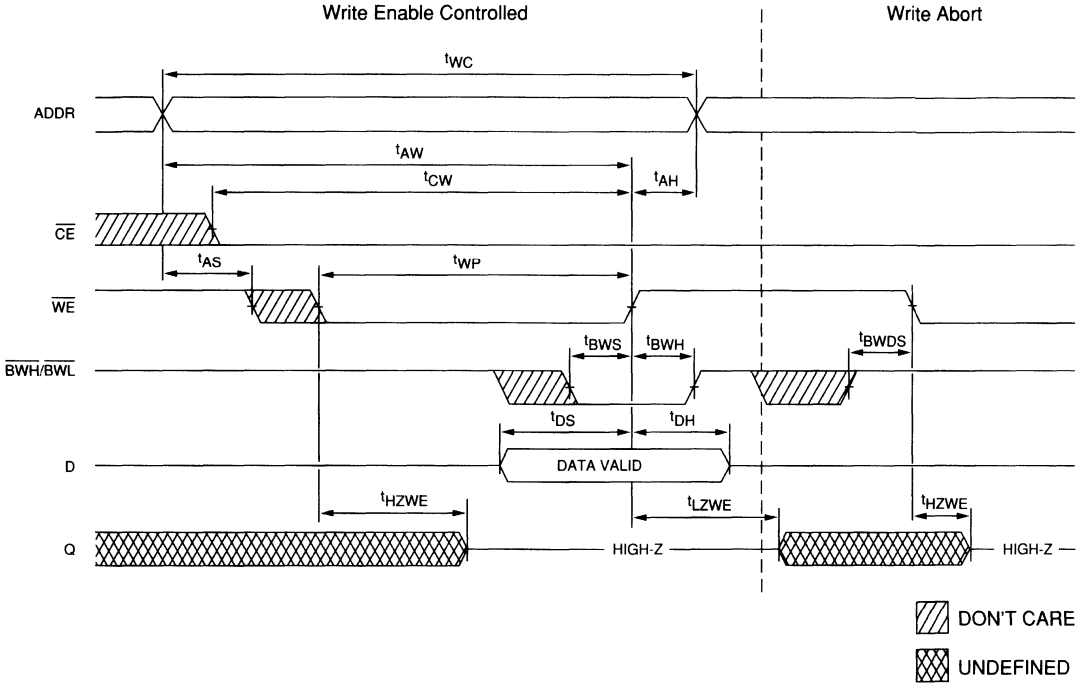
WRITE CYCLE NO. 2 [10, 14, 15]

Write Enable Initiated/Chip Enable Terminated
(ALE = DLE = HIGH)

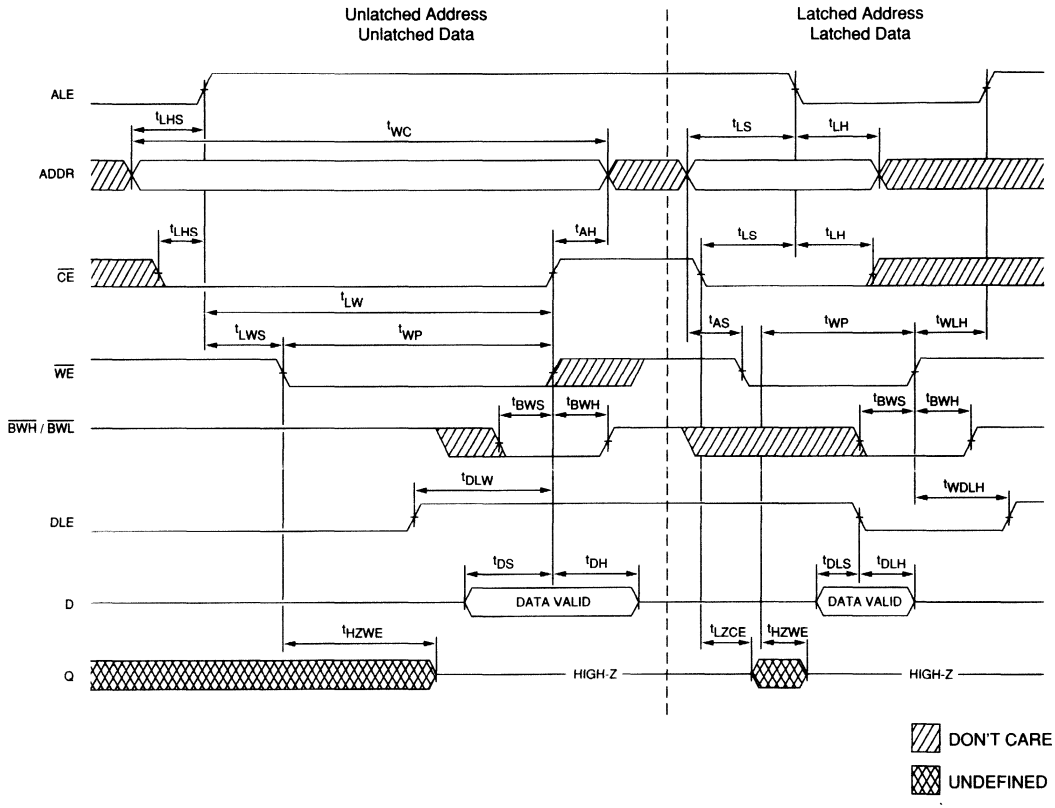


NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

WRITE CYCLE NO. 3 [7, 10, 14, 15]
(ALE = DLE = HIGH)



WRITE CYCLE NO. 4 [7, 10, 14, 15]



NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

NEW

3.3 VOLT CACHE DATA/LATCHED SRAM

LATCHED SRAM

16K x 18 SRAM

3.3V OPERATION
ADDRESS/DATA INPUT LATCHES

FEATURES

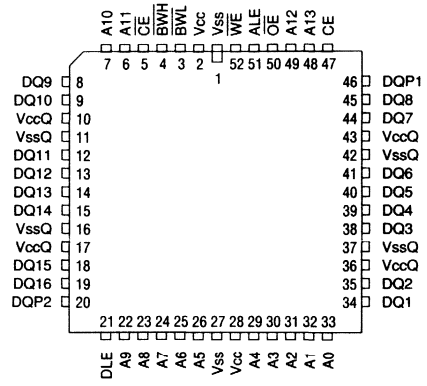
- Fast access times: 20 and 25ns
- Fast $\overline{OE}$: 8 and 10ns
- Single +3.3V ±0.3V power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Separate data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Parity bits
- Address and $\overline{CE}$ input latches

OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 52-pin PLCC — EJ
  - 52-pin PQFP — LG
- Part Number Example: MT5LC2818EJ-25

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5LC2818 SRAM is designed to operate at 3.3 volts. It integrates a 16K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus. Parity bits are provided for added data integrity.

Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8 and DQP1, the lower bits. While $\overline{BWH}$ controls DQ9-DQ16 and DQP2, the upper bits.

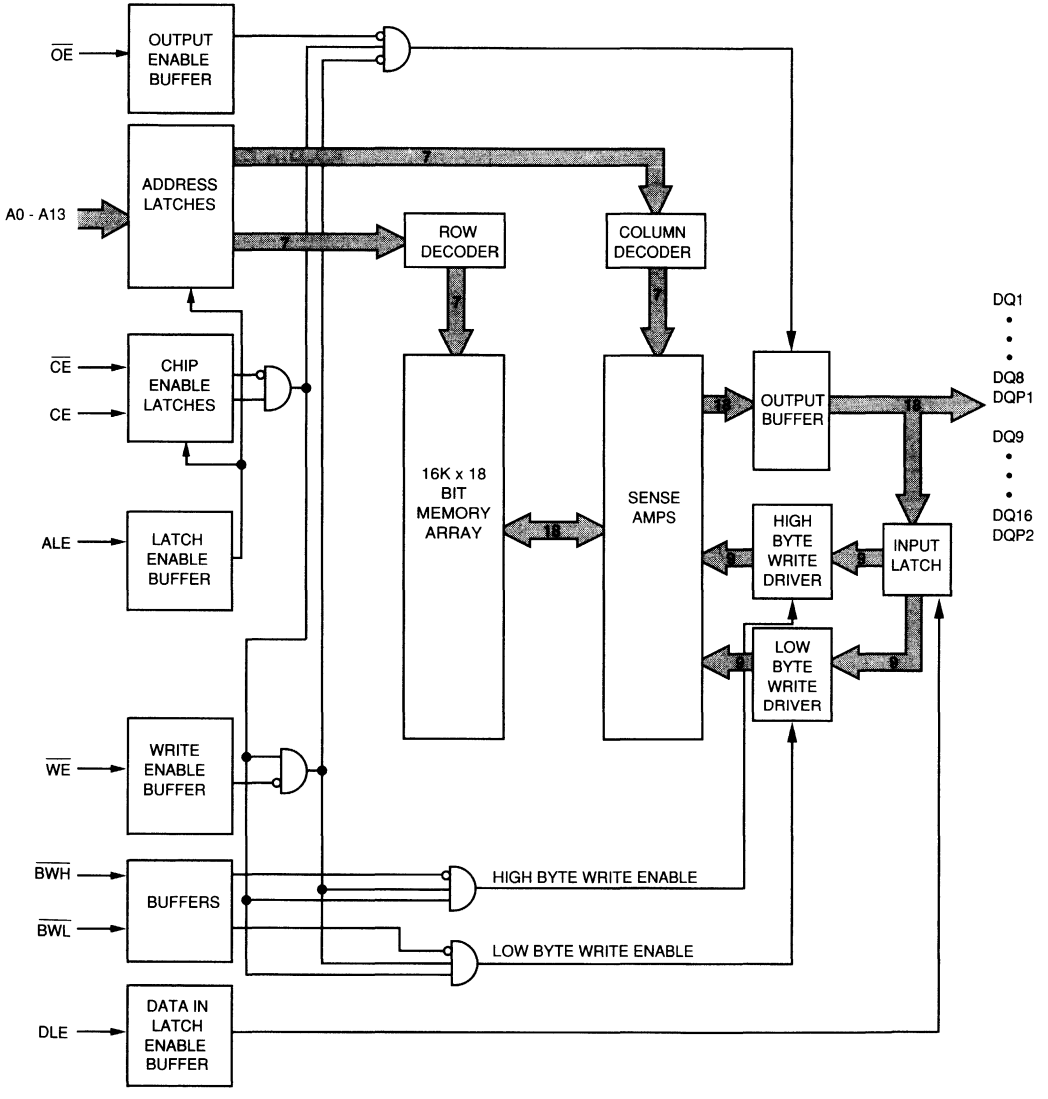
A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present in the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5LC2818 operates from a +3.3V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow for improved noise immunity.

NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
46, 20	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +3.3V ±0.3V
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±0.3V
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ	DQP
Deselected cycle	L	X	X	X	X	X	X	X	High-Z	High-Z
Deselected	X	H	X	X	X	X	X	X	High-Z	High-Z
READ	H	L	H	X	X	H	X	H	High-Z	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16	QP1, QP2
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16	QP1, QP2
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16	DP1, DP2
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16	DP1, DP2
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16	DP2
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16	DP2

NOTE:
1. Latched inputs (Addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to Vcc+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V; Vss = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}, CE ≥ V_{IH}; Vcc = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	70	100	mA	3
Power Supply Current: Standby	CE ≤ V_{IL}, $\overline{CE}$ ≥ V_{IH}; Vcc = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	15	30	mA	
	$\overline{CE}$ ≥ Vcc - 0.2V; CE ≤ Vss +0.2V Vcc = MAX; V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	3	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 3.3V ±0.3V)

DESCRIPTION	SYM	-20 MIN	-20 MAX	-25 MIN	-25 MAX	UNITS	NOTES
Address Latch							
Latch cycle time	^tLC	20		25		ns	
Latch HIGH time	^tLEH	5		5		ns	
Address/Chip Enable setup to latch LOW	^tLS	2		2		ns	
Address/Chip Enable hold from latch LOW	^tLH	3		3		ns	
Address/Chip Enable setup to latch HIGH	^tLHS	0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		ns	6, 7
Latch HIGH to output in High-Z	^tHZL	2	12	2	12	ns	6, 7
READ Cycle							
READ cycle time	^tRC	20		25		ns	
Address access time	^tAA		20		25	ns	
Chip Enable access time	^tACE		20		25	ns	
Output hold from address change	^tOH	4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		ns	6, 7
Chip disable to output in High-Z	^tHZCE	2	12	2	12	ns	6, 7
Output Enable access time	^tAOE		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE	0	8	0	10	ns	6, 7
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	
Chip Enable to end of write	^tCW	15		20		ns	
Address valid to end of write	^tAW	15		20		ns	
Address setup time	^tAS	0		0		ns	
Address hold from end of write	^tAH	3		3		ns	
WRITE pulse width	^tWP	15		20		ns	
Data setup time	^tDS	8		10		ns	
Data hold time	^tDH	0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		4		ns	6, 7
Write Enable to output in High-Z	^tHZWE	0	10	0	10	ns	6, 7
Byte Write Enable setup time	^tBWS	8		10		ns	
Byte Write Enable hold time	^tBWH	2		2		ns	
Byte Write disable setup time	^tBWDS	0		0		ns	
Data setup to DLE LOW	^tDLS	1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		ns	9
DLE HIGH to end of write	^tDLW	8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		ns	
ALE HIGH setup time to write enable LOW	^tLWS	0		0		ns	
ALE HIGH to end of write	^tLW	15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

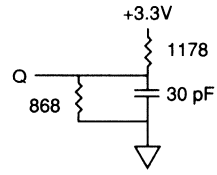


Fig. 1 OUTPUT LOAD EQUIVALENT

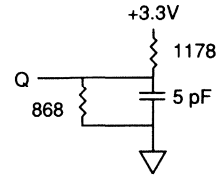
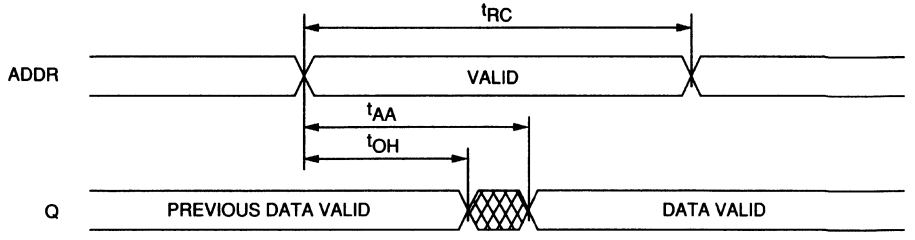


Fig. 2 OUTPUT LOAD EQUIVALENT

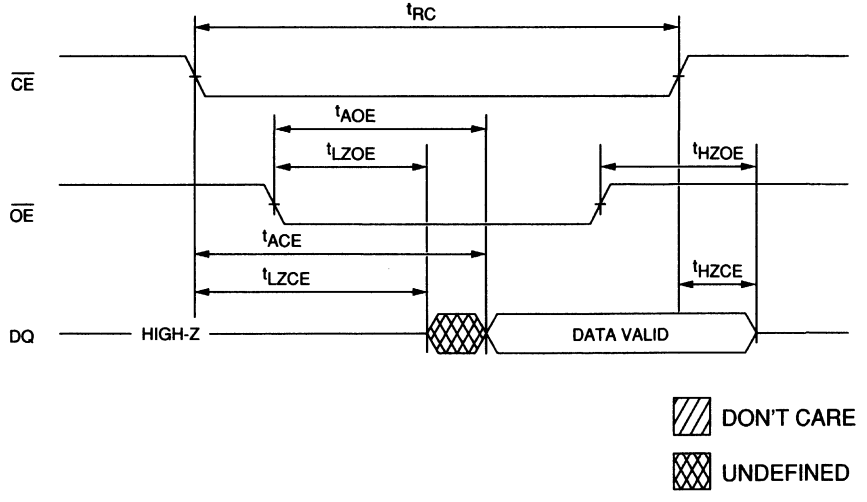
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5 pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, $^{t}HZOE$ is less than $^{t}LZOE$, $^{t}HZWE$ is less than $^{t}LZWE$, and ^{t}HZL is less than ^{t}LZL.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable and chip enable can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to, or coincident with, the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.
15. If output enable is inactive (HIGH), the output will be in High-Z (not undefined).

READ CYCLE NO. 1 [11, 12]

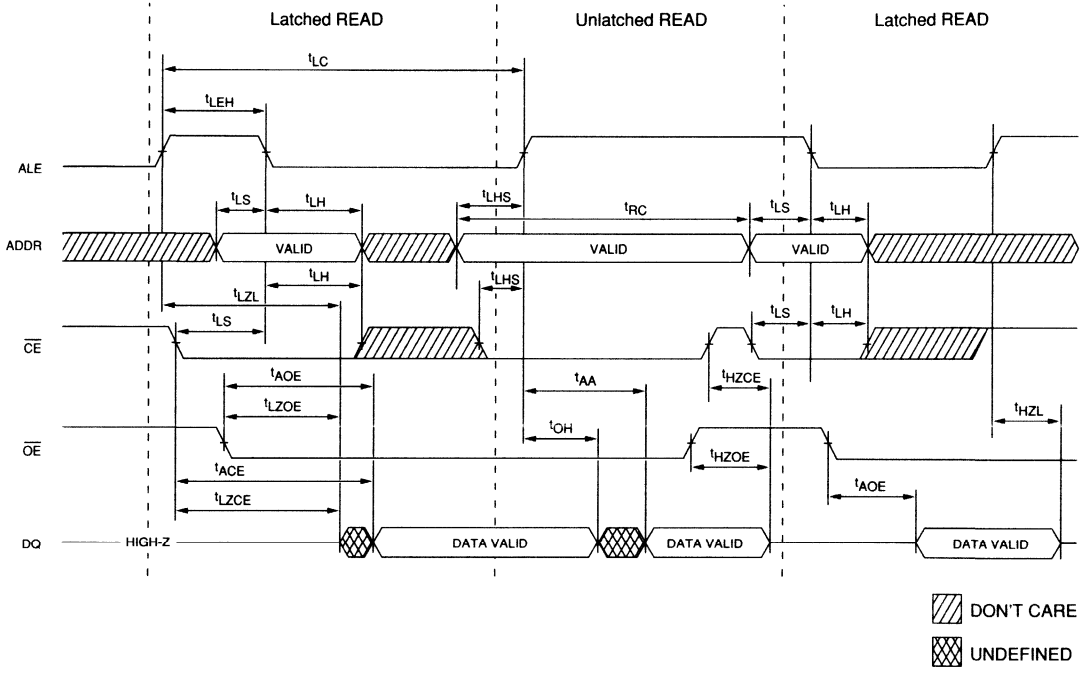


READ CYCLE NO. 2 [7, 11, 13, 14]



READ CYCLE NO. 3 [7, 11, 14]

(DLE = HIGH)

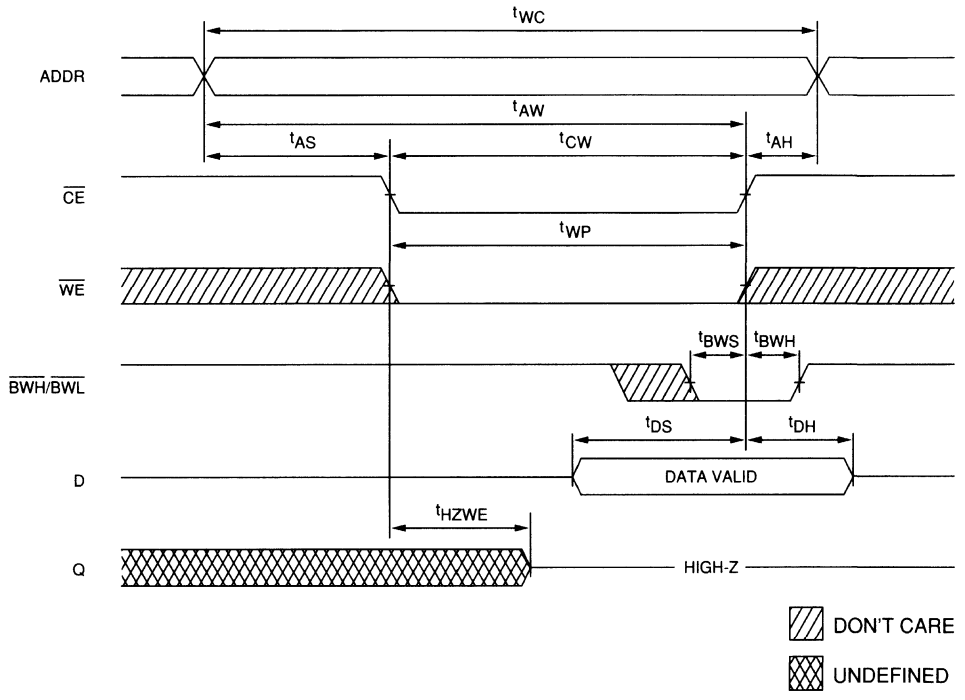


NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

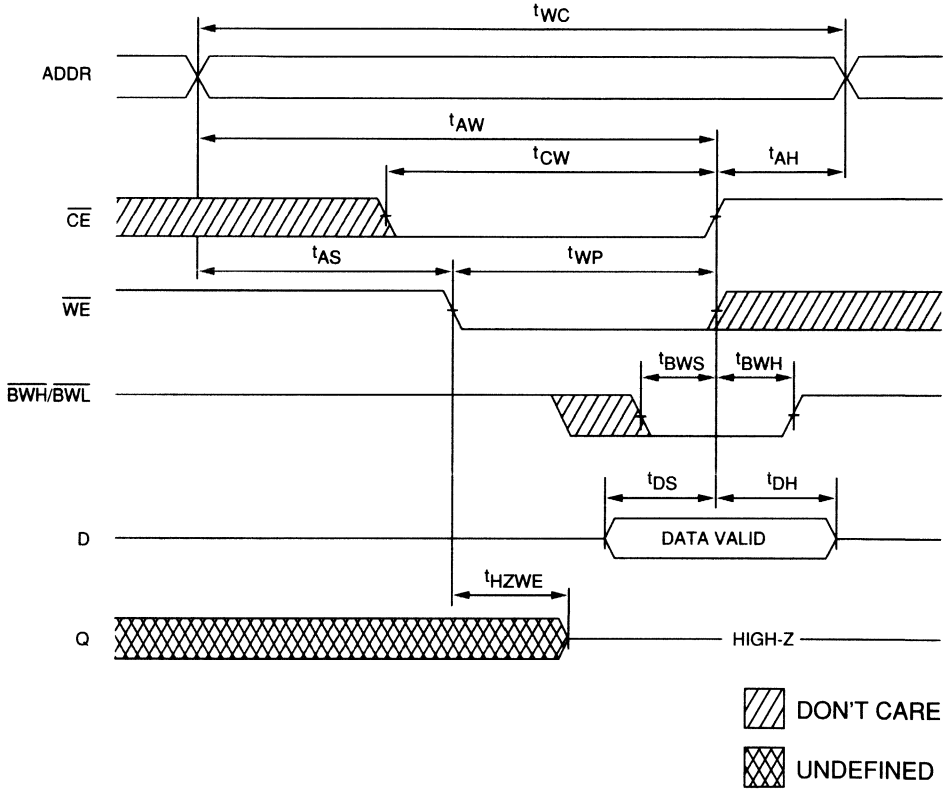
WRITE CYCLE NO. 1 [10, 14, 15]

Chip Enable Controlled
(ALE = DLE = HIGH)



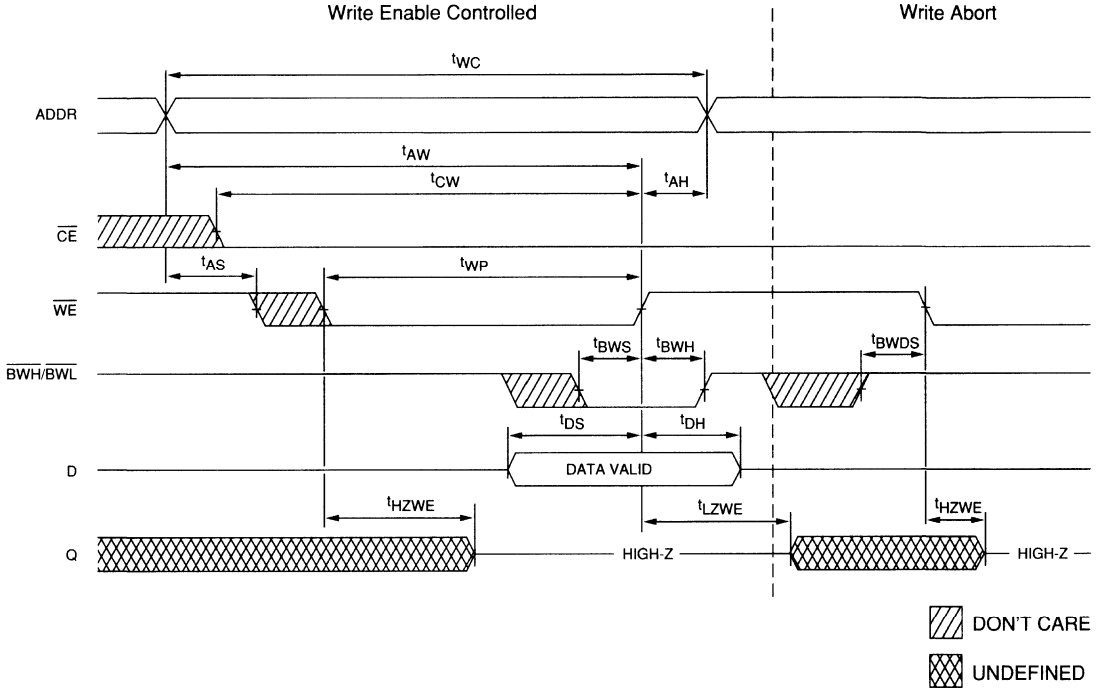
WRITE CYCLE NO. 2 [10, 14, 15]

Write Enable Initiated/Chip Enable Terminated
(ALE = DLE = HIGH)

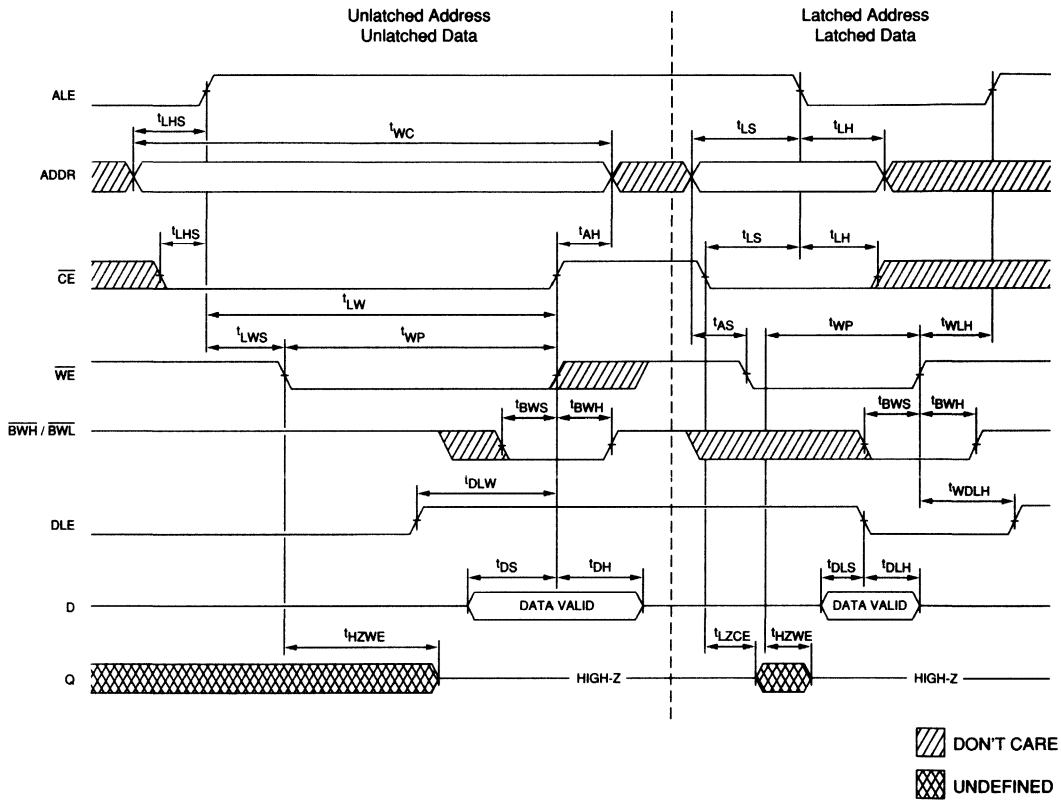


WRITE CYCLE NO. 3 [7, 10, 14, 15]

(ALE = DLE = HIGH)



WRITE CYCLE NO. 4 [7, 10, 14, 15]



NEW 3.3 VOLT CACHE DATA/LATCHED SRAM

NEW

3.3 VOLT CACHE DATA/LATCHED SRAM

LATCHED SRAM

16K x 16 SRAM

3.3V OPERATION
ADDRESS/ DATA INPUT LATCHES

NEW

3.3 VOLT CACHE DATA/LATCHED SRAM

FEATURES

- Fast access times: 20 and 25ns
- Fast $\overline{OE}$: 8 and 10ns
- Single +3.3V ±0.3V power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Separate data input latch
- Common data inputs and data outputs
- Dual Byte Enables for BYTE READ/WRITE capability and device power down
- Direct connection to 386SL
- Dual $\overline{CE}$s for simplified memory expansion
- Address and $\overline{CE}$ input latches

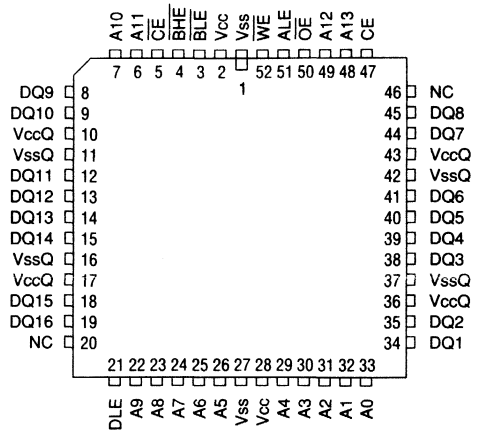
OPTIONS

MARKING

- Timing
  - 20ns access: -20
  - 25ns access: -25
- Packages
  - 52-pin PLCC: EJ
  - 52-pin PQFP: LG
- Part Number Example: MT56LC16K16C3

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SC-2)
52-Pin PQFP (SC-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT56LC16K16C3 SRAM is designed to operate at 3.3 volts. It integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte enables and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus requiring separate byte enables.

Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual byte enables ($\overline{BHE}$ and $\overline{BLE}$) allow individual bytes to be controlled. $\overline{BLE}$ controls DQ1-DQ8 the lower bits. $\overline{BHE}$ controls DQ9-DQ16 the upper bits. When $\overline{BHE}$ and $\overline{BLE}$ are HIGH, the device is powered down.

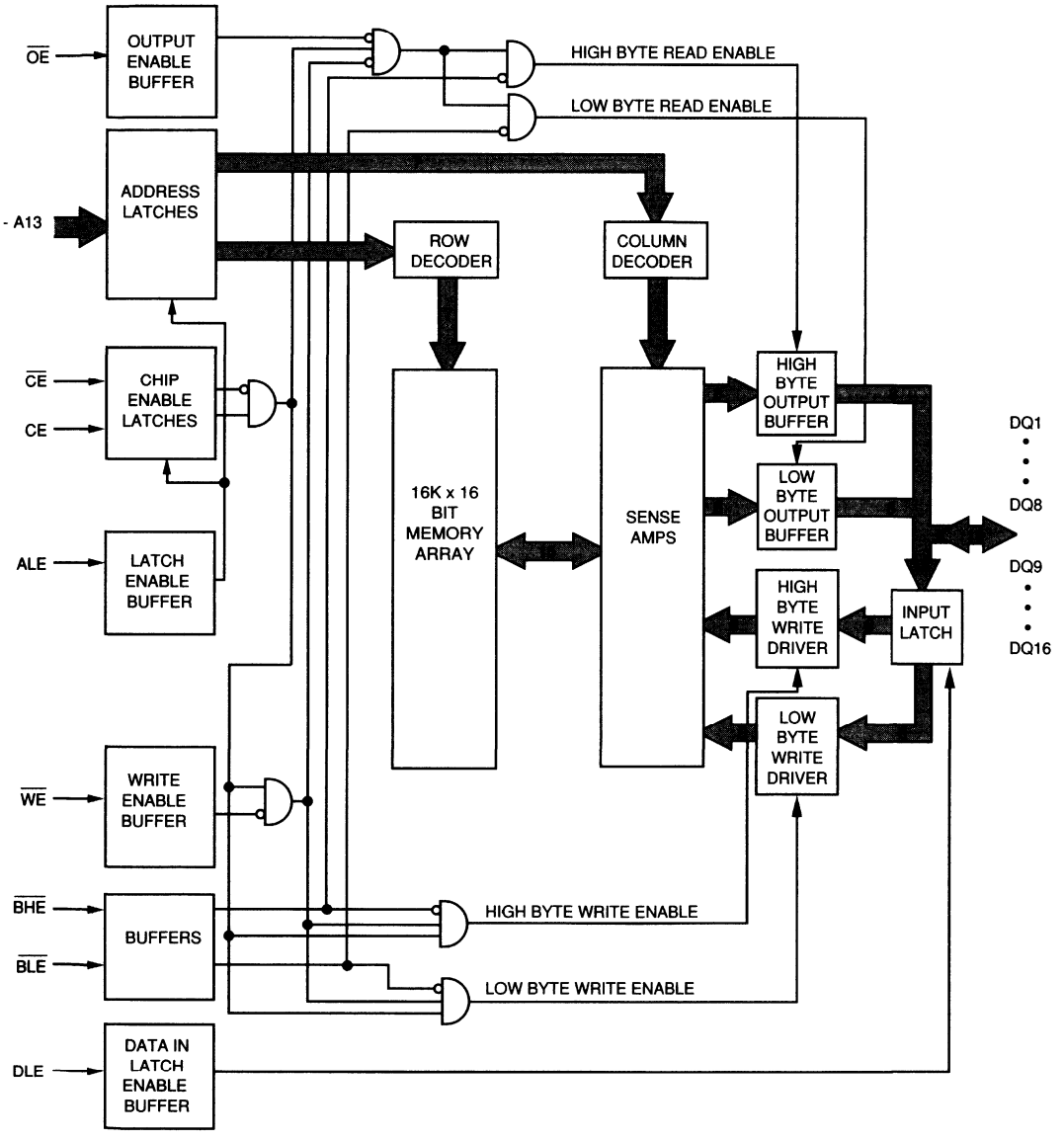
A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present on the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times and shortening the amount of time that valid data must be present.

The MT56C16K16C3 operates from a +3.3V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided for improved noise immunity.

NEW

3.3 VOLT CACHE DATA/LATCHED SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BLE}$ $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be selected, permitting direct connection in systems that provide separate chip selects for high and low bytes. When $\overline{BLE}$ is LOW, the lower byte, D1-D8, is enabled. When $\overline{BHE}$ is LOW, the upper byte, D9-D16, is enabled. The device will be in low power standby mode when both Byte Enables are inactive (HIGH) or when either Chip Enable is inactive.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration. The device will be in low power standby mode when either Chip Enable is inactive (CE= LOW or $\overline{CE}$=HIGH) or both Byte Enables are inactive.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
46, 20	NC	-	No connect: These signals are no connects (NCs). NCs are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the required setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +3.3V ±0.3V
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±0.3V
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

NEW

3.3 VOLT CACHE DATA/LATCHED SRAM

TRUTH TABLE

OPERATION		CE	$\overline{CE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	ALE	DLE	$\overline{OE}$	DQ
Deselected (low power standby)		L	X	X	X	X	X	X	X	High-Z
Deselected (low power standby)		X	H	X	X	X	X	X	X	High-Z
Deselected (low power standby)		X	X	X	H	H	X	X	X	High-Z
READ		H	L	H	L	L	H	X	H	High-Z
WORD READ		H	L	H	L	L	H	X	L	Q1-Q16
LATCHED WORD READ		H	L	H	L	L	L	X	L	Q1-Q16
BYTE READ	(DQ1-DQ8)	H	L	H	L	H	H	X	L	D1-D8
LATCHED BYTE READ	(DQ1-DQ8)	H	L	H	L	H	L	X	L	D1-D8
BYTE READ	(DQ9-DQ16)	H	L	H	H	L	H	X	L	D9-D16
LATCHED BYTE READ	(DQ9-DQ16)	H	L	H	H	L	L	X	L	D9-D16
WORD WRITE transparent data-in	(DQ1-DQ16)	H	L	L	L	L	H	H	X	D1-D16
LATCHED WORD WRITE transparent data-in	(DQ1-DQ16)	H	L	L	L	L	L	H	X	D1-D16
WORD WRITE latched data-in	(DQ1-DQ16)	H	L	L	L	L	H	L	X	D1-D16
LATCHED WORD WRITE latched data-in	(DQ1-DQ16)	H	L	L	L	L	L	L	X	D1-D16
BYTE WRITE transparent data-in	(DQ1-DQ8)	H	L	L	L	H	H	H	X	D1-D8
LATCHED BYTE WRITE transparent data-in	(DQ1-DQ8)	H	L	L	L	H	L	H	X	D1-D8
BYTE WRITE transparent data-in	(DQ9-DQ16)	H	L	L	H	L	H	H	X	D9-D16
LATCHED BYTE WRITE transparent data-in	(DQ9-DQ16)	H	L	L	H	L	L	H	X	D9-D16
BYTE WRITE latched data-in	(DQ1-DQ8)	H	L	L	L	H	H	L	X	D1-D8
LATCHED BYTE WRITE latched data-in	(DQ1-DQ8)	H	L	L	L	H	L	L	X	D1-D8
BYTE WRITE latched data-in	(DQ9-DQ16)	H	L	L	H	L	H	L	X	D9-D16
LATCHED BYTE WRITE latched data-in	(DQ9-DQ16)	H	L	L	H	L	L	L	X	D9-D16

NOTE:
1. Latched inputs (Addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to Vcc+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V; Vss = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; CE ≥ V_{IH}; Vcc = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	70	100	mA	3
Power Supply Current: Standby	CE ≤ V_{IL}; $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ ≥ V_{IH}; Vcc = MAX; Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	15	30	mA	
	$\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ ≥ Vcc - 0.2V; CE ≤ Vss +0.2V Vcc = MAX; V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	3	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 3.3V ±0.3V)

		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address Latch							
Latch cycle time	^tLC	20		25		ns	
Latch HIGH time	^tLEH	5		5		ns	
Address/Chip Enable setup to latch LOW	^tLS	2		2		ns	
Address/Chip Enable hold from latch LOW	^tLH	3		3		ns	
Address/Chip Enable setup to latch HIGH	^tLHS	0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		ns	6, 7
Latch HIGH to output in High-Z	^tHZL	2	12	2	12	ns	6, 7
READ Cycle							
READ cycle time	^tRC	20		25		ns	
Address access time	^tAA		20		25	ns	
Chip Enable access time	^tACE		20		25	ns	
Output hold from address change	^tOH	4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		ns	6, 7
Chip disable to output in High-Z	^tHZCE	2	12	2	12	ns	6, 7
Output Enable access time	^tAOE		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE	2	8	2	10	ns	6, 7
Byte Enable access time	^tABE		20		25	ns	
Byte Enables to output in Low-Z	^tLZBE	2		2		ns	6, 7
Byte Disables to output in High-Z	^tHZBE	2	12	2	12	ns	6, 7
WRITE Cycle							
WRITE cycle time	^tWC	20		25		ns	
Chip Enable to end of write	^tCW	15		20		ns	
Address valid to end of write	^tAW	15		20		ns	
Address setup time	^tAS	0		0		ns	
Address hold from end of write	^tAH	3		3		ns	
WRITE pulse width	^tWP	15		20		ns	
Data setup time	^tDS	8		10		ns	
Data hold time	^tDH	0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		4		ns	6, 7
Write Enable to output in High-Z	^tHZWE	0	10	0	10	ns	6, 7
Byte Enable to end of write	^tBW	15		20		ns	
Data setup to DLE LOW	^tDLS	1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		ns	9
DLE HIGH to end of write	^tDLW	8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		ns	
ALE HIGH setup time to Write Enable LOW	^tLWS	0		0		ns	
ALE HIGH to end of write	^tLW	15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

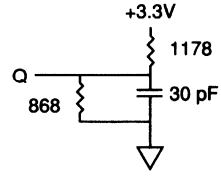


Fig. 1 OUTPUT LOAD EQUIVALENT

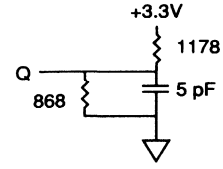


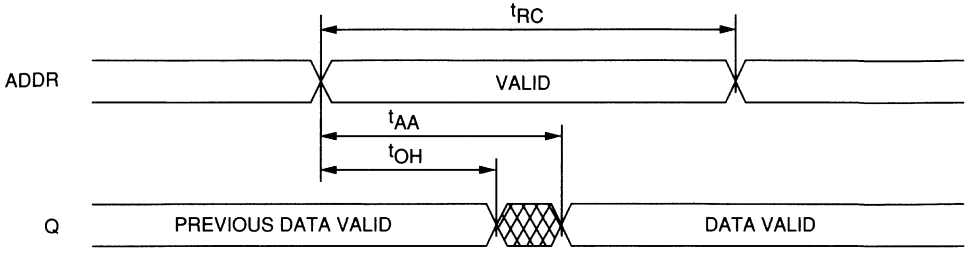
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZOE is less than ^{t}LZOE, and ^{t}HZBE is less than ^{t}LZBE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to, or coincident with, the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.
15. If output enable is inactive (HIGH) the output will be in High-Z instead of undefined.
16. $\overline{BHE}$ and $\overline{BLE}$ are LOW.

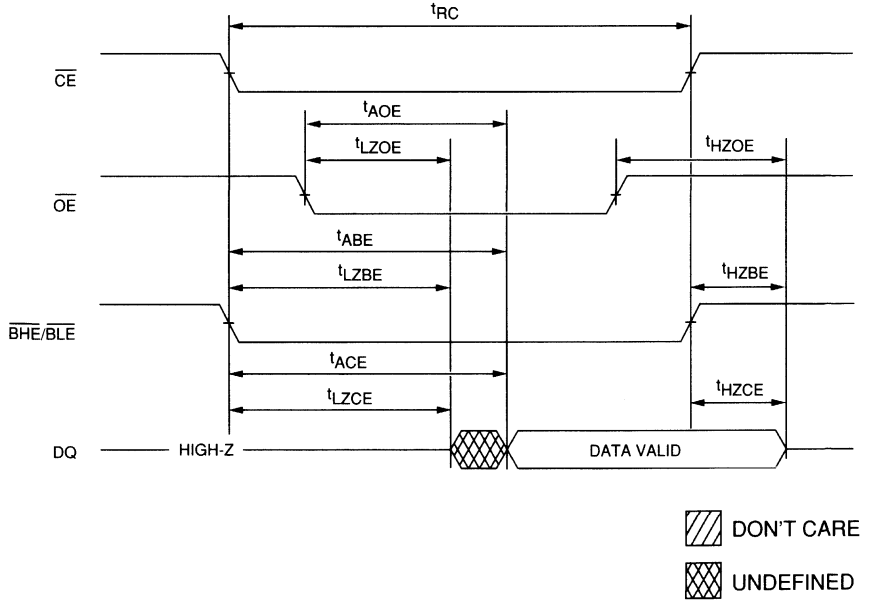
READ CYCLE NO. 1 [11, 12, 16]

(ALE = DLE = HIGH)

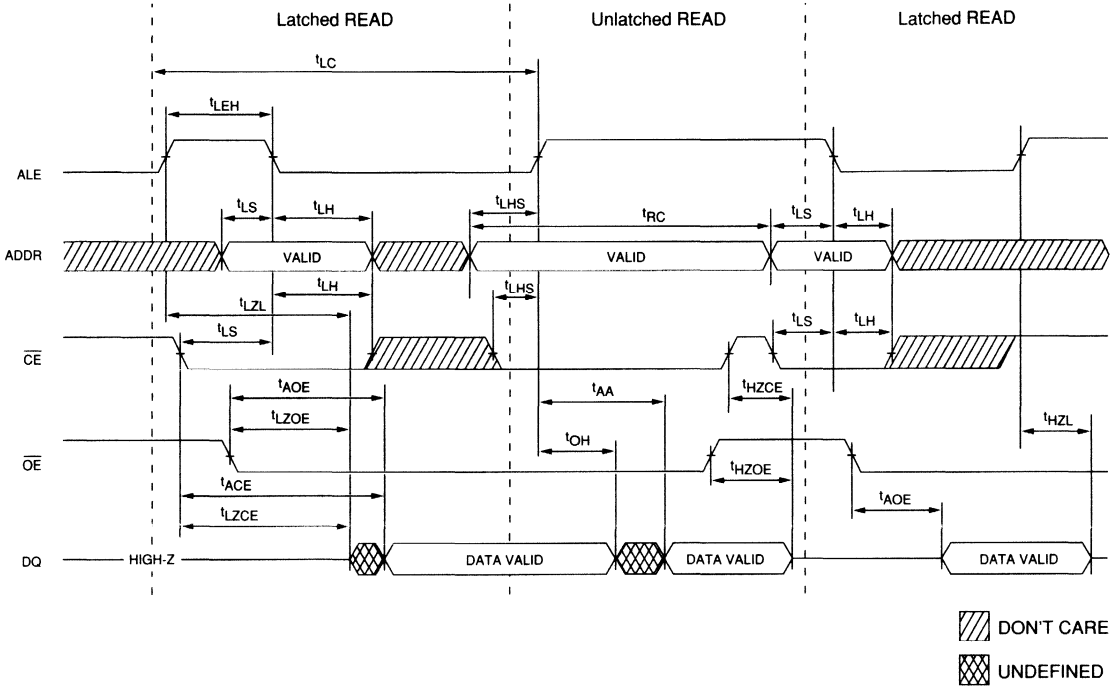


READ CYCLE NO. 2 [7, 11, 13, 14]

(ALE = DLE = HIGH)



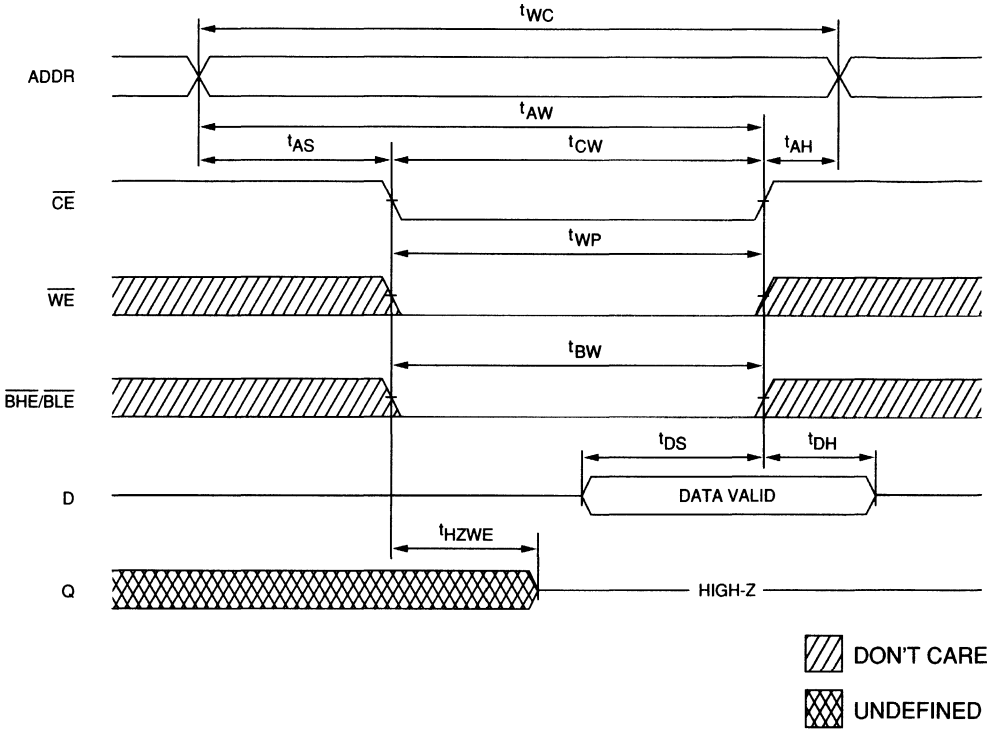
READ CYCLE NO. 3 [7, 11, 14, 16]
(DLE = HIGH)



NEW ■ 3.3 VOLT CACHE DATA/LATCHED SRAM

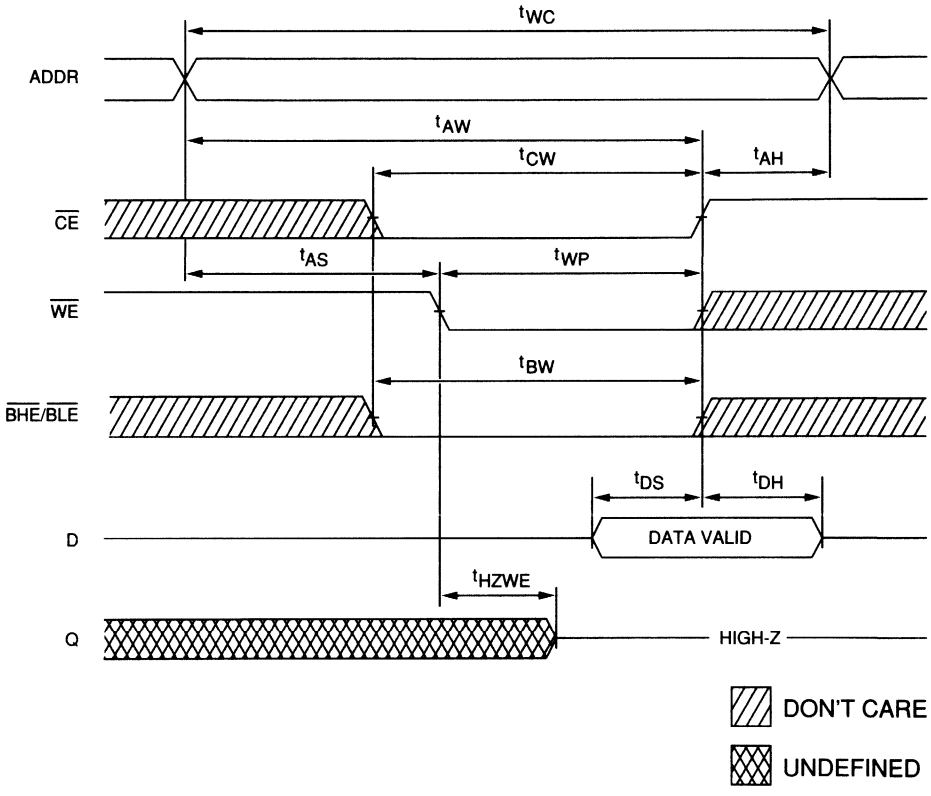
WRITE CYCLE NO. 1 [10, 14, 15]

Chip Enable Controlled
(ALE = DLE = HIGH)



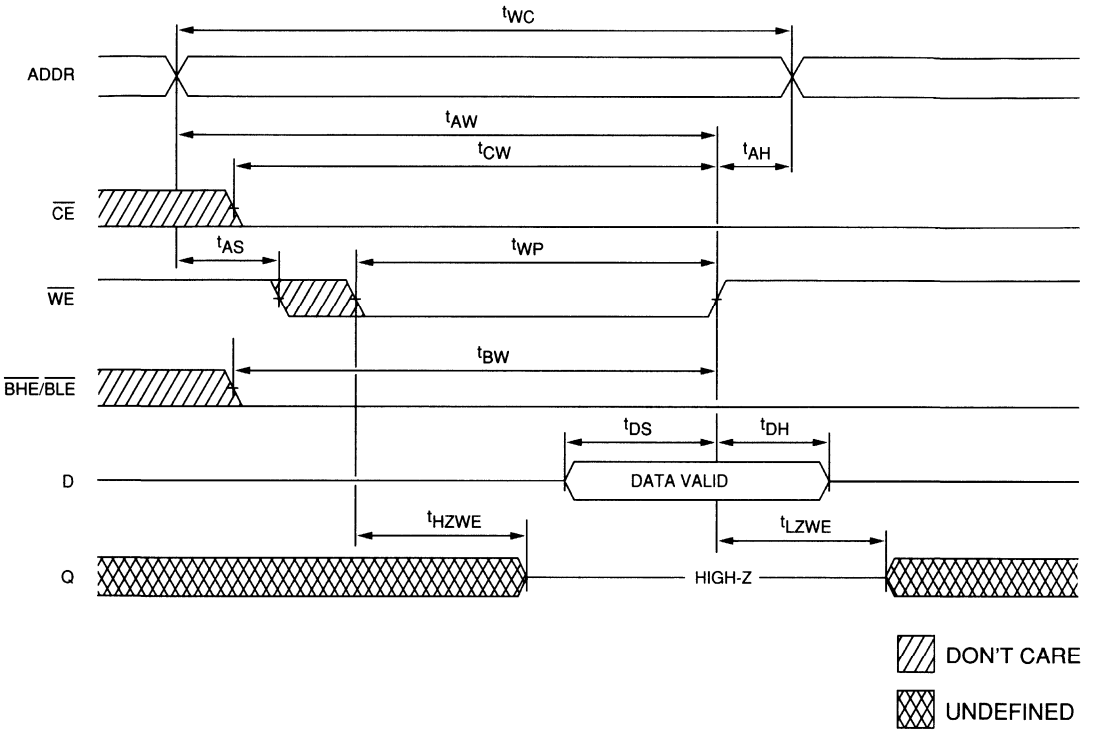
WRITE CYCLE NO. 2 [10, 14, 15]

Write Enable Initiated / Chip Enable Terminated
(ALE = DLE = HIGH)



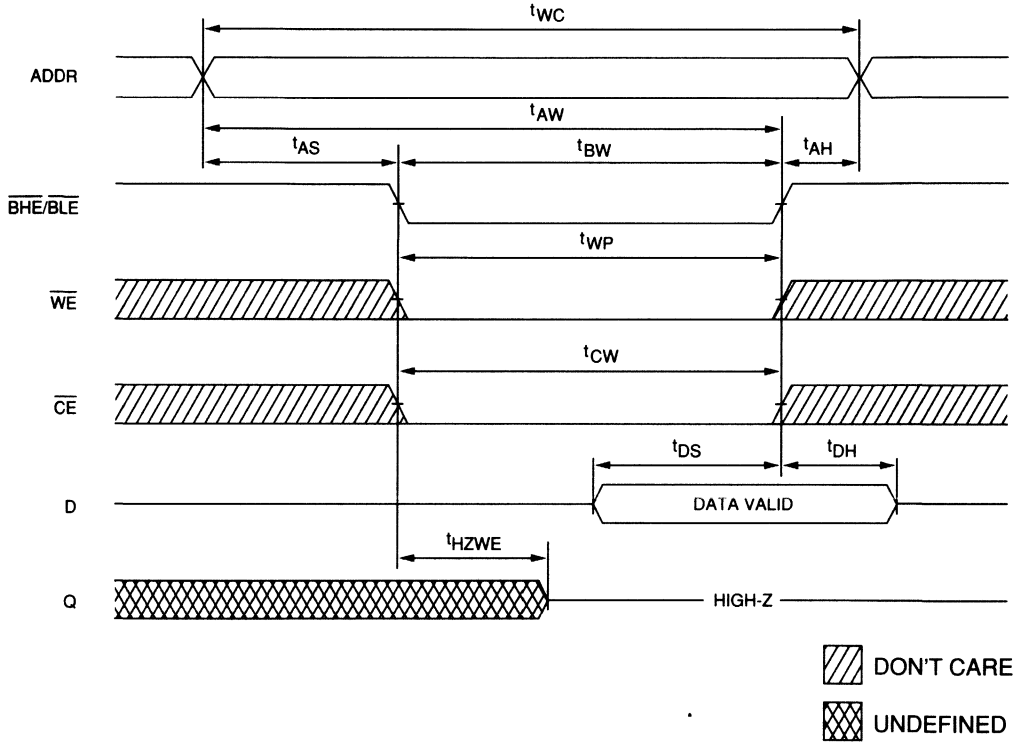
WRITE CYCLE NO. 3 [7, 10, 14, 15]

Write Enable Controlled
(ALE = DLE = HIGH)



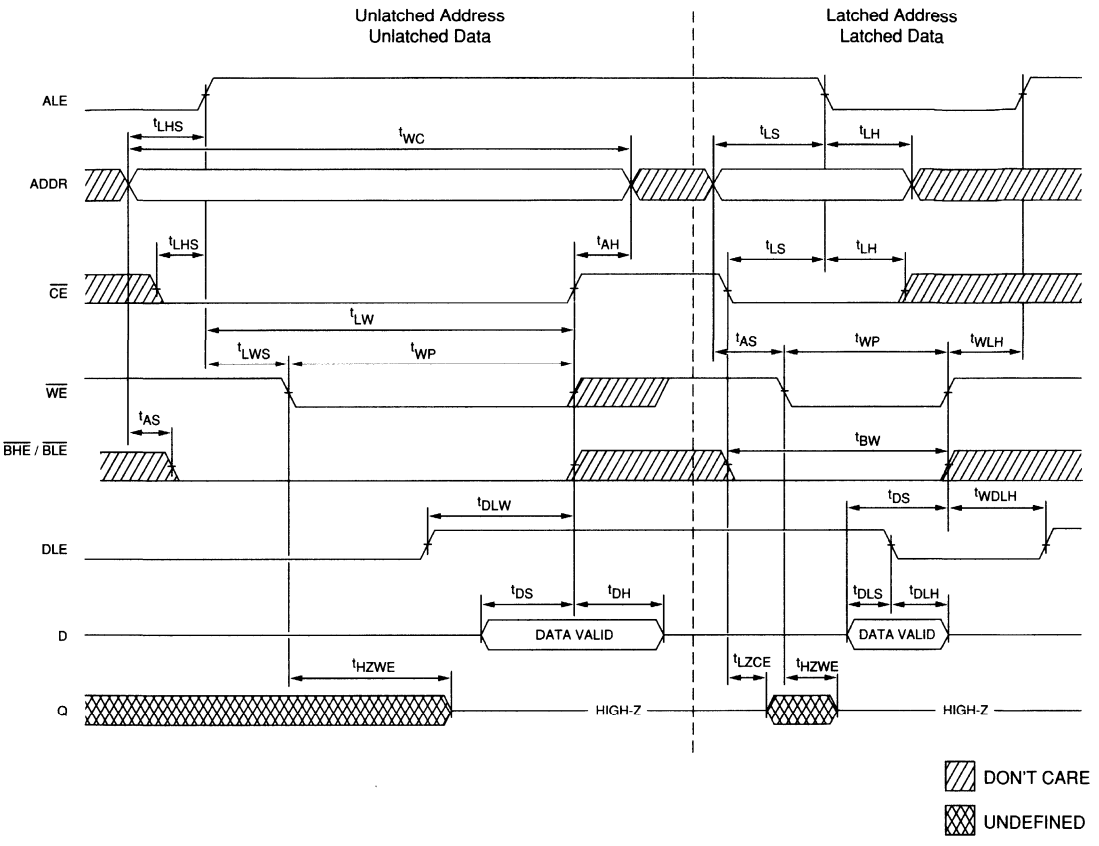
WRITE CYCLE NO. 4 [10, 14, 15]

Byte Enable Controlled
(ALE = DLE = HIGH)



NEW ■ 3.3 VOLT CACHE DATA/LATCHED SRAM

WRITE CYCLE NO. 5 [7, 10, 14, 15]



MICRON

FIFO MEMORIES PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Cycle Time (ns)	Package/Number of Pins		Page
				PDIP	PLCC	
512 x 9	Expandable Depth and Width	MT52C9005	15, 20, 25, 35	28	32	7-1
512 x 9	Programmable Flag Expandable Depth and Width	MT52C9007	15, 20, 25, 35	28	32	7-13
1K x 9	Expandable Depth and Width	MT52C9010	15, 20, 25, 35	28	32	7-29
1K x 9	Programmable Flag Expandable Depth and Width	MT52C9012	15, 20, 25, 35	28	32	7-41
2K x 9	Expandable Depth and Width	MT52C9020	15, 20, 25, 35	28	32	7-57
2K x 9	Programmable Flag Expandable Depth and Width	MT52C9022	15, 20, 25, 35	28	32	7-69
4K x 9	Expandable Depth and Width	MT52C4K9A1	15, 20, 25, 35	28	32	7-85
4K x 9	Programmable Flag Expandable Depth and Width	MT52C4K9E5	15, 20, 25, 35	28	32	*
8K x 9	Expandable Depth and Width	MT52C8K9B2	15, 20, 25, 35	28	32	7-85
8K x 9	Programmable Flag Expandable Depth and Width	MT52C8K9F6	15, 20, 25, 35	28	32	*
512 x 18	Synchronous FIFO with clocked, registered I/O	MT53C51218A1	15, 20, 25, 35	-	68	7-97
1K x 18	Synchronous FIFO with clocked, registered I/O	MT53C1K18B2	15, 20, 25, 35	-	68	7-97
2K x 18	Synchronous FIFO with clocked, registered I/O	MT53C2K18C3	15, 20, 25, 35	-	68	7-97
4K x 18	Synchronous FIFO with clocked, registered I/O	MT53C4K18D4	15, 20, 25, 35	-	68	7-97

NOTE: 1. Automotive and industrial temperature specifications begin on page 7-115.
2. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

*Consult factory for availability and data sheet.

FIFO

512 x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag capability in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin- and function-compatible with higher-density standard FIFOs

OPTIONS — MARKING

- Timing

15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35

- Packages

Plastic DIP (300 mil)	None
PLCC	EJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

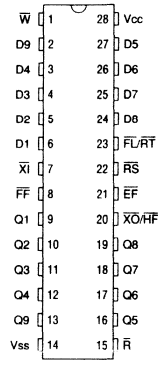
- Temperature

Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT

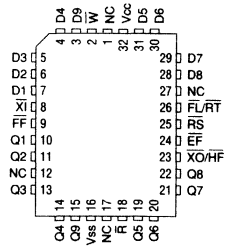
- Part Number Example: MT52C9005EJ-35 IT

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



32-Pin PLCC
(SC-1)



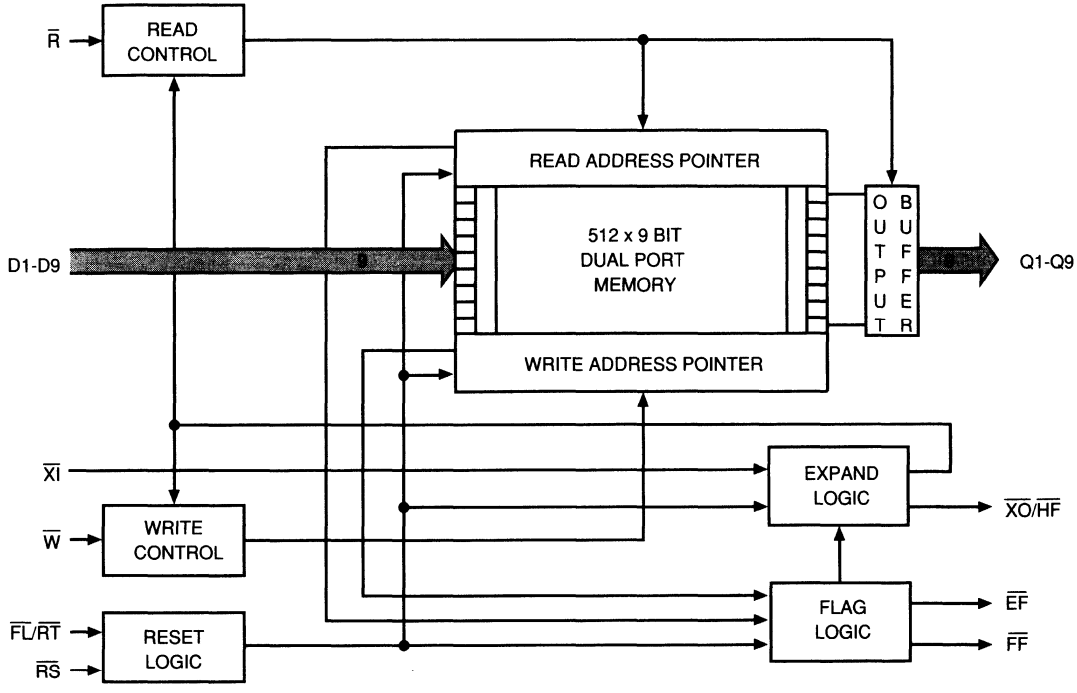
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO may be expanded by cascading multiple devices. Also, the MT52C9005 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K and 2K FIFOs provides a single-chip, depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



FIFO

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$, if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied LOW for the first FIFO in the chain, and tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical READ. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than half-full; will stay LOW until the FIFO becomes half-full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9005 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$ when discussing the half-full flag.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is connected to $\overline{XO}$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the final empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (512/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9005 allows the receiving device to request that the data read earlier from the FIFO be repeated, when less than 512 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.

FIFO

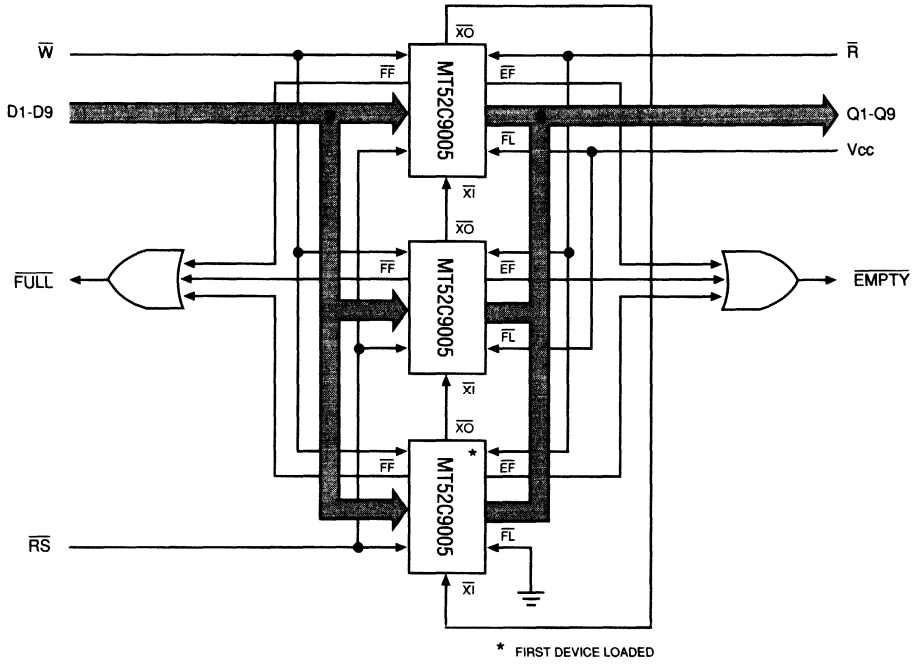


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9005s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9005. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}/\overline{RT}$/DIR= First Load/Retransmit; $\overline{EF}$ = Empty Flag Output; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	140	130	120	110	mA	3
Power Supply Current: Standby	W, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

FIFO

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^tA		15		20		25		35	ns	
READ cycle time	^tRC	25		30		35		45		ns	
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	6
READ LOW to Low-Z	^tRLZ	3		3		3		3		ns	
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RESET cycle time	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
READ HIGH to RESET HIGH	^tRRS	15		20		25		35		ns	
WRITE HIGH to RESET HIGH	^tWRS	15		20		25		35		ns	
RETRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RETRANSMIT pulse width	^tRT	15		20		25		35		ns	
RETRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RETRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET to $\overline{AEF}$, $\overline{EF}$ LOW	^tEFL		25		30		35		45	ns	
RESET to $\overline{AEF}$, $\overline{HF}$, $\overline{FF}$ HIGH	^tHFH, ^tFFH		25		30		35		45	ns	
READ LOW to $\overline{EF}$ LOW	^tREF		20		20		25		30	ns	
READ HIGH to $\overline{FF}$ HIGH	^tRFF		20		20		25		30	ns	
WRITE LOW to $\overline{FF}$ LOW	^tWFF		20		20		25		30	ns	
WRITE HIGH to $\overline{EF}$ HIGH	^tWEF		20		20		25		30	ns	
WRITE LOW to $\overline{HF}$ LOW	^tWHF		25		30		35		45	ns	
READ HIGH to $\overline{HF}$ HIGH	^tRHF		25		30		35		45	ns	
READ HIGH after $\overline{EF}$ HIGH	^tRPE	15		20		25		35		ns	5
WRITE HIGH after $\overline{FF}$ HIGH	^tWPF	15		20		25		35		ns	5
READ/WRITE to $\overline{XO}$ LOW	^tXOL		15		20		25		35	ns	
READ/WRITE to $\overline{XO}$ HIGH	^tXOH		15		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time	^tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	^tXIR	10		10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

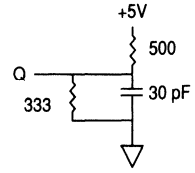
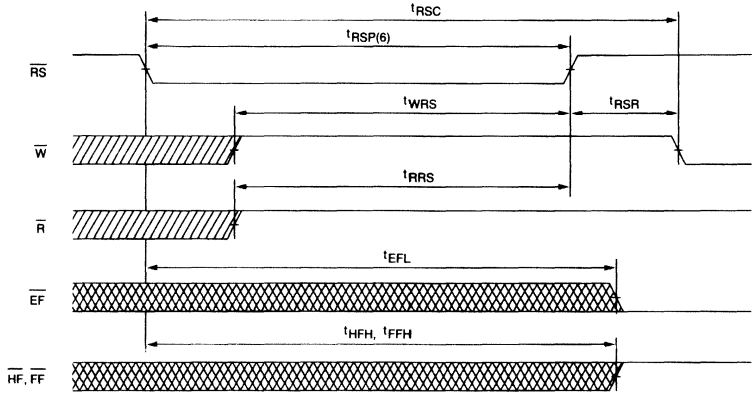
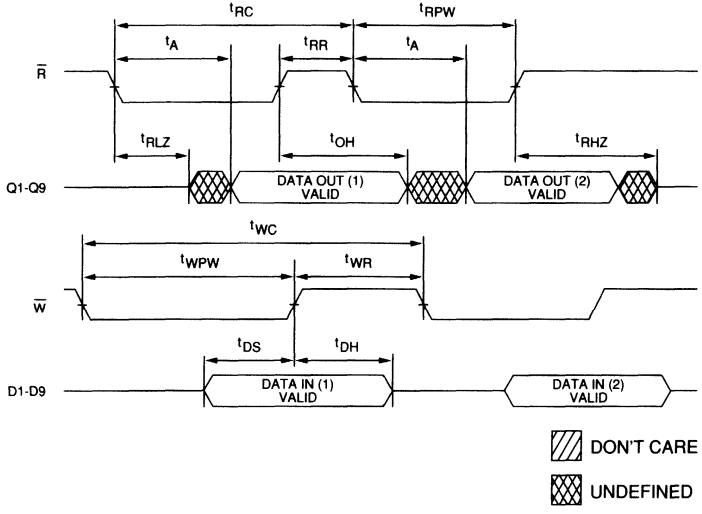


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET

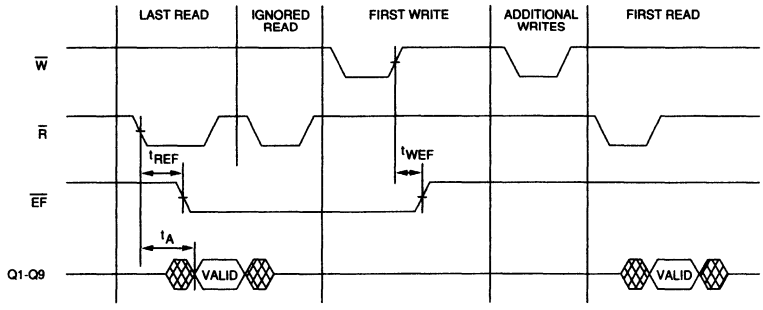


ASYNCHRONOUS READ AND WRITE

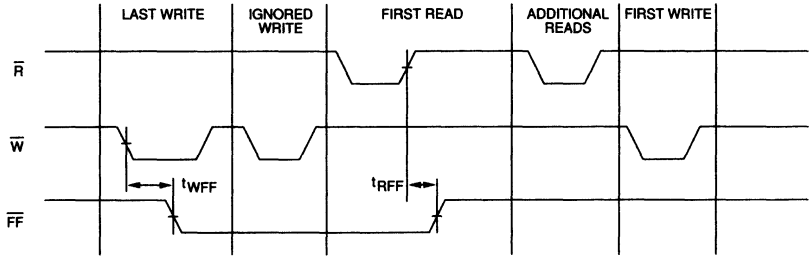


FIFO

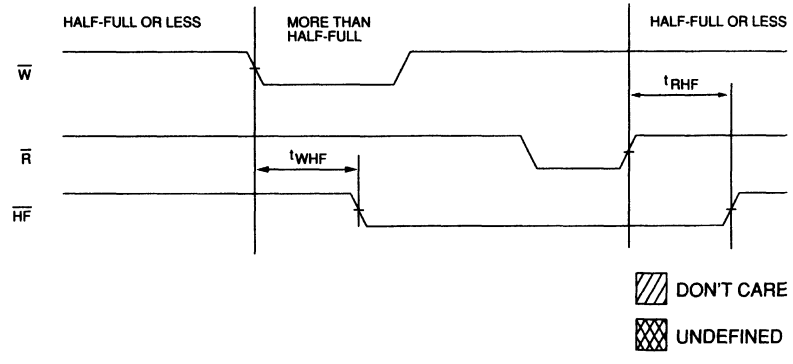
EMPTY FLAG



FULL FLAG

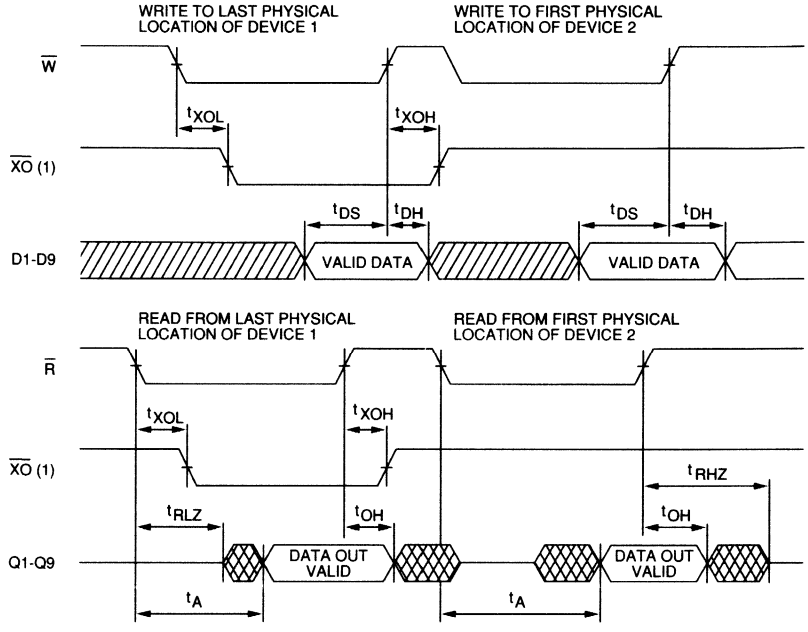


HALF-FULL FLAG



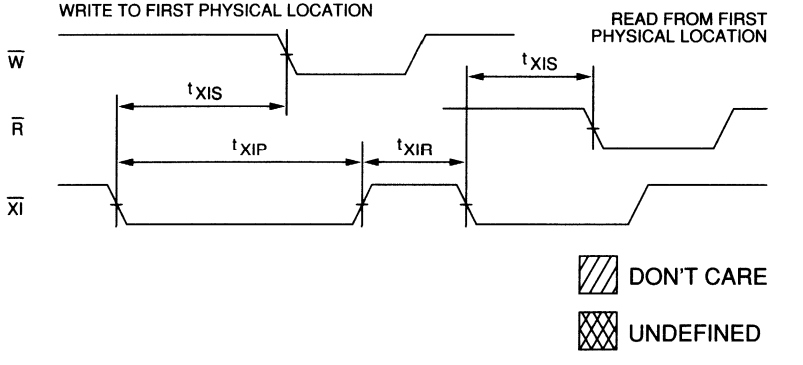
FIFO

EXPANSION MODE ($\overline{XO}$)



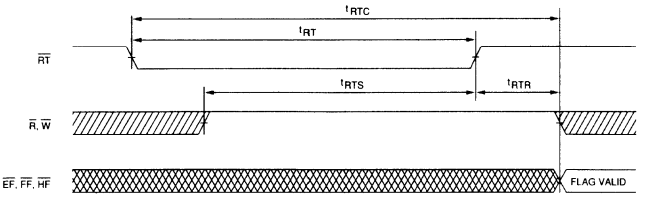
NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

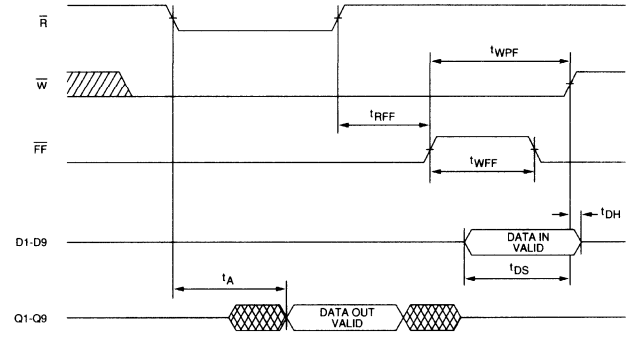


FIFO

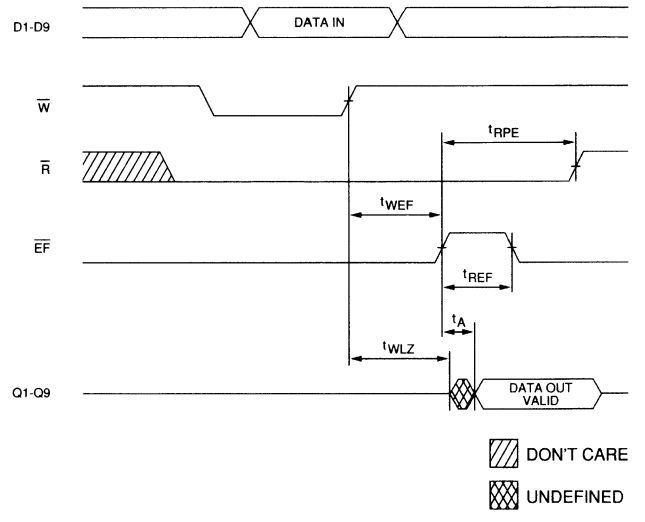
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



FIFO

FIFO

512 x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost-Full and Almost-Empty Flags
- Programmable Half-Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in SINGLE DEVICE mode
- Fully expandable by width and depth
- Pin- and function-compatible with higher-density standard FIFOs

OPTIONS — MARKING

- Timing

15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35

- Packages

Plastic DIP (300 mil)	None
PLCC	EJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

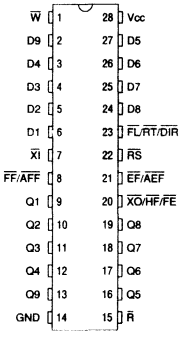
- Temperature

Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT

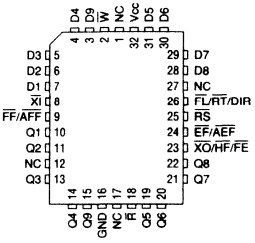
- Part Number Example: MT52C9007EJ-25 AT

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



32-Pin PLCC (SC-1)



GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

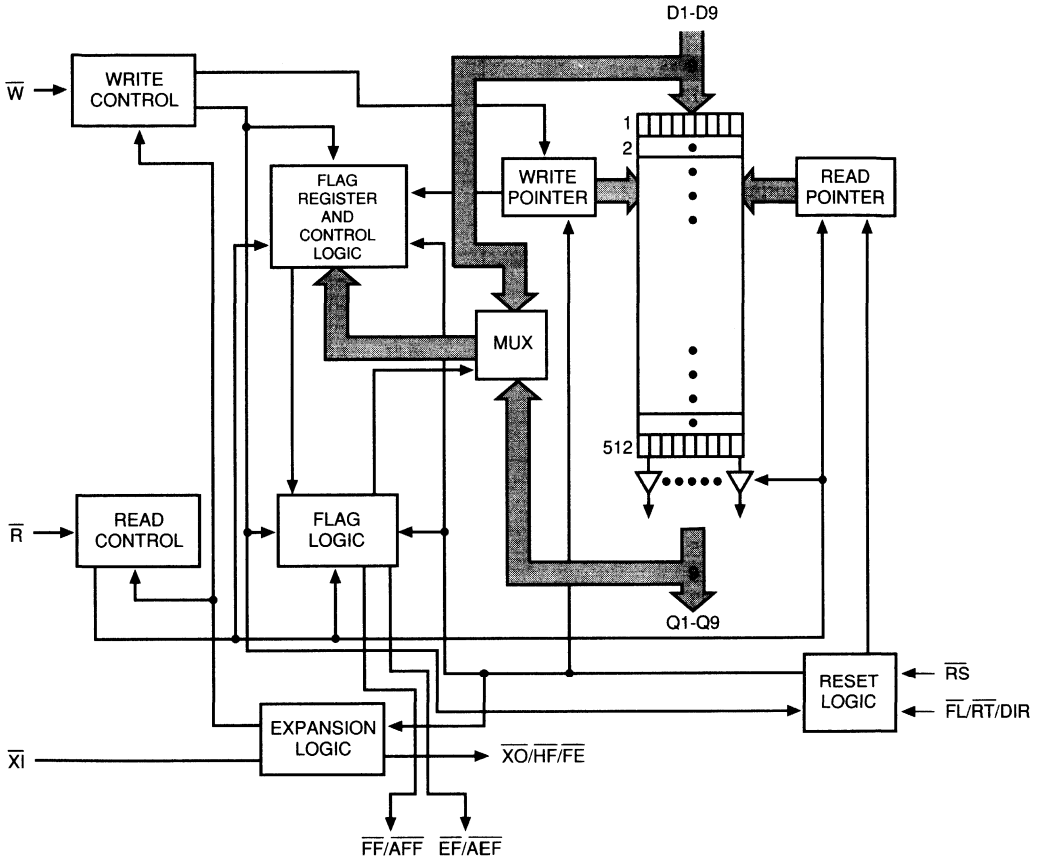
Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9007 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9007 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 7-17). In configured mode, up to three flags are provided. The first two are the almost-empty flag ($\overline{AEF}$) and the almost-full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FF}$, $\overline{EF}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO may be expanded by cascading multiple devices. Also, the MT52C9007 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K and 2K FIFOs provides a single-chip depth-expansion solution.

FIFO

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are in High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion-In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in SINGLE DEVICE mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF}/\overline{AEF}$	Output	Empty Flag/Almost-Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost-Empty Flag output. This pin is active LOW.
9	8	$\overline{FF}/\overline{AFF}$	Output	Full Flag/Almost-Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost-Full Flag output. This pin is active LOW.
23	20	$\overline{XO}/\overline{HF}/\overline{FE}$	Output	Expansion Out/Half Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost-Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO}/\overline{HF}$ in NONCONFIGURED mode.
10, 11, 13, 14, 19, 20, 21, 22,15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input LOW. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9007 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{XO}/\overline{HF}/\overline{FE}$ pin will be shown as $(\overline{XO})/\overline{HF}/(\overline{FE})$ when discussing half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins is latched on the rising edge. If the location to be written is the final empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While the $\overline{FF}$ is asserted, all writes are inhibited, and previously stored data is unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{R}$. Valid data will appear ^{t}A after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read from a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9007 allows the receiving device to request that data read earlier from the FIFO be repeated, when less than 512 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}/(DIR)$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{FL})/\overline{RT}/(DIR)$ is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a flow-through READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

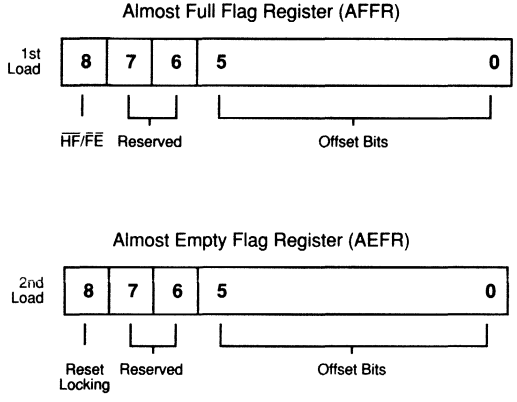
FIFO

REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost-empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

Two 9-bit internal registers have been provided for flag configuration. One is the almost-full flag register (AFFR) and the other is the almost-empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9007



Note that bits 0-5 are used for setting the offset value. The offset value ranges from 1 to 63 increments. Each increment value corresponds to 2 words. This provides a maximum offset of 126 words.

Bits 6 and 7 are reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{FE}$ pin. When this bit is set LOW, the HF/$\overline{FE}$ pin is configured as an $\overline{HF}$ flag output. When it is set HIGH, the HF/$\overline{FE}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers may be reconfigured without device reset. The part may be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^tRS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL APPLICATIONS

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9007s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).

FIFO

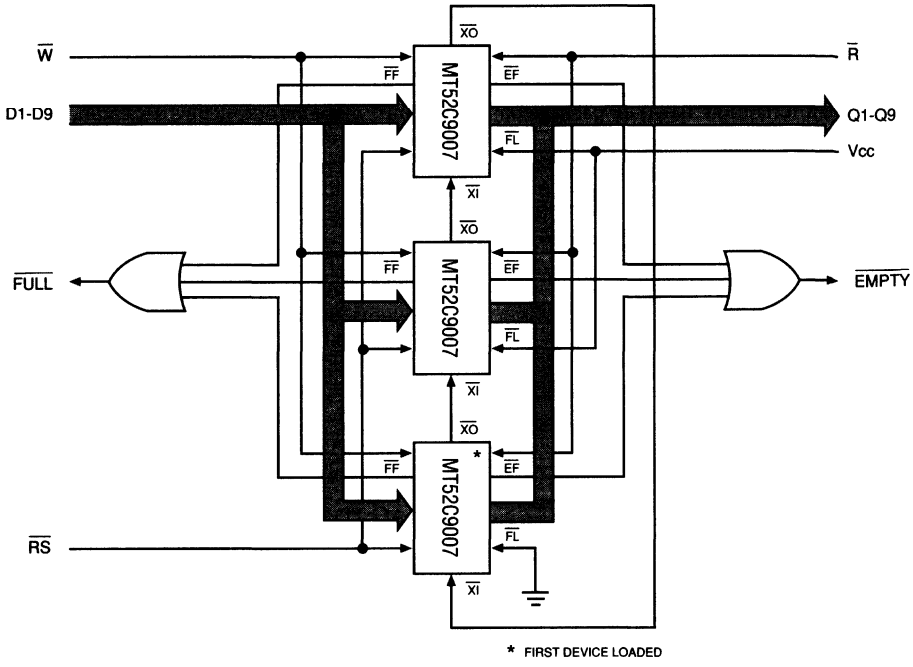


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9007s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9007. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

FIFO

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}/\overline{RT}$/DIR = First Load/Retransmit; $\overline{EF}$ = Empty Flag Output; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	140	130	120	110	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^tRF		40		33.3		28.5		22.2	MHz	
READ cycle time	^tRC	25		30		35		45		ns	
Access time	^tA		15		20		25		35	ns	6
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	
READ LOW to Low-Z	^tRLZ	3		3		3		3		ns	7
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5, 7
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RETRANSMIT Cycle											
RESTRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RESTRANSMIT pulse width	^tRT	15		20		25		35		ns	
RESTRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RESTRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^tRS	15		20		25		35		ns	
RESET and register programming cycle time	^tRSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^tRDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^tRW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^tWRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^tRRS	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{R}/\overline{W}$ to $\overline{XO}$ LOW	tXOL		15		20		25		35	ns	
$\overline{R}/\overline{W}$ to $\overline{XO}$ HIGH	tXOH		15		20		25		35	ns	
$\overline{XI}$ pulse width	tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time to $\overline{R}/\overline{W}$	tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	tXIR	10		10		10		10		ns	
Flags Timing											
$\overline{W}$ HIGH to Flags Valid	tWFV		15		15		15		15	ns	
$\overline{RS}$ to $\overline{AEF}$, $\overline{EF}$ LOW	tEFL		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{EF}$ LOW	tREF		20		20		25		30	ns	
$\overline{W}$ HIGH to $\overline{EF}$ HIGH	tWEF		20		20		25		30	ns	
$\overline{R}$ HIGH after $\overline{EF}$ HIGH	tRPE	15		20		25		35		ns	5
$\overline{RS}$ to $\overline{AFF}$, $\overline{HF}$, $\overline{FF}$ HIGH	tHFH, tFFH		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{FF}$ HIGH	tRFF		15		20		25		30	ns	
$\overline{W}$ LOW to $\overline{FF}$ LOW	tWFF		20		20		25		30	ns	
$\overline{W}$ HIGH after $\overline{FF}$ HIGH	tWPF	15		20		25		35		ns	5
$\overline{W}$ LOW to $\overline{HF}$ LOW	tWHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{HF}$ HIGH	tRHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{AFF}$ HIGH	tRAFF		25		30		35		45	ns	
$\overline{W}$ LOW to $\overline{AFF}$ LOW	tWAFF		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{AEF}$ LOW	tRAEF		25		30		35		45	ns	
$\overline{W}$ HIGH to $\overline{AEF}$ HIGH	tWAEF		25		30		35		45	ns	

FIFO

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

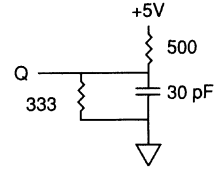
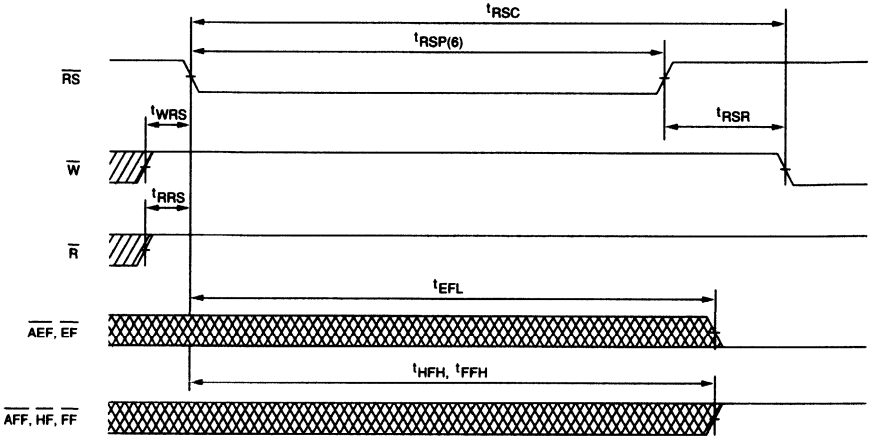


Figure 2
OUTPUT LOAD EQUIVALENT

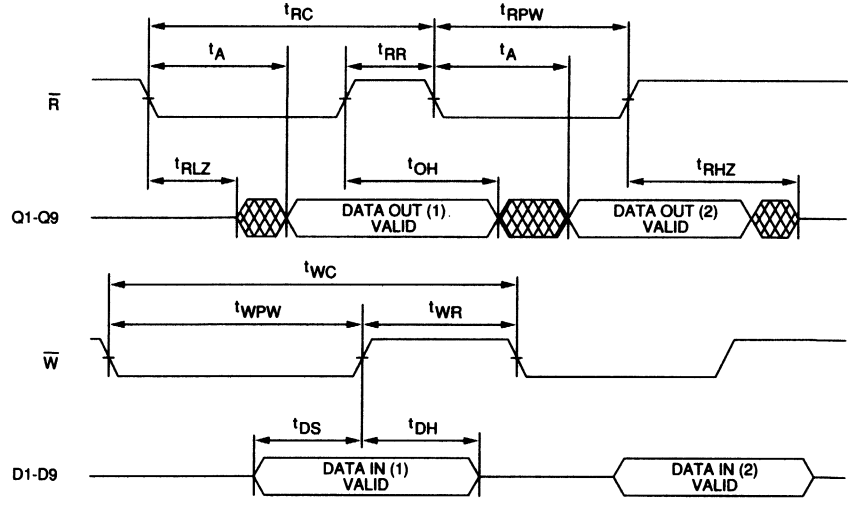
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{R}$ and DIR signals must go inactive (HIGH) coincident with $\overline{RS}$ going inactive (HIGH).
9. DIR must become valid before $\overline{W}$ goes active (LOW).

RESET
(WITH NO REGISTER PROGRAMMING)



ASYNCHRONOUS READ AND WRITE

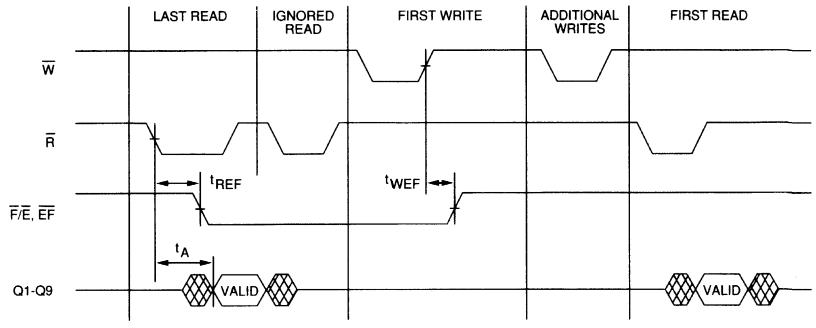


DON'T CARE

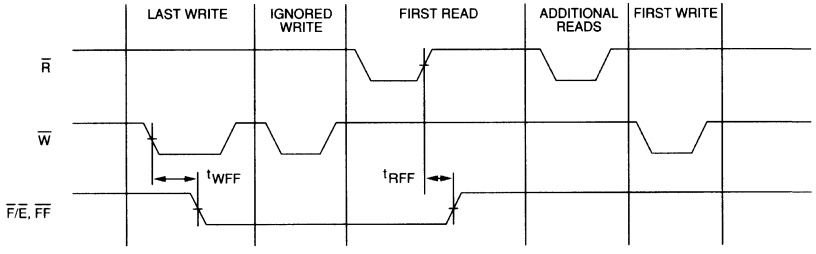
UNDEFINED

FIFO

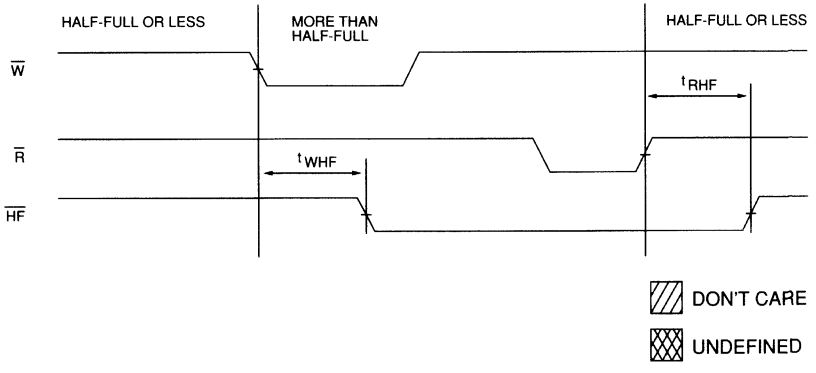
EMPTY FLAG



FULL FLAG

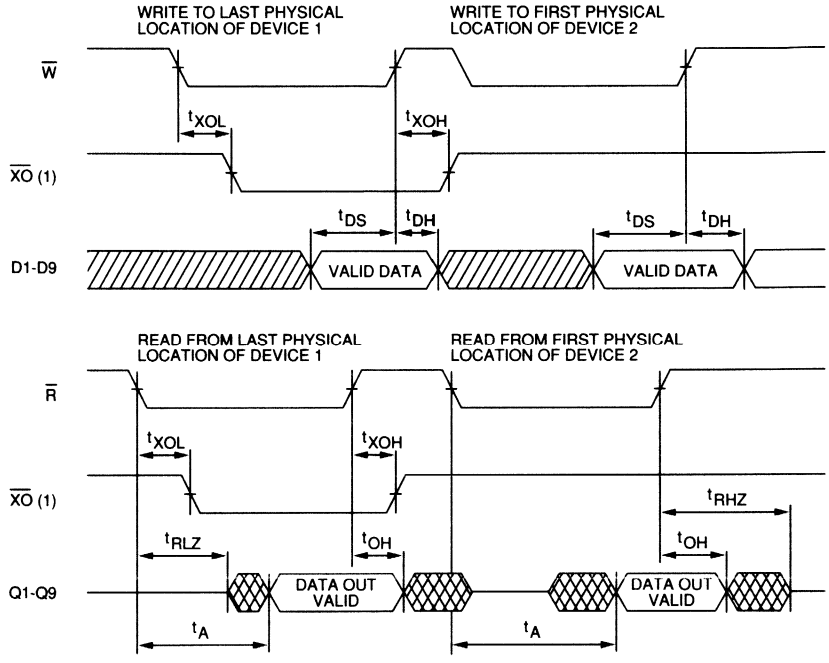


HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



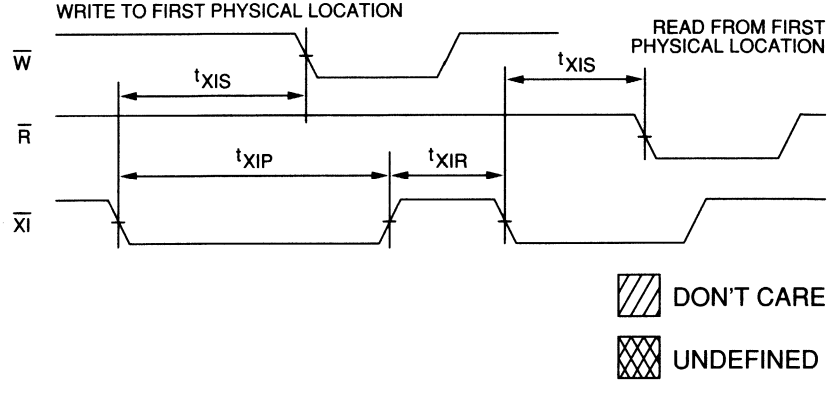
FIFO

EXPANSION MODE ($\overline{XO}$)



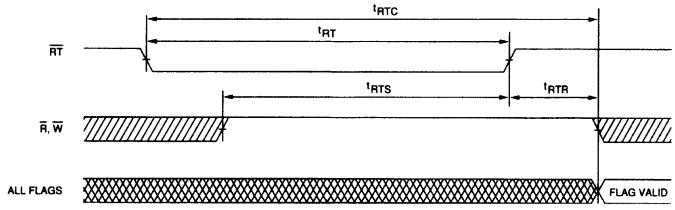
NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

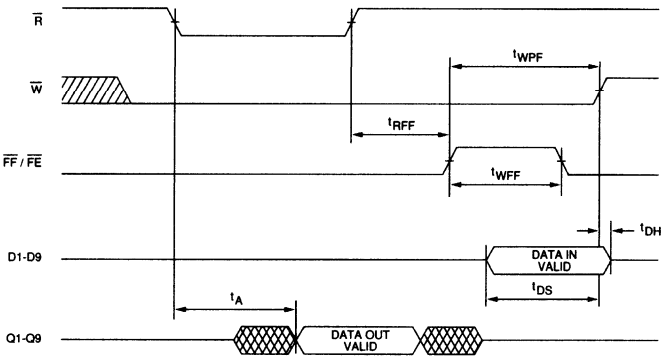


FIFO

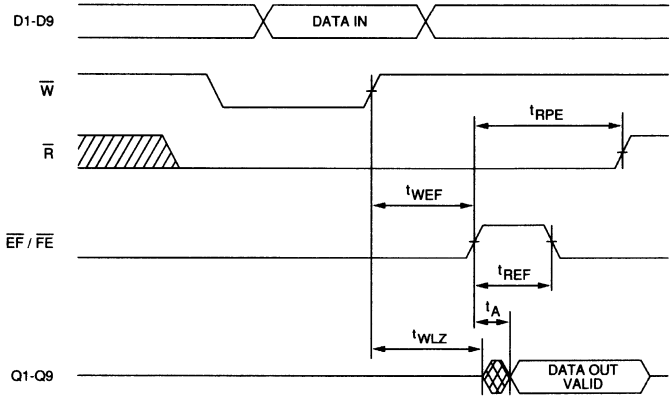
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH

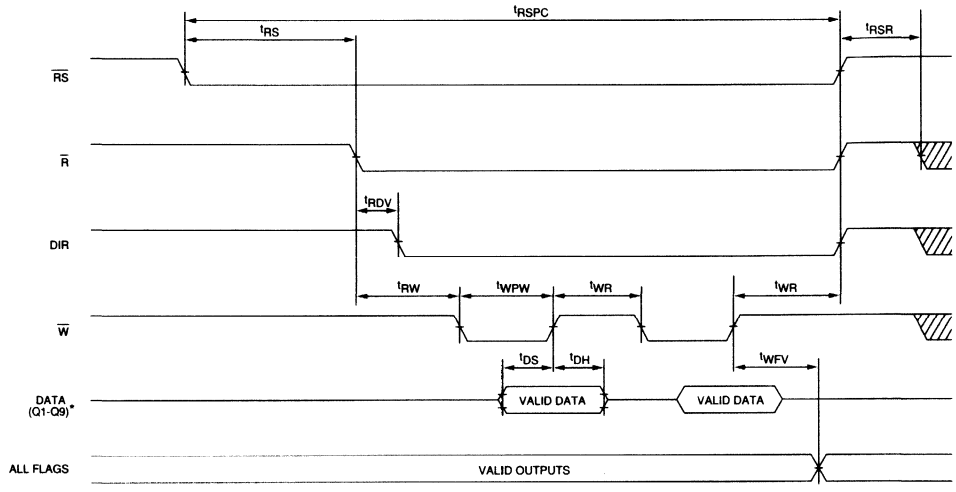


DON'T CARE

UNDEFINED

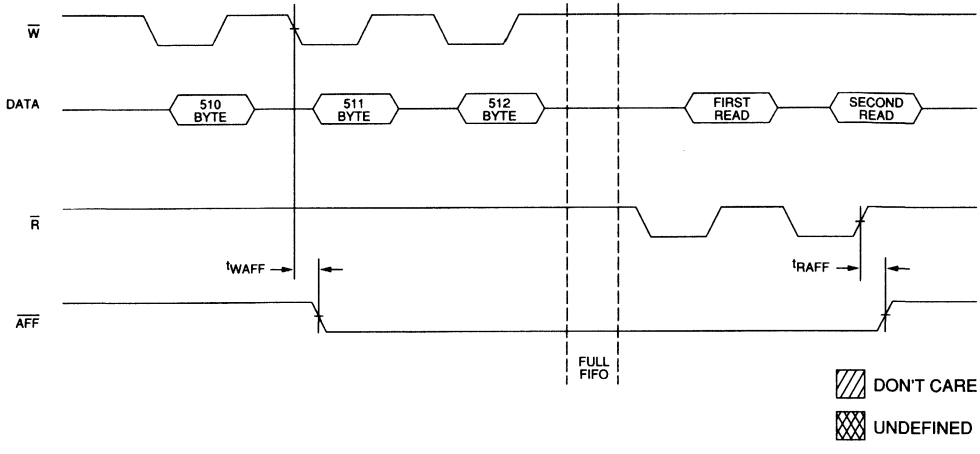
FIFO

RESET/REGISTER PROGRAMMING CYCLE TIME [8, 9]



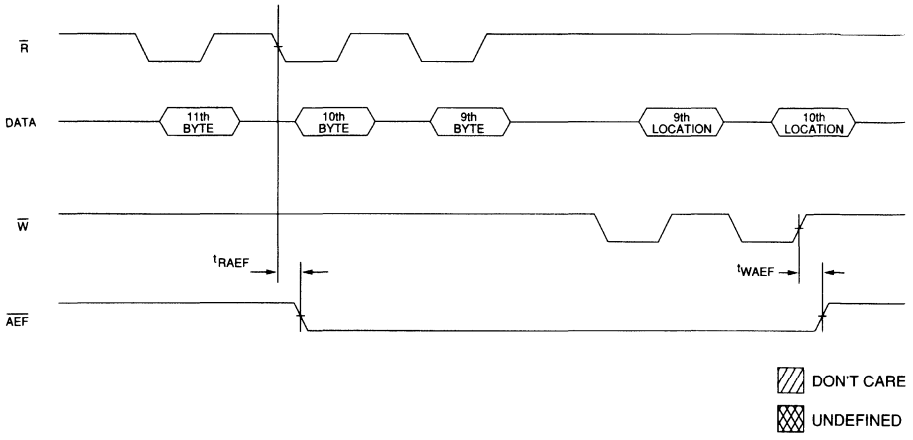
* When DIR = LOW, data is loaded from Q1-Q8; when DIR = HIGH, data is loaded from D1-D9.

ALMOST-FULL FLAG (2-BYTE OFFSET)



FIFO

ALMOST-EMPTY FLAG (10-BYTE OFFSET)



FIFO

FIFO

1K x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag capability in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin- and-function compatible with higher-density standard FIFOs

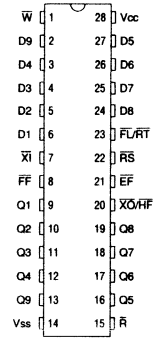
OPTIONS — MARKING

- Timing
  - 15ns access time — -15
  - 20ns access time — -20
  - 25ns access time — -25
  - 35ns access time — -35
- Packages
  - Plastic DIP (300 mil) — None
  - PLCC — EJ

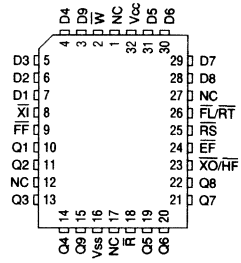
  NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
- Part Number Example: MT52C9010-20

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



32-Pin PLCC
(SC-1)



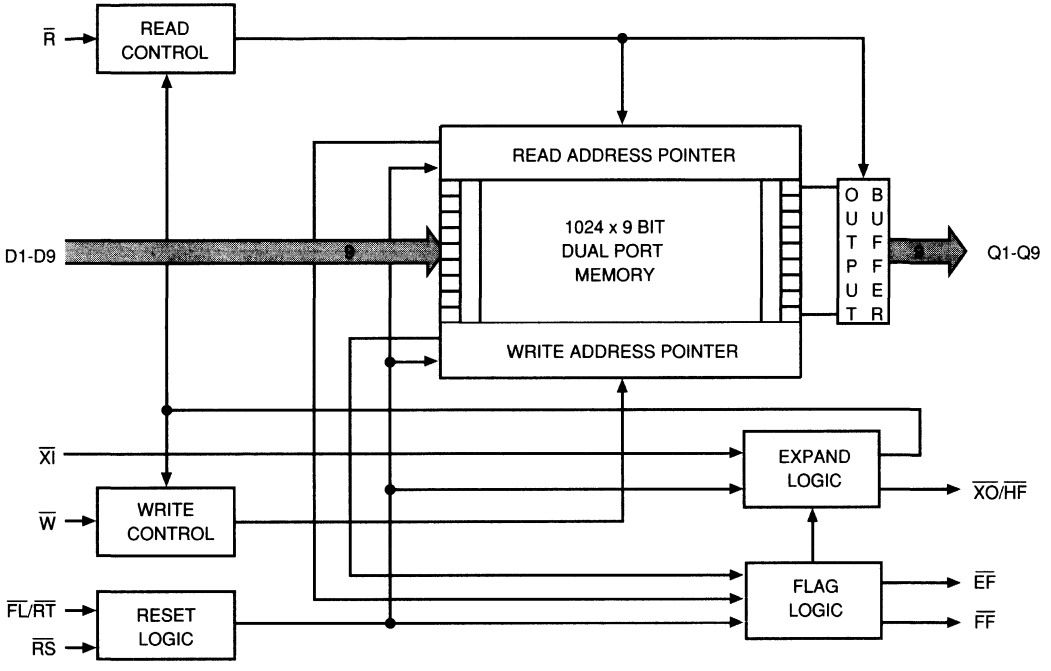
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO may be expanded by cascading multiple devices. Also, the MT52C9010 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with the 2K x 9 FIFO provides a single-chip, depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



FIFO

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$, if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied low for the first FIFO in the chain, tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical READ. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than half-full; will stay LOW until the FIFO becomes half-full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9010 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$ when discussing the half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is tied to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the final empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (1,024/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9010 allows the receiving device to request that the data read earlier from the FIFO be repeated, when less than 1,024 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume (useful only in SINGLE mode with no wraparound).

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.

FIFO

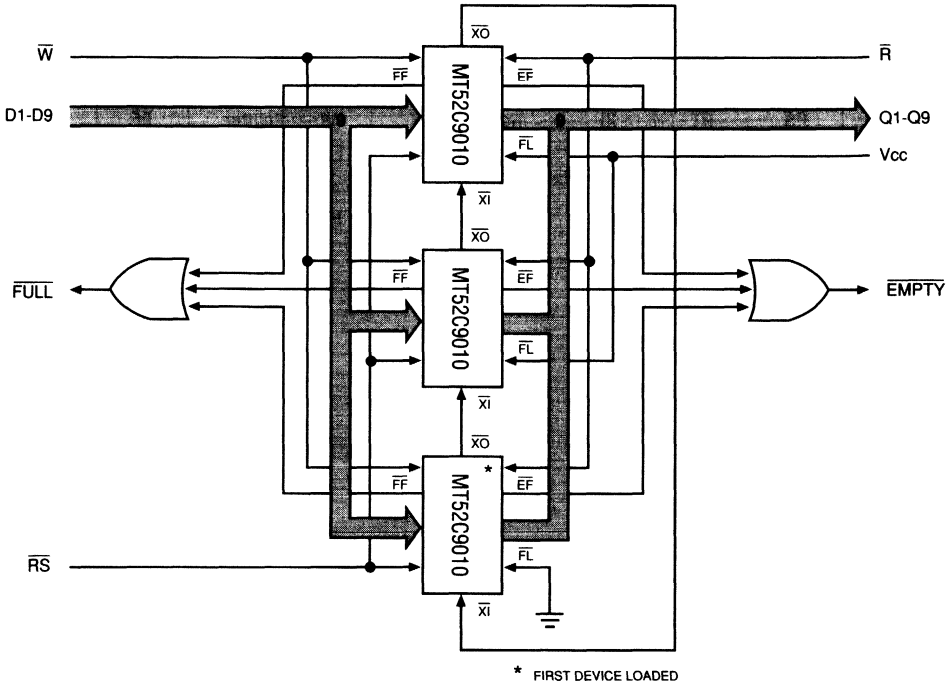


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9010s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9010. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

FIFO

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}/\overline{RT}$/DIR= First Load/Retransmit; $\overline{EF}$ = Empty Flag Output; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	140	130	120	110	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

FIFO

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^tA		15		20		25		35	ns	
READ cycle time	^tRC	25		30		35		45		ns	
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	6
READ LOW to Low-Z	^tRLZ	3		3		3		3		ns	
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RESET cycle time	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
READ HIGH to RESET HIGH	^tRRS	15		20		25		35		ns	
WRITE HIGH to RESET HIGH	^tWRS	15		20		25		35		ns	
RETRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RETRANSMIT pulse width	^tRT	15		20		25		35		ns	
RETRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RETRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET to $\overline{AEF}$, $\overline{EF}$ LOW	^tEFL		25		30		35		45	ns	
RESET to $\overline{AFF}$, $\overline{HF}$, $\overline{FF}$ HIGH	^tHFH, ^tFFH		25		30		35		45	ns	
READ LOW to $\overline{EF}$ LOW	^tREF		20		20		25		30	ns	
READ HIGH to $\overline{FF}$ HIGH	^tRFF		20		20		25		30	ns	
WRITE LOW to $\overline{FF}$ LOW	^tWFF		20		20		25		30	ns	
WRITE HIGH to $\overline{EF}$ HIGH	^tWEF		20		20		25		30	ns	
WRITE LOW to $\overline{HF}$ LOW	^tWHF		25		30		35		45	ns	
READ HIGH to $\overline{HF}$ HIGH	^tRHF		25		30		35		45	ns	
READ HIGH after $\overline{EF}$ HIGH	^tRPE	15		20		25		35		ns	5
WRITE HIGH width after $\overline{FF}$ HIGH	^tWPF	15		20		25		35		ns	5
READ/WRITE to $\overline{XO}$ LOW	^tXOL		15		20		25		35	ns	
READ/WRITE to $\overline{XO}$ HIGH	^tXOH		15		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time	^tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	^tXIR	10		10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

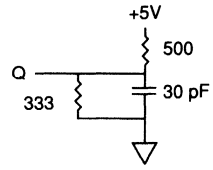
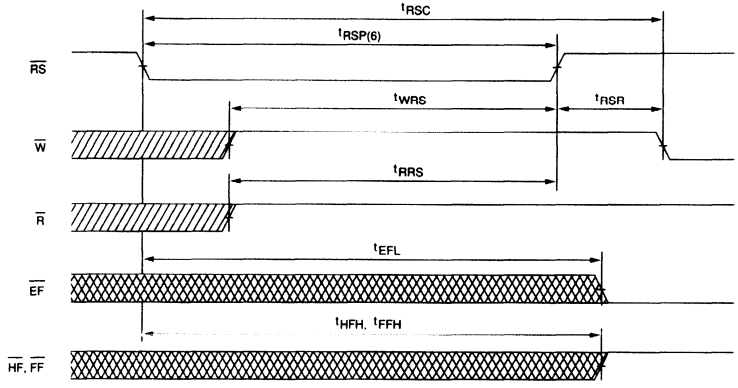
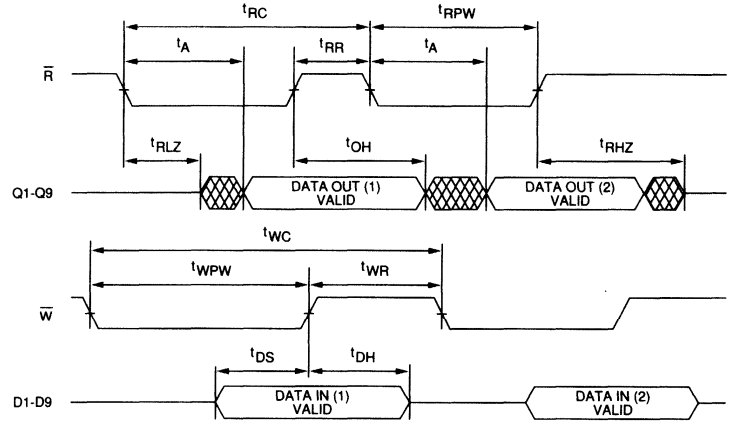


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET



ASYNCHRONOUS READ AND WRITE

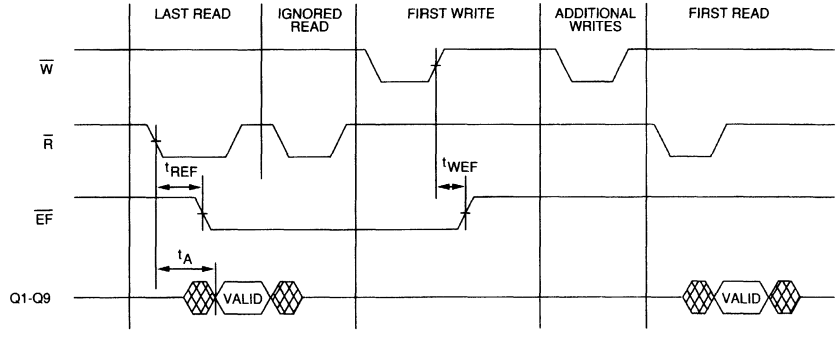


DON'T CARE

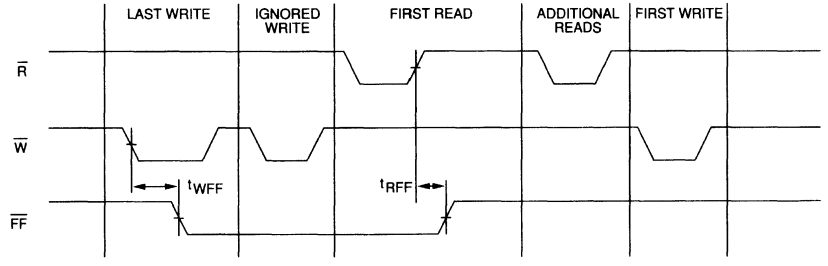
UNDEFINED

FIFO

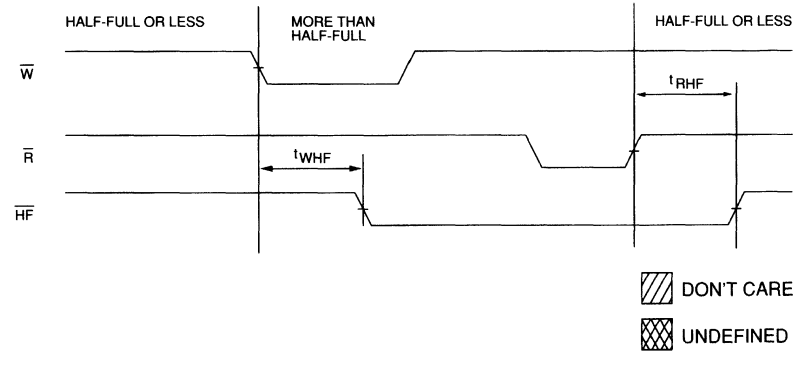
EMPTY FLAG



FULL FLAG

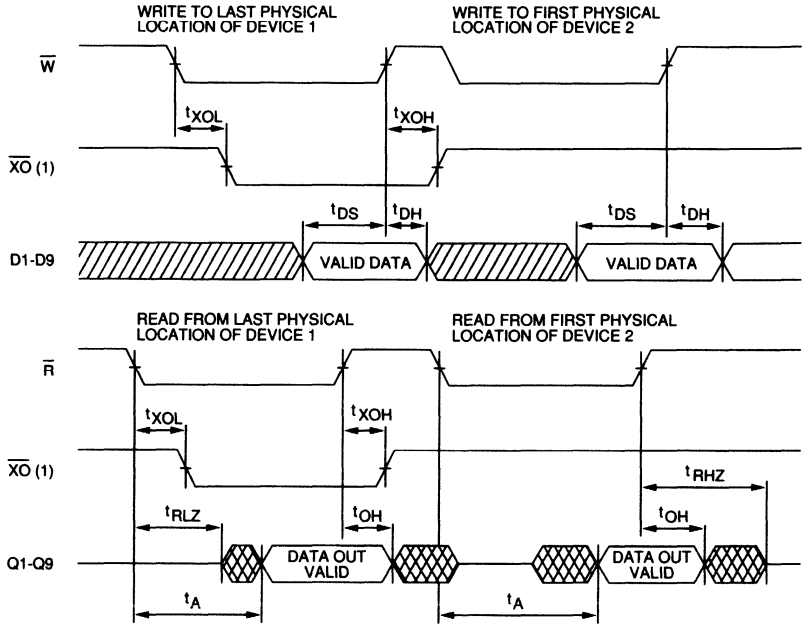


HALF-FULL FLAG



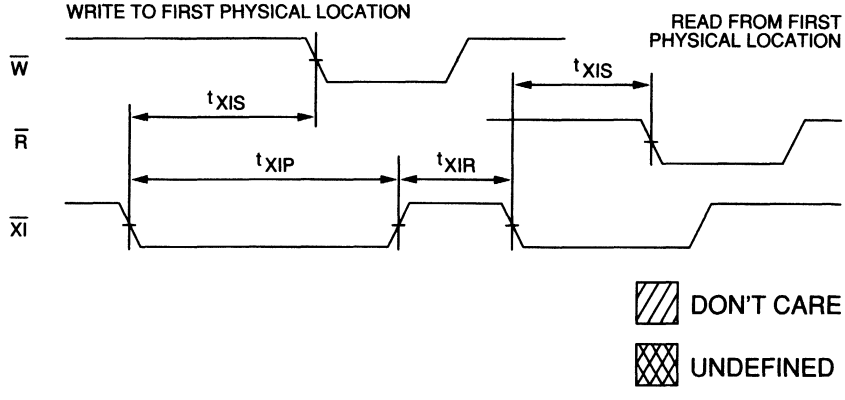
FIFO

EXPANSION MODE ($\overline{XO}$)



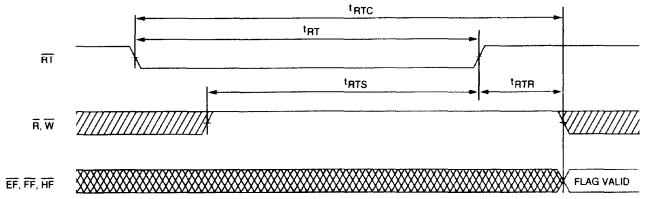
NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

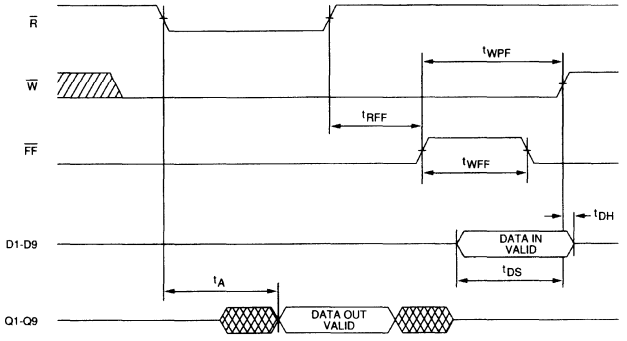


FIFO

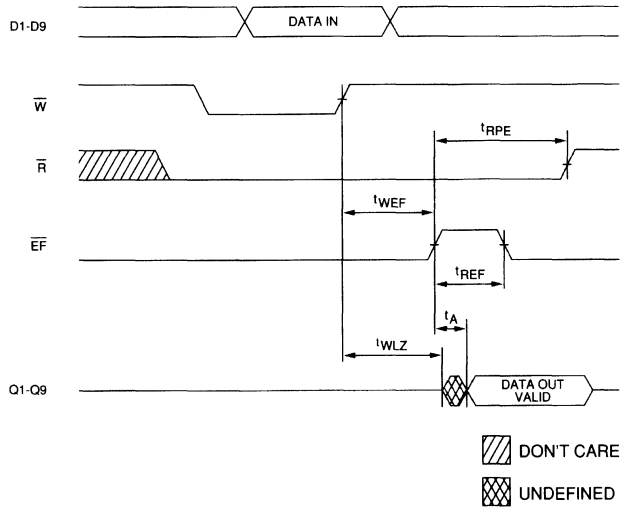
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



FIFO

FIFO

1K x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost-Full and Almost-Empty Flags
- Programmable Half-Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in SINGLE DEVICE mode
- Fully expandable by width and depth
- Pin- and function-compatible with standard higher- and lower-density FIFOs

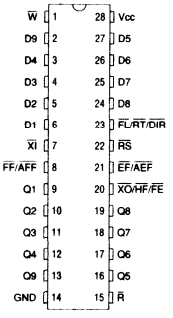
OPTIONS — MARKING

- Timing
  - 15ns access time — -15
  - 20ns access time — -20
  - 25ns access time — -25
  - 35ns access time — -35
- Packages
  - Plastic DIP (300 mil) — None
  - PLCC — EJ

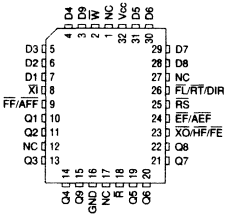
  NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
- Part Number Example: MT52C9012EJ-20

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



32-Pin PLCC
(SC-1)



GENERAL DESCRIPTION

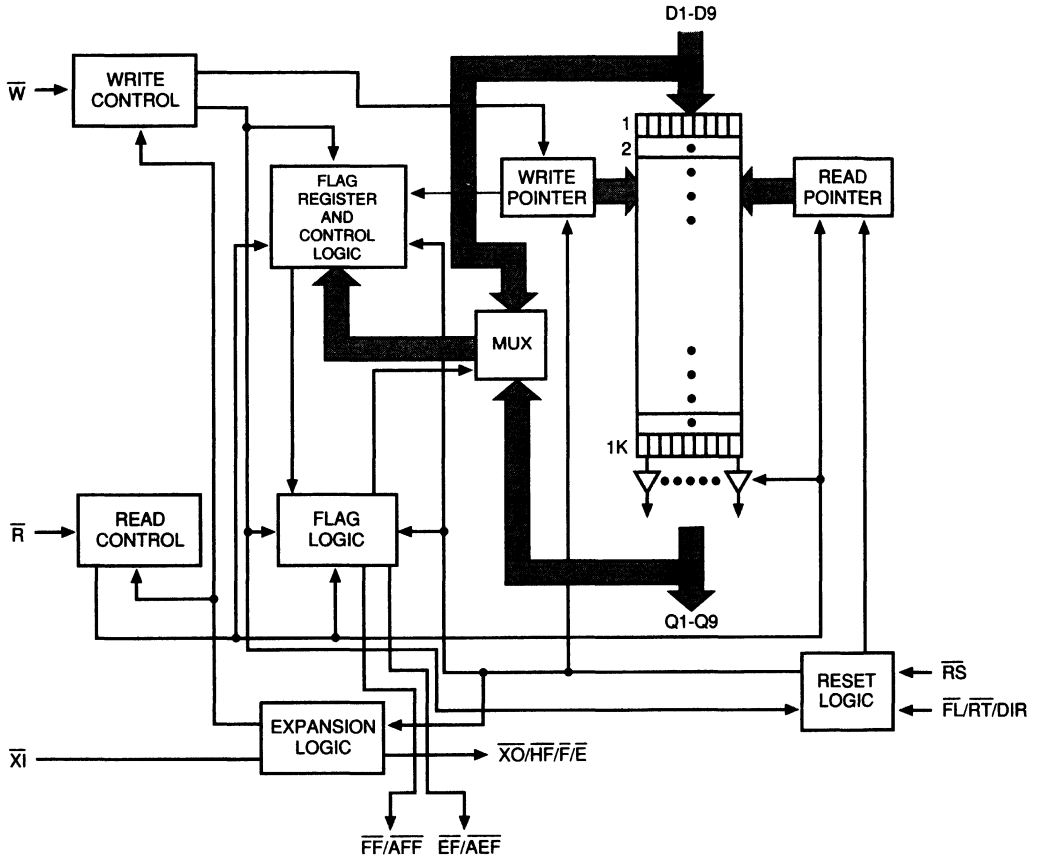
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9012 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9012 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 7-45). In CONFIGURED mode, up to three flags are provided. The first two are the almost-empty flag ($\overline{AEF}$) and the almost-full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FE}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9012 is speed, function and pin compatible with higher and lower density FIFOs from Micron. This upward compatibility with 2K FIFOs provides a single-chip depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are in High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion-In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$) of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in SINGLE DEVICE mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF}/\overline{AEF}$	Output	Empty Flag/Almost-Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost-Empty Flag output. This pin is active LOW.
9	8	$\overline{FF}/\overline{AFF}$	Output	Full Flag/Almost-Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost-Full Flag output. This pin is active LOW.
23	20	$\overline{XO}/\overline{HF}/\overline{FE}$	Output	Expansion Out/Half-Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost-Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO}/\overline{HF}$ in NONCONFIGURED mode.
10, 11, 13, 14, 19, 20, 21, 22,15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input LOW. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FIFO

FUNCTIONAL DESCRIPTION

The MT52C9012 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the XO/HF/FE pin will be shown as (XO)/HF/(FE) when discussing half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}$/($\overline{HF}$) of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and if the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the final empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is asserted, all writes are inhibited, and previously stored data is unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}$/($\overline{HF}$) to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read from a FIFO will cause $\overline{XO}$/($\overline{HF}$) to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9012 allows the receiving device to request that data read earlier from the FIFO be repeated, when less than 1,024 writes have been performed between resets. When the ($\overline{FL}$)/$\overline{RT}$/(DIR) pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^tRTR after ($\overline{FL}$)/$\overline{RT}$/(DIR) is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

FIFO

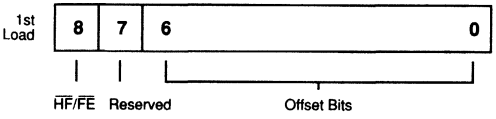
REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost-empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

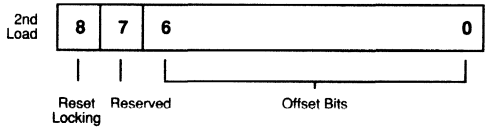
Two 9-bit internal registers have been provided for flag configuration. One is the almost-full flag register (AFFR) and the other is the almost-empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9012

Almost Full Flag Register (AFFR)



Almost Empty Flag Register (AEFR)



Note that bits 0-6 are used for setting the offset value. The offset value ranges from 1 to 127 increments. Each increment value corresponds to 2 words. This provides a maximum offset of 254 words.

Bit 7 is reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{FE}$ pin. When this bit is set LOW, the HF/$\overline{FE}$ pin is configured as an $\overline{HF}$ flag output. When it is set HIGH, the HF/$\overline{FE}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^{t}RS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL APPLICATIONS

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9012s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).

FIFO

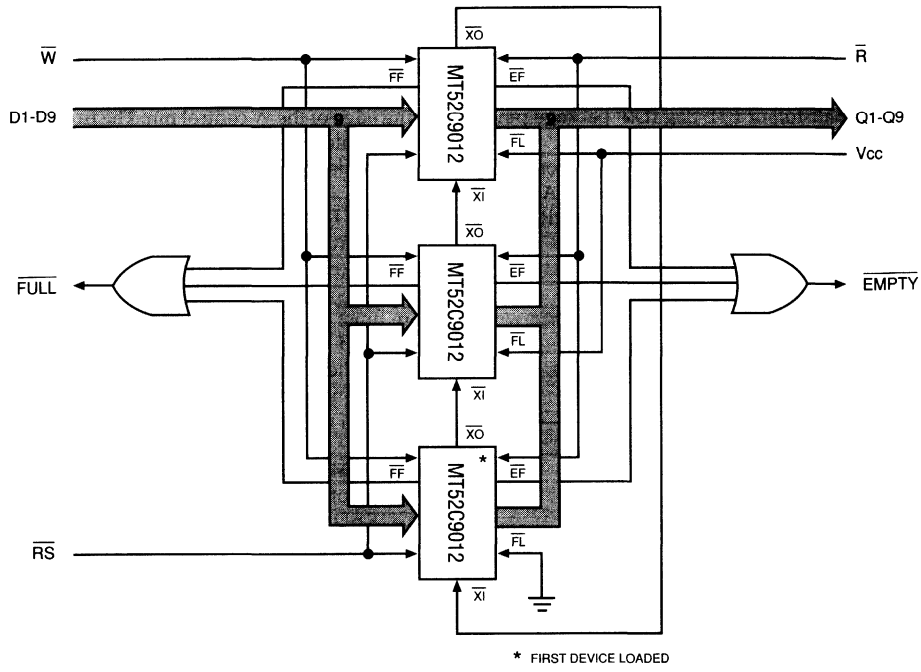


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9012s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9012. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

FIFO

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}/\overline{RT}$/DIR = First Load/Retransmit; $\overline{EF}$ = Empty Flag Outpu; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

FIFO

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	140	130	120	110	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^tRF		40		33.3		28.5		22.2	MHz	
READ cycle time	^tRC	25		30		35		45		ns	
Access time	^tA		15		20		25		35	ns	6
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	
READ LOW to Low-Z	^tRLZ	3		3		3		3		ns	7
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5, 7
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RETRANSMIT Cycle											
RESTRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RESTRANSMIT pulse width	^tRT	15		20		25		35		ns	
RESTRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RESTRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^tRS	15		20		25		35		ns	
RESET and register programming cycle time	^tRSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^tRDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^tRW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^tWRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^tRRS	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{R}/\overline{W}$ to $\overline{XO}$ LOW	tXOL		15		20		25		35	ns	
$\overline{R}/\overline{W}$ to $\overline{XO}$ HIGH	tXOH		15		20		25		35	ns	
$\overline{XI}$ pulse width	tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time to $\overline{R}/\overline{W}$	tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	tXIR	10		10		10		10		ns	
Flags Timing											
$\overline{W}$ HIGH to Flags Valid	tWFV		15		15		15		15	ns	
$\overline{RS}$ to $\overline{AEF}$, $\overline{EF}$ LOW	tEFL		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{EF}$ LOW	tREF		20		20		25		30	ns	
$\overline{W}$ HIGH to $\overline{EF}$ HIGH	tWEF		20		20		25		30	ns	
$\overline{R}$ HIGH after $\overline{EF}$ HIGH	tRPE	15		20		25		35		ns	5
$\overline{RS}$ to $\overline{AFF}$, $\overline{HF}$, $\overline{FF}$ HIGH	tHFH, tFFH		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{FF}$ HIGH	tRFF		15		20		25		30	ns	
$\overline{W}$ LOW to $\overline{FF}$ LOW	tWFF		20		20		25		30	ns	
$\overline{W}$ HIGH after $\overline{FF}$ HIGH	tWPF	15		20		25		35		ns	5
$\overline{W}$ LOW to $\overline{HF}$ LOW	tWHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{HF}$ HIGH	tRHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{AFF}$ HIGH	tRAFF		25		30		35		45	ns	
$\overline{W}$ LOW to $\overline{AFF}$ LOW	tWAFF		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{AEF}$ LOW	tRAEF		25		30		35		45	ns	
$\overline{W}$ HIGH to $\overline{AEF}$ HIGH	tWAEF		25		30		35		45	ns	

FIFO

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

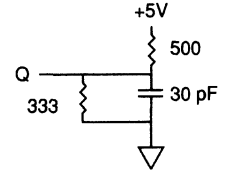
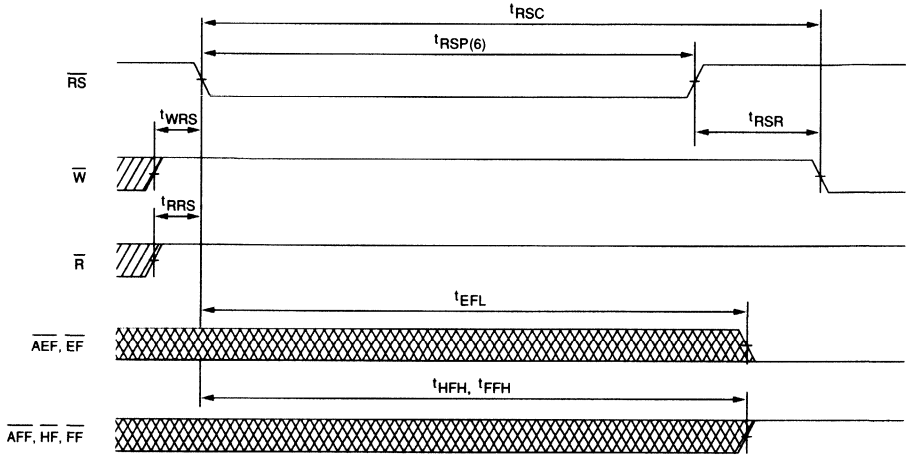


Figure 2
OUTPUT LOAD EQUIVALENT

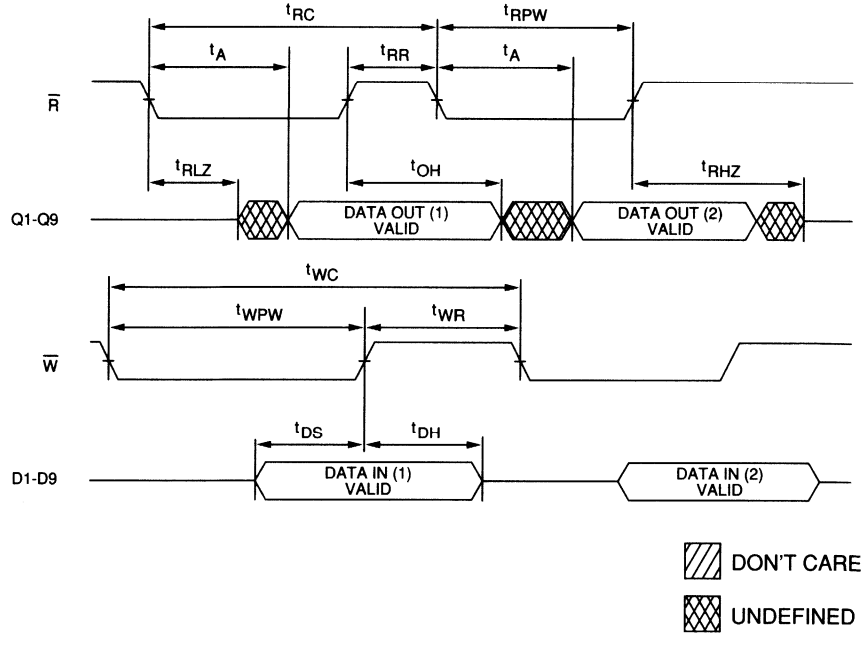
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{R}$ and DIR signals must go inactive (HIGH) coincident with $\overline{RS}$ going inactive (HIGH).
9. DIR must become valid before $\overline{W}$ goes active (LOW).

RESET
(WITH NO REGISTER PROGRAMMING)

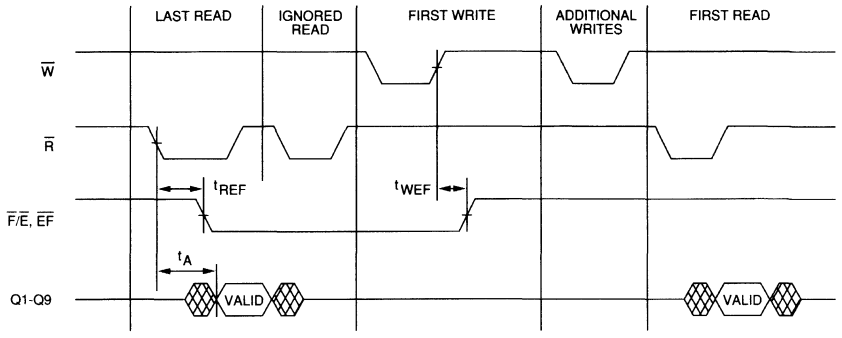


ASYNCHRONOUS READ AND WRITE

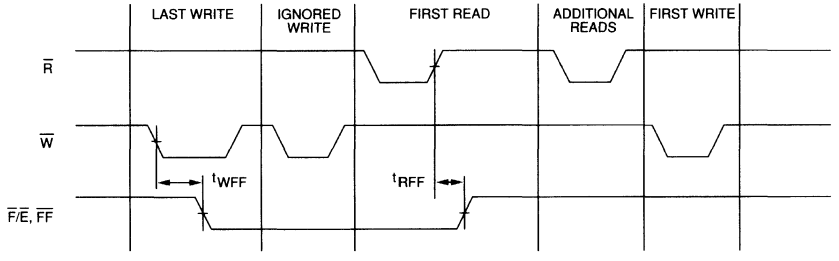


FIFO

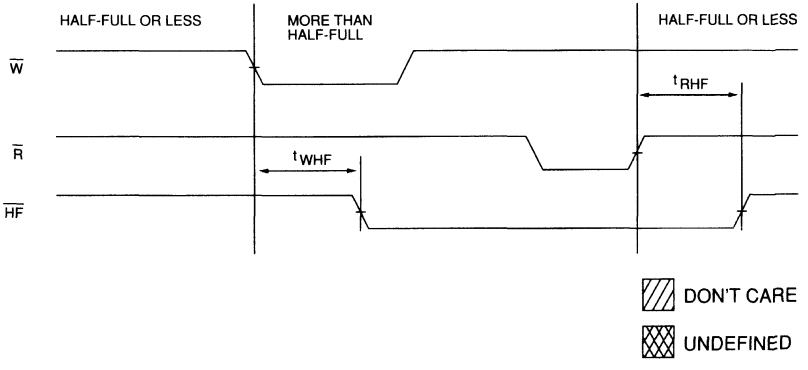
EMPTY FLAG



FULL FLAG

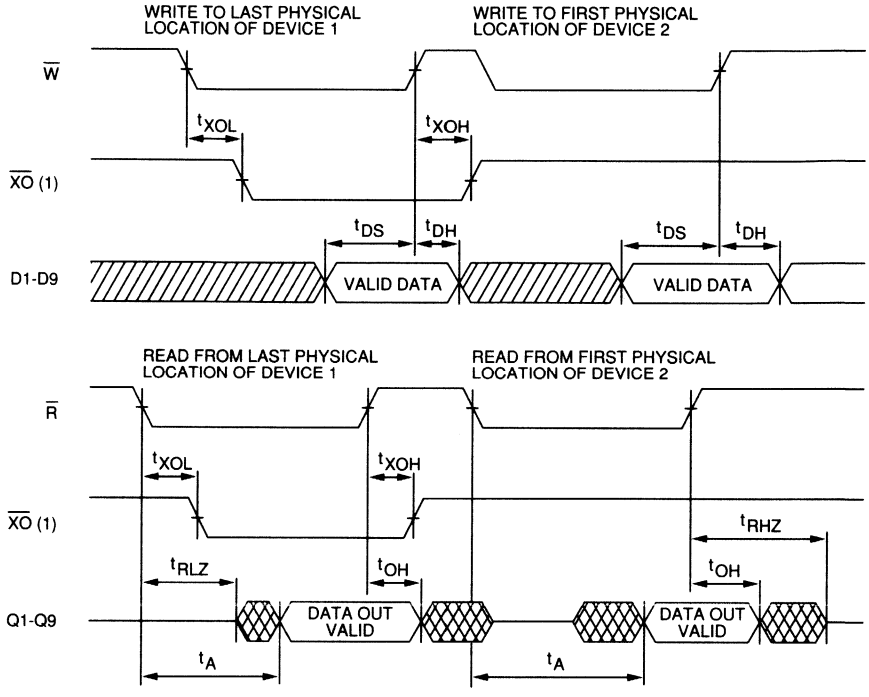


HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



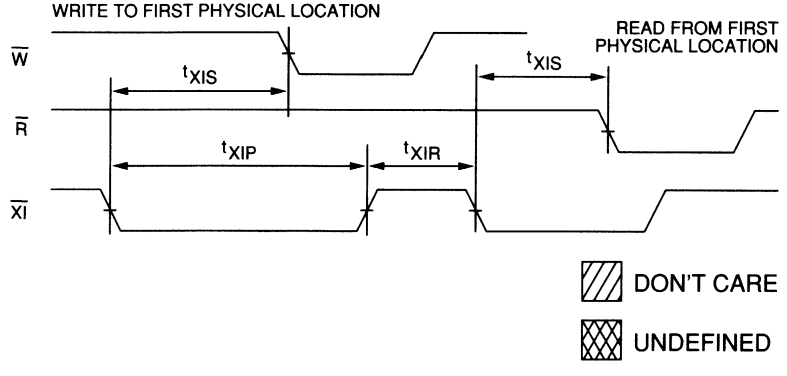
FIFO

EXPANSION MODE ($\overline{XO}$)



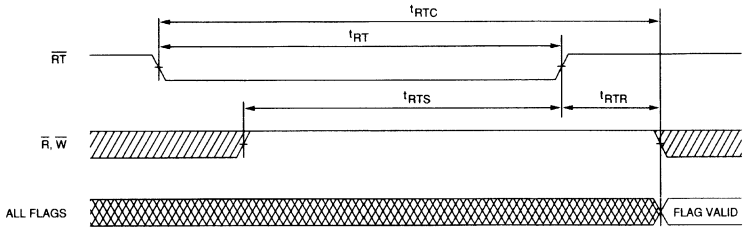
NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

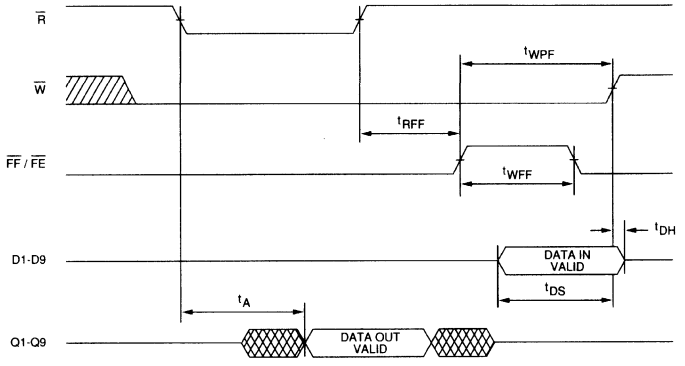


FIFO

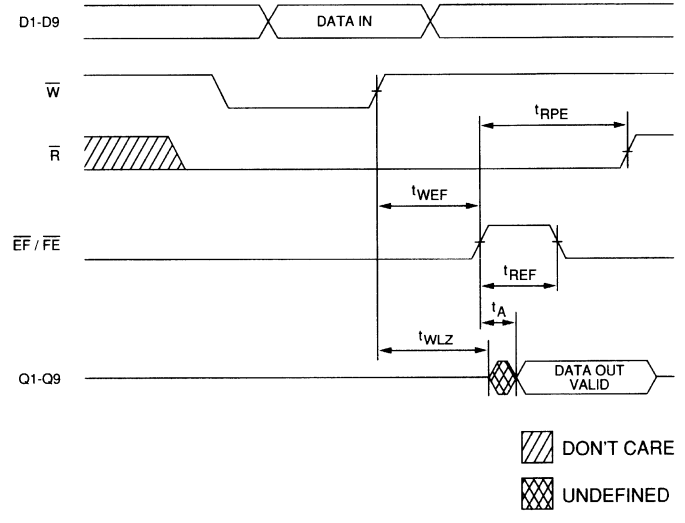
RETRANSMIT



WRITE FLOW-THROUGH

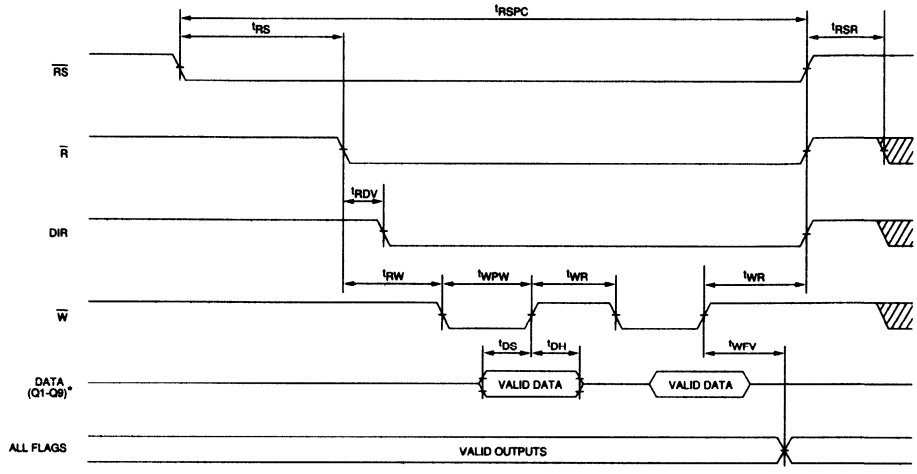


READ FLOW-THROUGH



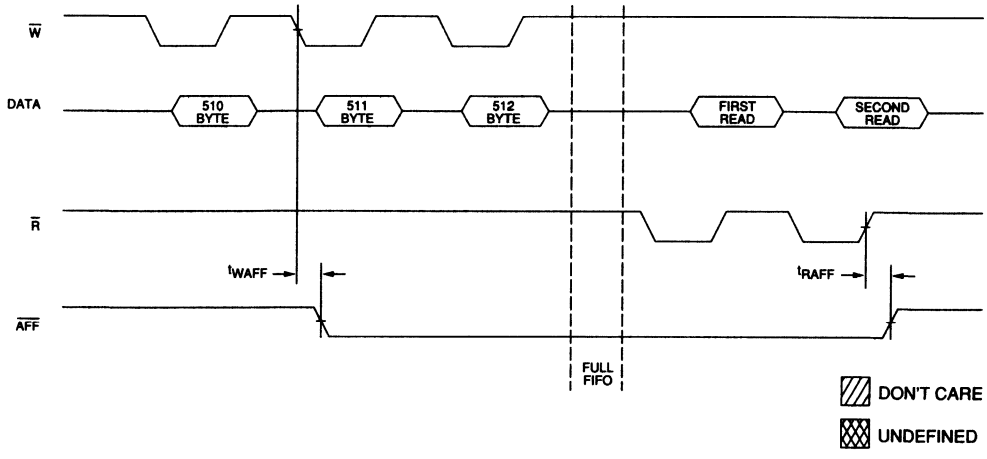
FIFO

RESET/REGISTER PROGRAMMING CYCLE TIME [8, 9]



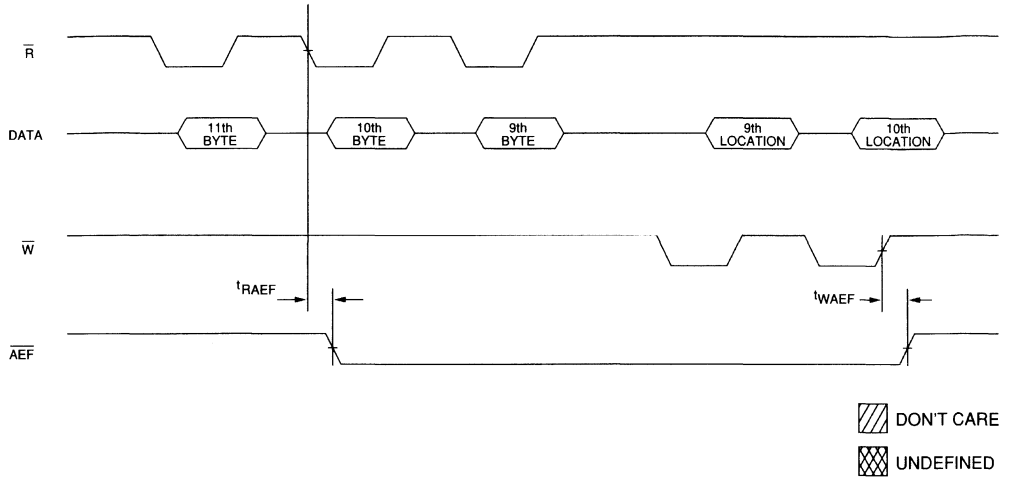
* When DIR = LOW, data is loaded from Q1-Q8; when DIR = HIGH, data is loaded from D1-D9.

ALMOST-FULL FLAG (2-BYTE OFFSET)



FIFO

ALMOST-EMPTY FLAG (10-BYTE OFFSET)



FIFO

2K x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin- and function-compatible with other standard FIFOs

OPTIONS MARKING

- Timing

15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35

- Packages

Plastic DIP (300 mil)	None
PLCC	EJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

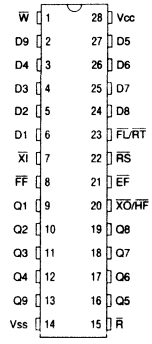
- Temperature

Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT

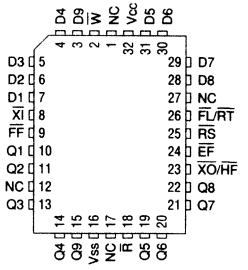
- Part Number Example: MT52C9020EJ-20

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



32-Pin PLCC
(SC-1)



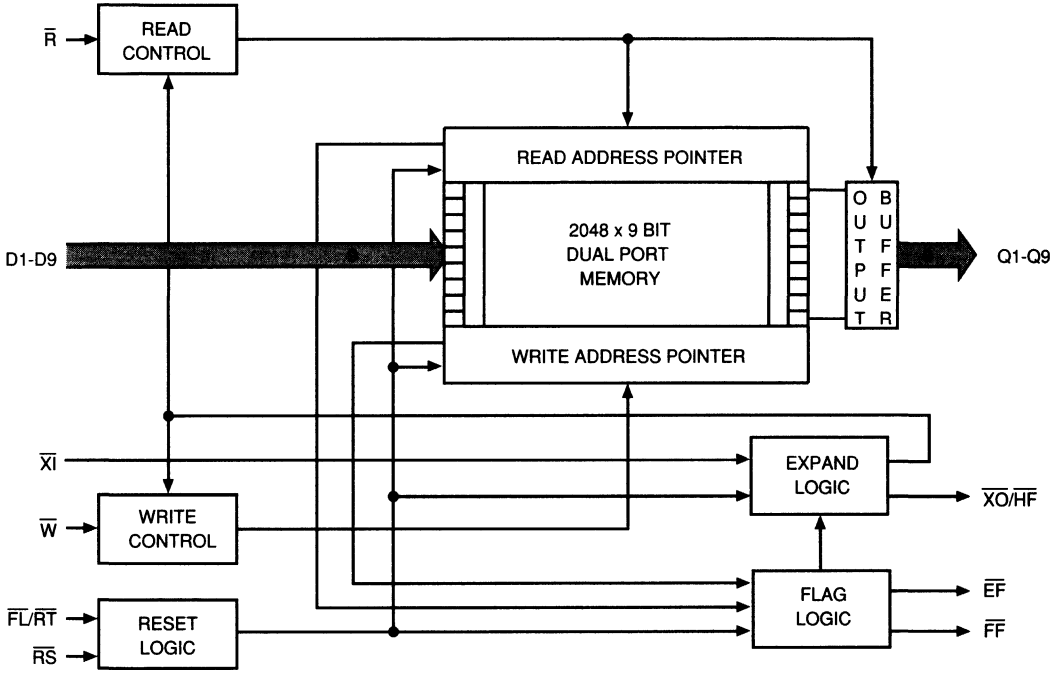
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$, if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied low for the first FIFO in the chain, tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical READ. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than Half-Full; will stay LOW until the FIFO becomes Half-Full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9020 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the XO/HF pin will be shown as (XO)/HF when discussing the half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is tied to $\overline{XO}$/($\overline{HF}$) of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the final empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, (XO)/$\overline{HF}$ is asserted when the half-full-plus-one location (2,048/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}$/$\overline{HF}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{R}$. Valid data will appear ^{t}A after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, (XO)/$\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a READ is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}$/$\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9020 allows the receiving device to request that the data read earlier from the FIFO be repeated, when less than 2,048 writes have been performed between resets. When the ($\overline{FL}$)/$\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^{t}RTR after ($\overline{FL}$)/$\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.

FIFO

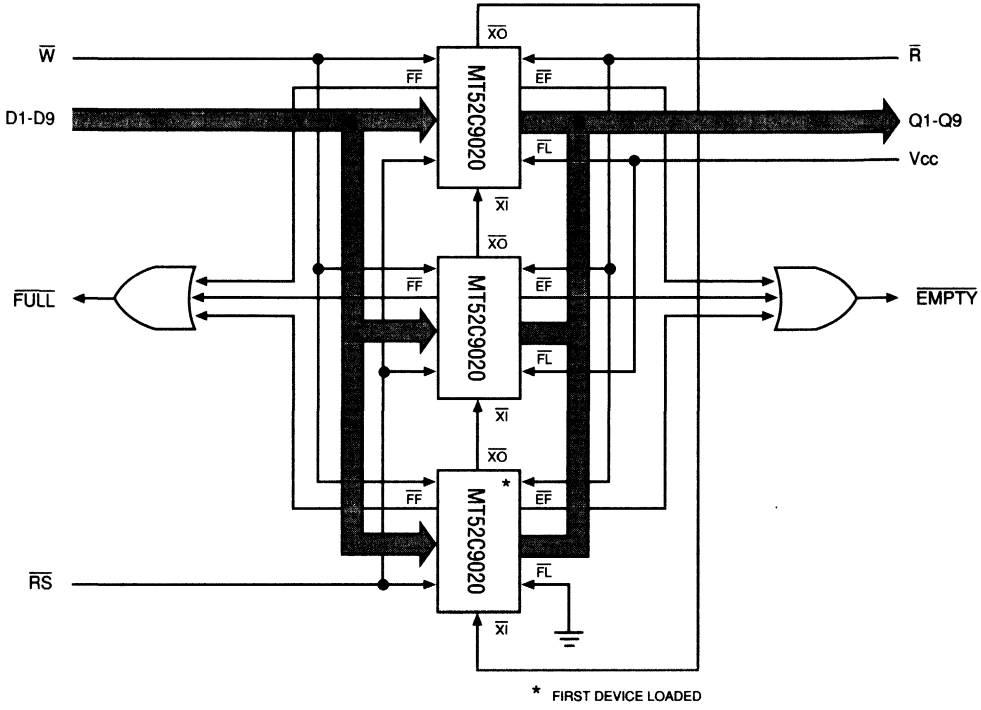


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9020s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9020. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

FIFO

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}$/$\overline{RT}$/DIR= First Load/Retransmit; $\overline{EF}$ = Empty Flag Output; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	140	130	120	110	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

FIFO

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^tA		15		20		25		35	ns	
READ cycle time	^tRC	25		30		35		45		ns	
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	6
READ LOW to Low-Z	^tRLZ	3		3		3		3		ns	
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RESET cycle time	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
READ HIGH to Reset HIGH	^tRRS	15		20		25		35		ns	
WRITE HIGH to Reset HIGH	^tWRS	15		20		25		35		ns	
RETRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RETRANSMIT pulse width	^tRT	15		20		25		35		ns	
RETRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RETRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET to $\overline{AEF}$, $\overline{EF}$ LOW	^tEFL		25		30		35		45	ns	
RESET to $\overline{AFF}$, $\overline{HF}$, $\overline{FF}$ HIGH	^tHFH, ^tFFH		25		30		35		45	ns	
READ LOW to $\overline{EF}$ LOW	^tREF		20		20		25		30	ns	
READ HIGH to $\overline{FF}$ HIGH	^tRFF		20		20		25		30	ns	
WRITE LOW to $\overline{FF}$ LOW	^tWFF		20		20		25		30	ns	
WRITE HIGH to $\overline{EF}$ HIGH	^tWEF		20		20		25		30	ns	
WRITE LOW to $\overline{HF}$ LOW	^tWHF		25		30		35		45	ns	
READ HIGH to $\overline{HF}$ HIGH	^tRHF		25		30		35		45	ns	
READ HIGH after $\overline{EF}$ HIGH	^tRPE	15		20		25		35		ns	5
WRITE HIGH after $\overline{FF}$ HIGH	^tWPF	15		20		25		35		ns	5
READ/WRITE to $\overline{XO}$ LOW	^tXOL		15		20		25		35	ns	
READ/WRITE to $\overline{XO}$ HIGH	^tXOH		15		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time	^tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	^tXIR	10		10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

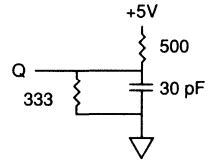
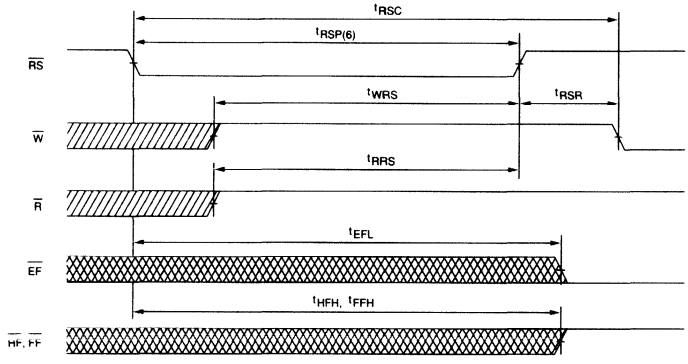
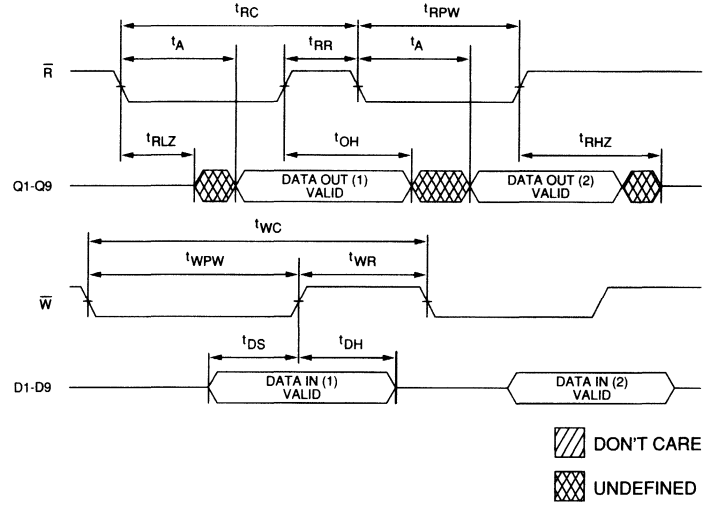


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET

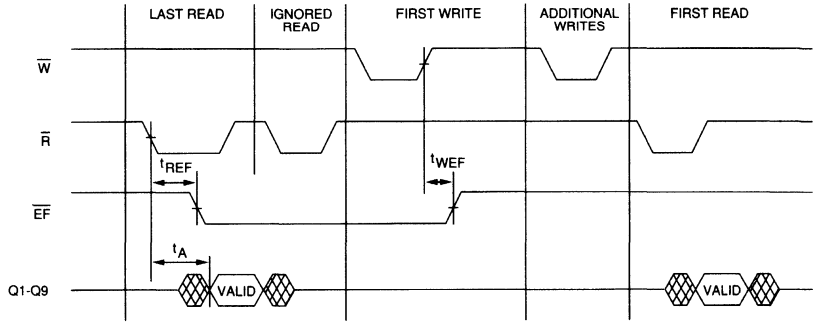


ASYNCHRONOUS READ AND WRITE

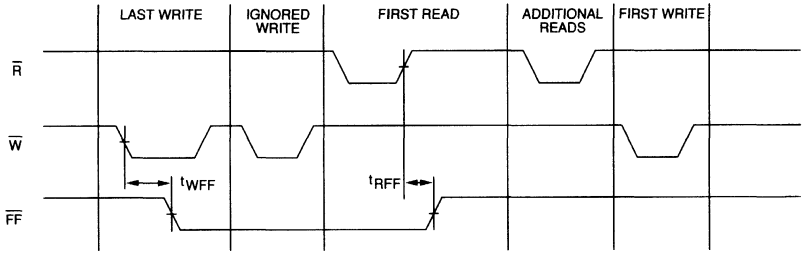


FIFO

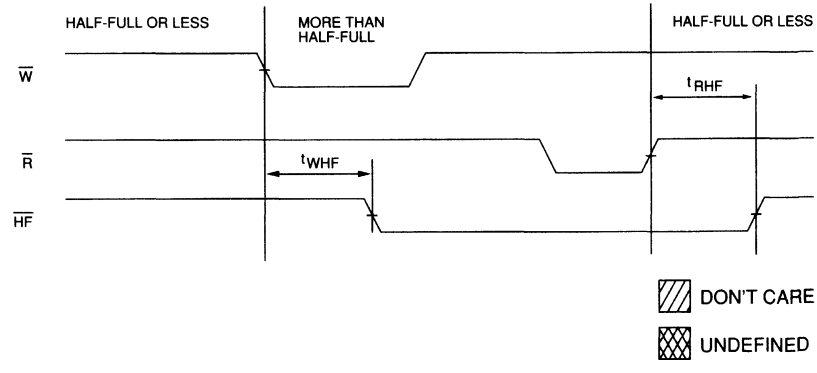
EMPTY FLAG



FULL FLAG

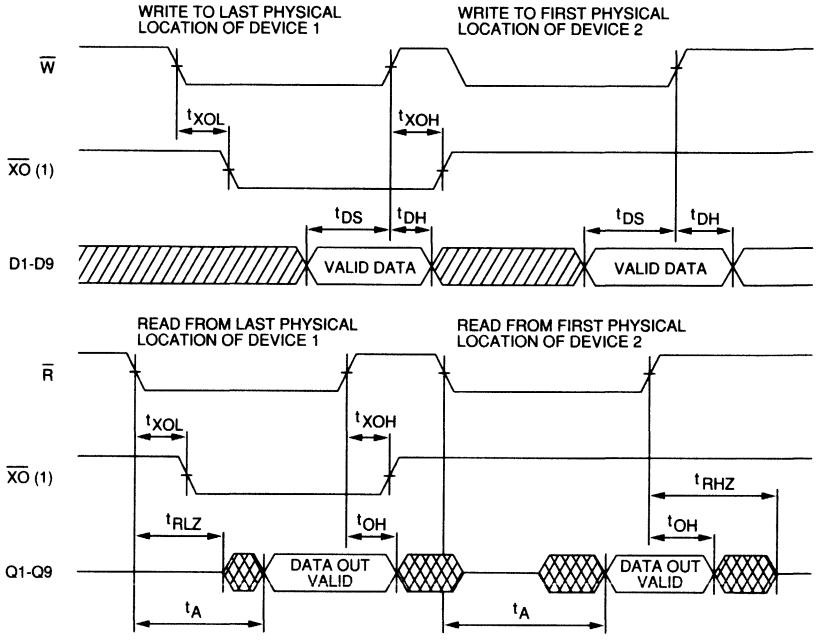


HALF-FULL FLAG



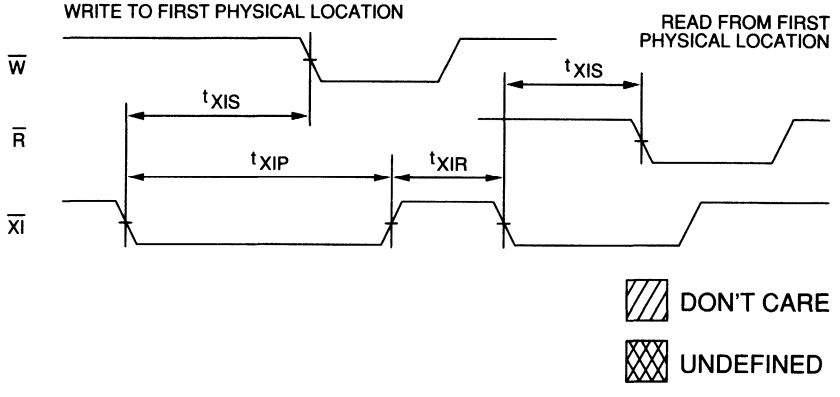
FIFO

EXPANSION MODE ($\overline{XO}$)



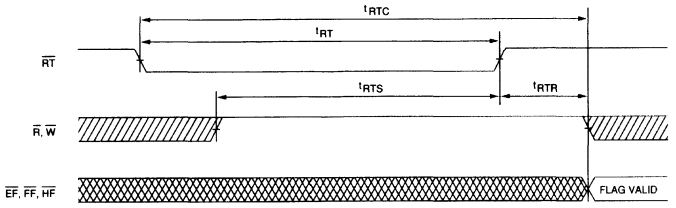
NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

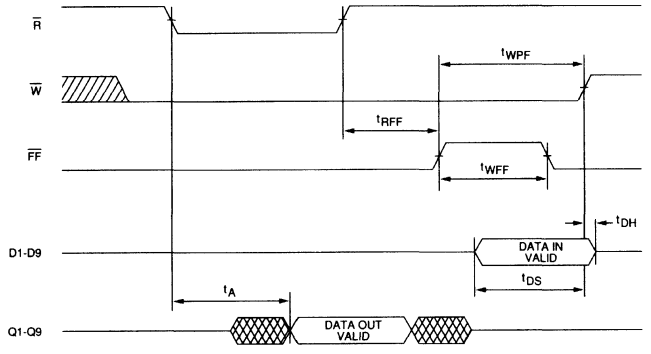


FIFO

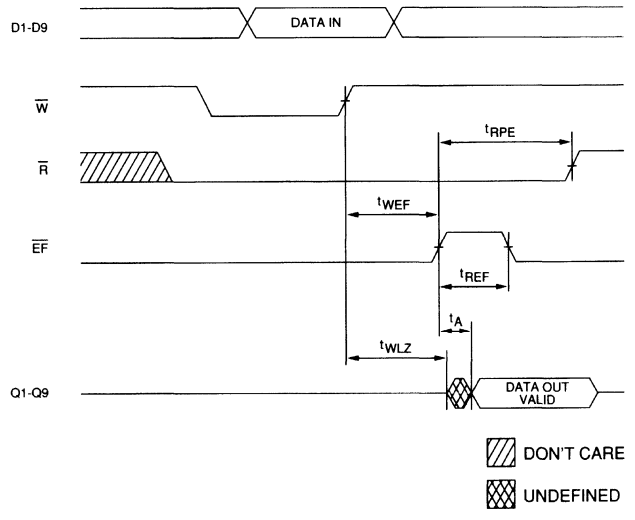
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



FIFO

FIFO

2K x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost-Full and Almost-Empty Flags
- Programmable Half-Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in SINGLE DEVICE mode
- Fully expandable by width and depth
- Pin- and function-compatible with standard FIFOs

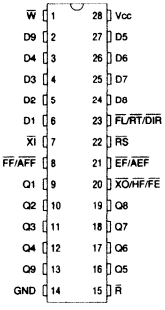
OPTIONS — MARKING

- Timing
  - 15ns access time — -15
  - 20ns access time — -20
  - 25ns access time — -25
  - 35ns access time — -35
- Packages
  - Plastic DIP (300 mil) — None
  - PLCC — EJ

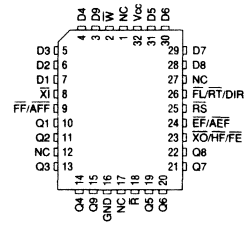
  NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
- Part Number Example: MT52C9022EJ-15

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



32-Pin PLCC
(SC-1)



GENERAL DESCRIPTION

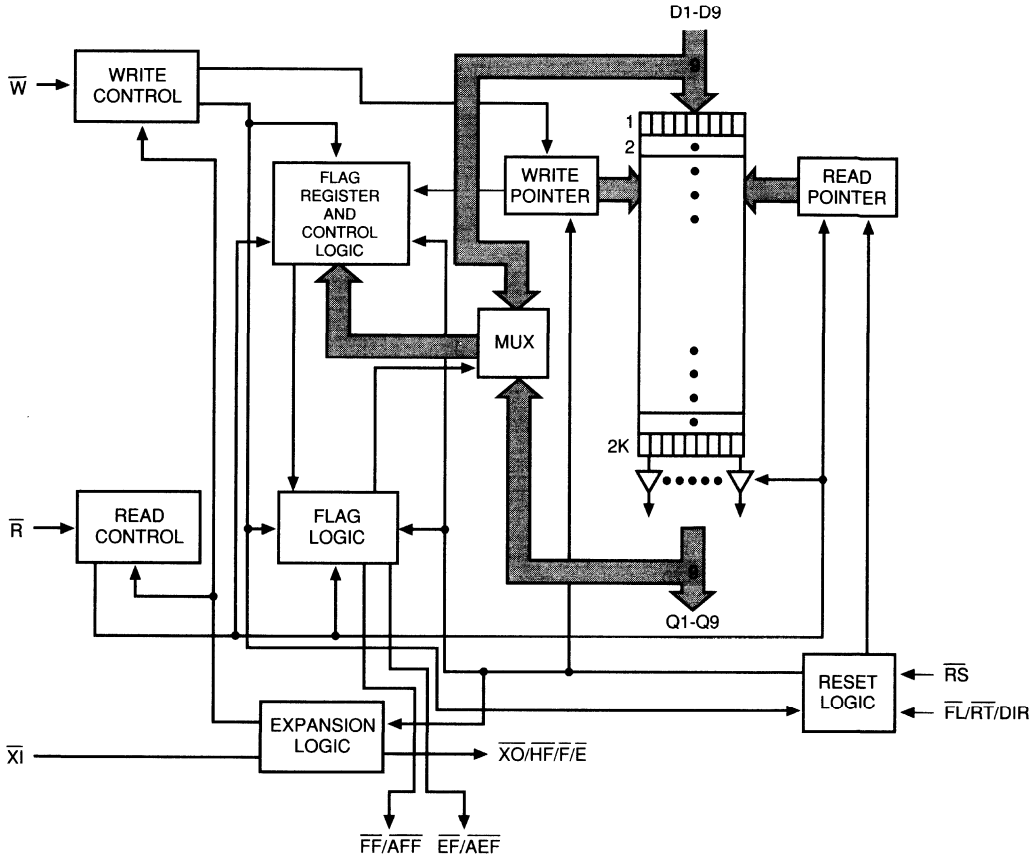
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9022 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9022 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 7-73). In configured mode, up to three flags are provided. The first two are the almost-empty flag ($\overline{AEF}$) and the almost-full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FE}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. The MT52C9022 is speed, function and pin compatible with lower density FIFOs from Micron.

FUNCTIONAL BLOCK DIAGRAM



FIFO

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are in High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion-In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$) of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in SINGLE DEVICE mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF}/\overline{AEF}$	Output	Empty Flag/Almost-Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost-Empty Flag output. This pin is active LOW.
9	8	$\overline{FF}/\overline{AFF}$	Output	Full Flag/Almost-Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost-Full Flag output. This pin is active LOW.
23	20	$\overline{XO}/\overline{HF}/\overline{FE}$	Output	Expansion Out/Half Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost-Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO}/\overline{HF}$ in NONCONFIGURED mode.
10, 11, 13, 14, 19, 20, 21, 22,15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input LOW. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9022 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the XO/HF/FE pin will be shown as (XO)/HF/(FE) when discussing half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}$/($\overline{HF}$) of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and if the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the final empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While the $\overline{FF}$ is asserted, all writes are inhibited and previously stored data is unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}$/($\overline{HF}$) to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last location read from a FIFO will cause $\overline{XO}$/($\overline{HF}$) to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9022 allows the receiving device to request that data read earlier from the FIFO be repeated, when less than 2,048 writes have been performed between resets. When the ($\overline{FL}$)/$\overline{RT}$/(DIR) pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^tRTR after ($\overline{FL}$)/$\overline{RT}$/(DIR) is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

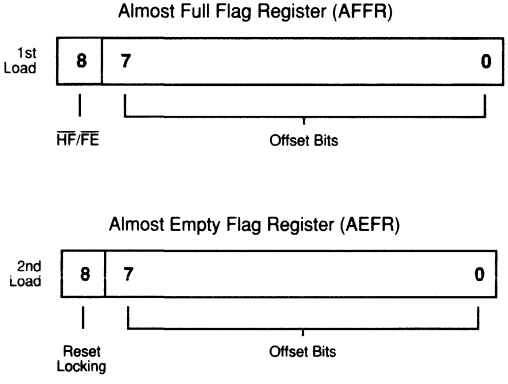
FIFO

REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost-empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

Two 9-bit internal registers have been provided for flag configuration. One is the almost-full flag register (AFFR) and the other is the almost-empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9022



Note that bits 0-7 are used for setting the offset value. The offset value ranges from 1 to 255 increments. Each increment value corresponds to 2 words. This provides a maximum offset of 510 words.

Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{FE}$ pin. When this bit is set LOW, the $HF/\overline{FE}$ pin is configured as an $\overline{HF}$ flag output. When it is set HIGH, the $HF/\overline{FE}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^tRS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL APPLICATIONS

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9022s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$ flag, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO if full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).

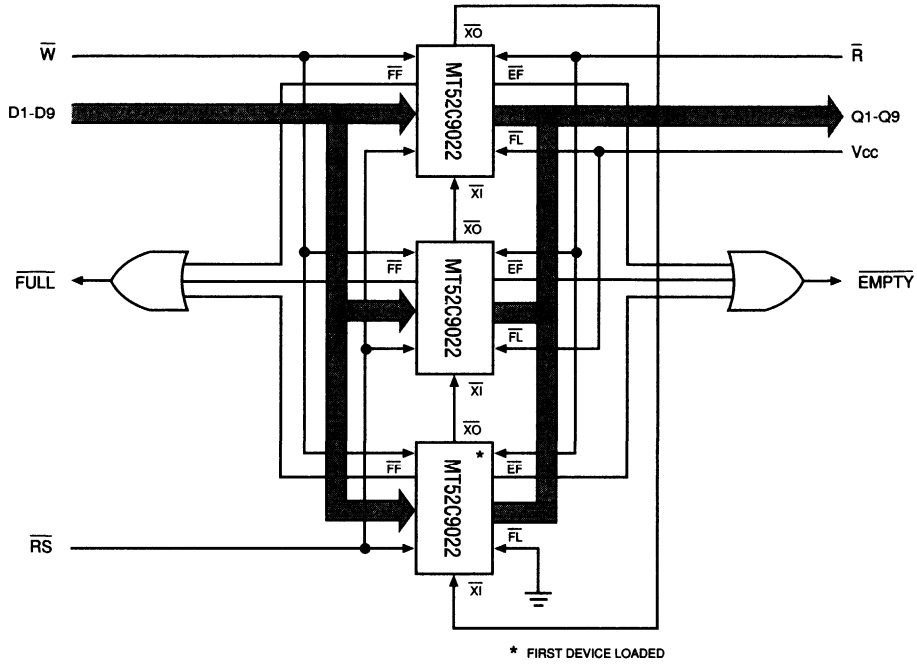


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9022s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9022. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The READ pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}$/$\overline{RT}$/DIR = First Load/Retransmit; $\overline{EF}$ = Empty Flag Output; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MAX -15	MAX -20	MAX -25	MAX -35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	140	130	120	110	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2 or $V_{IN} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^tRF		40		33.3		28.5		22.2	MHz	
READ cycle time	^tRC	25		30		35		45		ns	
Access time	^tA		15		20		25		35	ns	6
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	
READ LOW to Low-Z	^tRLZ	3		3		3		3		ns	7
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5, 7
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RETRANSMIT Cycle											
RESTRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RESTRANSMIT pulse width	^tRT	15		20		25		35		ns	
RESTRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RESTRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^tRS	15		20		25		35		ns	
RESET and register programming cycle time	^tRSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^tRDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^tRW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^tWRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^tRRS	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{R}/\overline{W}$ to $\overline{XO}$ LOW	tXOL		15		20		25		35	ns	
$\overline{R}/\overline{W}$ to $\overline{XO}$ HIGH	tXOH		15		20		25		35	ns	
$\overline{XI}$ pulse width	tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time to $\overline{R}/\overline{W}$	tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	tXIR	10		10		10		10		ns	
Flags Timing											
$\overline{W}$ HIGH to Flags Valid	tWFV		15		15		15		15	ns	
$\overline{RS}$ to $\overline{AEF}$, $\overline{EF}$ LOW	tEFL		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{EF}$ LOW	tREF		20		20		25		30	ns	
$\overline{W}$ HIGH to $\overline{EF}$ HIGH	tWEF		20		20		25		30	ns	
$\overline{R}$ HIGH after $\overline{EF}$ HIGH	tRPE	15		20		25		35		ns	5
$\overline{RS}$ to $\overline{AFF}$, $\overline{HF}$, $\overline{FF}$ HIGH	tHFH, tFFH		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{FF}$ HIGH	tRFF		15		20		25		30	ns	
$\overline{W}$ LOW to $\overline{FF}$ LOW	tWFF		20		20		25		30	ns	
$\overline{W}$ HIGH after $\overline{FF}$ HIGH	tWPF	15		20		25		35		ns	5
$\overline{W}$ LOW to $\overline{HF}$ LOW	tWHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{HF}$ HIGH	tRHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{AFF}$ HIGH	tRAFF		25		30		35		45	ns	
$\overline{W}$ LOW to $\overline{AFF}$ LOW	tWAFF		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{AEF}$ LOW	tRAEF		25		30		35		45	ns	
$\overline{W}$ HIGH to $\overline{AEF}$ HIGH	tWAEF		25		30		35		45	ns	

FIFO

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

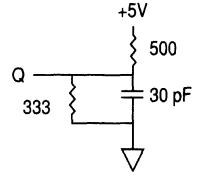
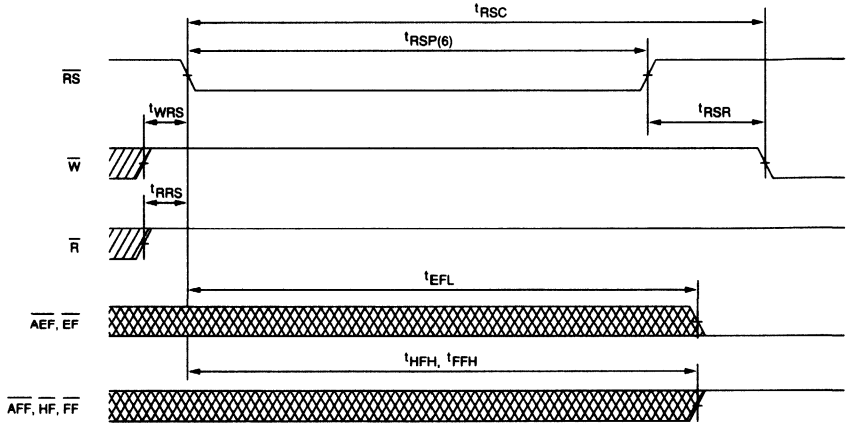


Figure 2
OUTPUT LOAD EQUIVALENT

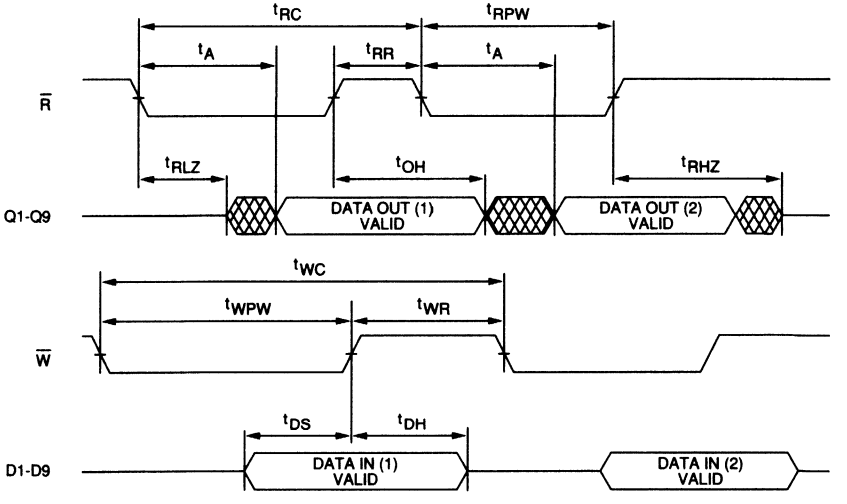
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{R}$ and DIR signals must go inactive (HIGH) coincident with $\overline{RS}$ going inactive (HIGH).
9. DIR must become valid before $\overline{W}$ goes active (LOW).

RESET
(WITH NO REGISTER PROGRAMMING)



ASYNCHRONOUS READ AND WRITE

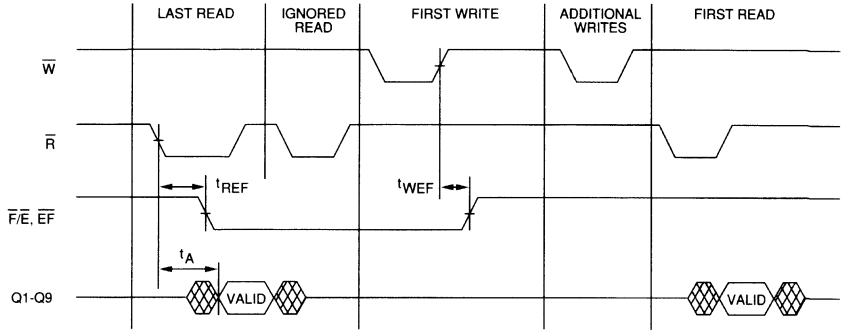


DON'T CARE

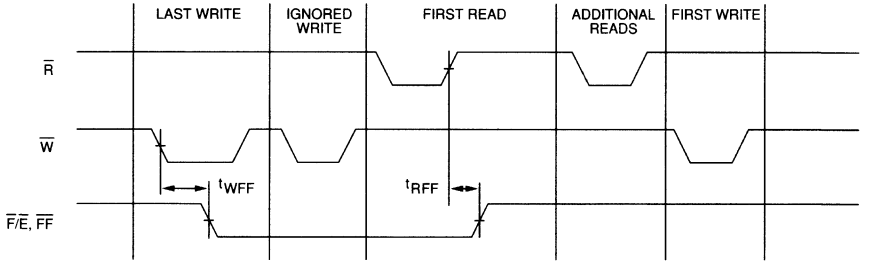
UNDEFINED

FIFO

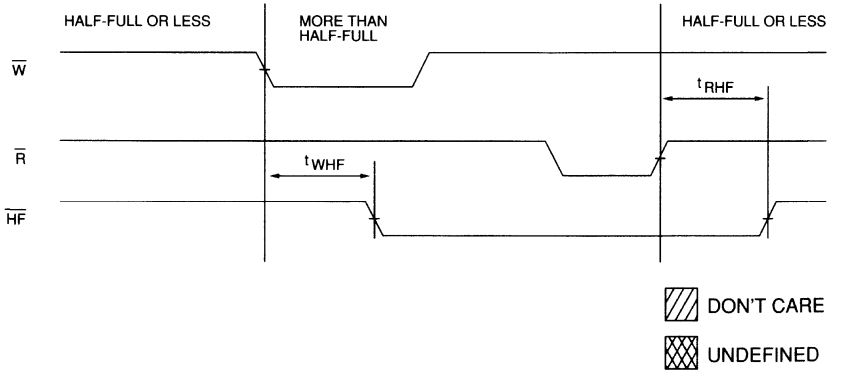
EMPTY FLAG



FULL FLAG

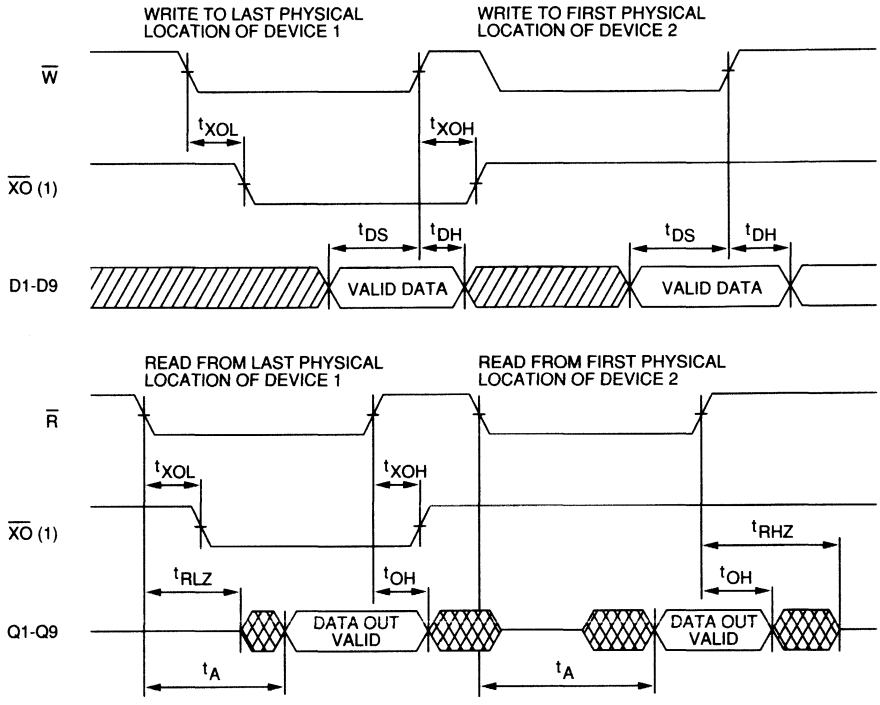


HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



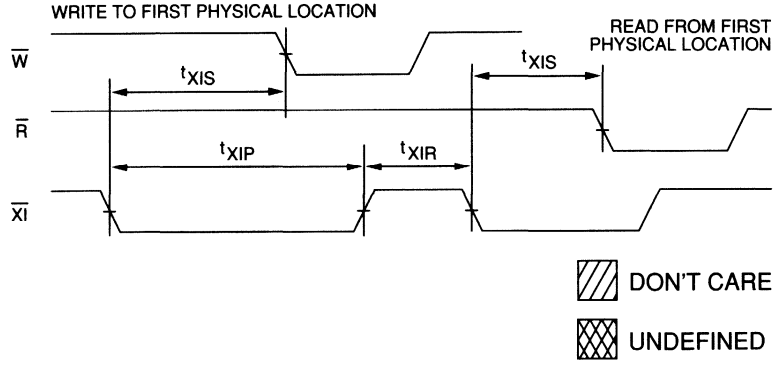
FIFO

EXPANSION MODE ($\overline{XO}$)



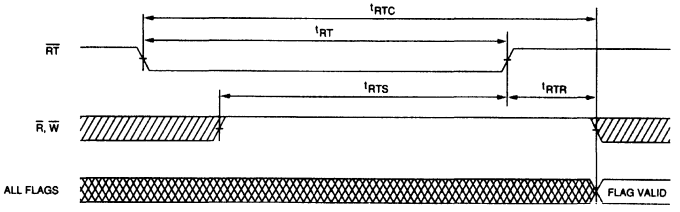
NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

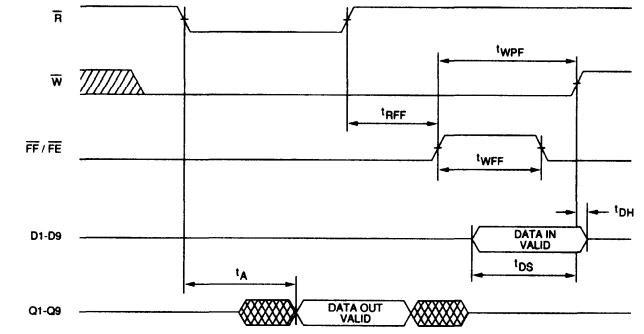


FIFO

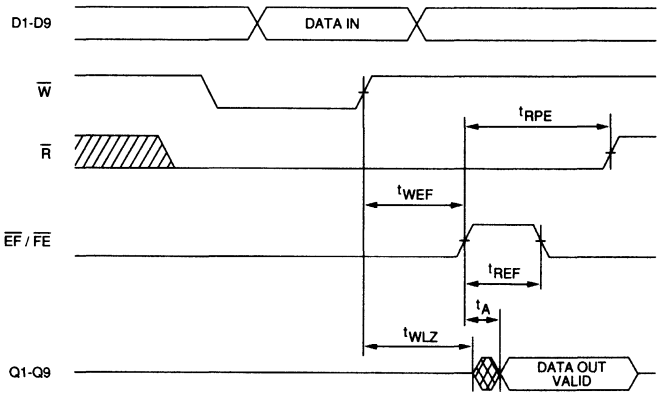
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH

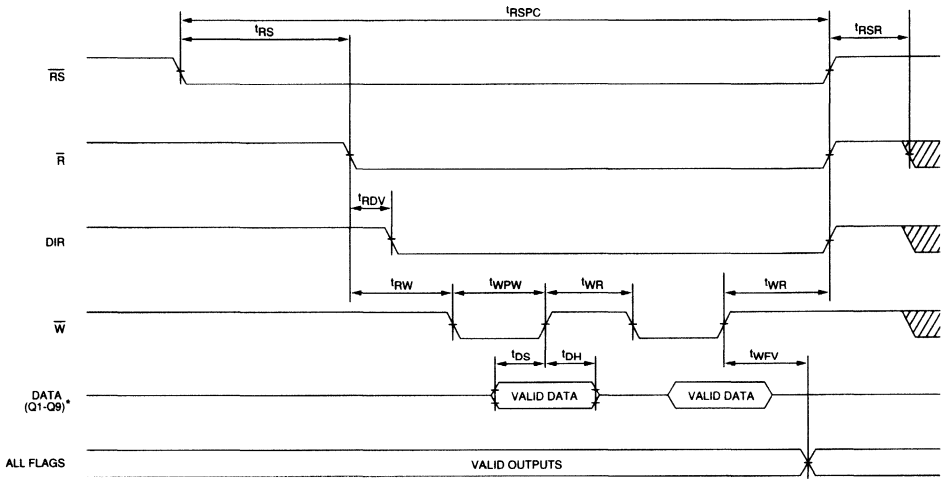


DON'T CARE

UNDEFINED

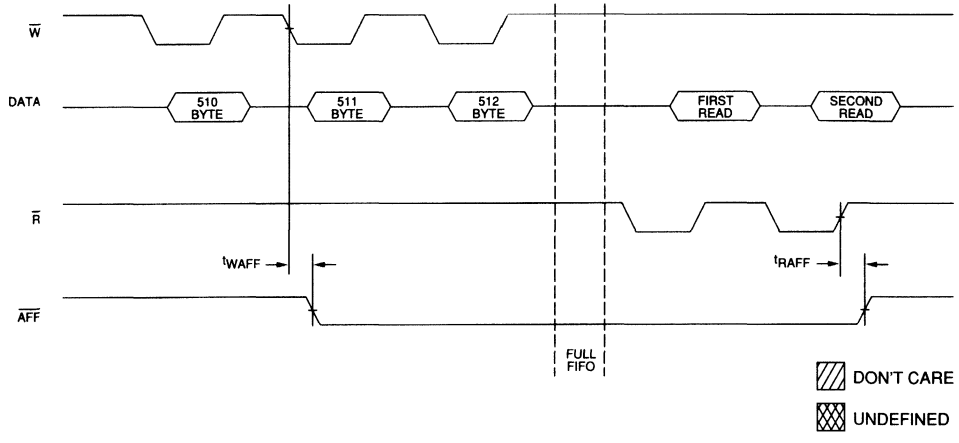
FIFO

RESET/REGISTER PROGRAMMING CYCLE TIME [8, 9]



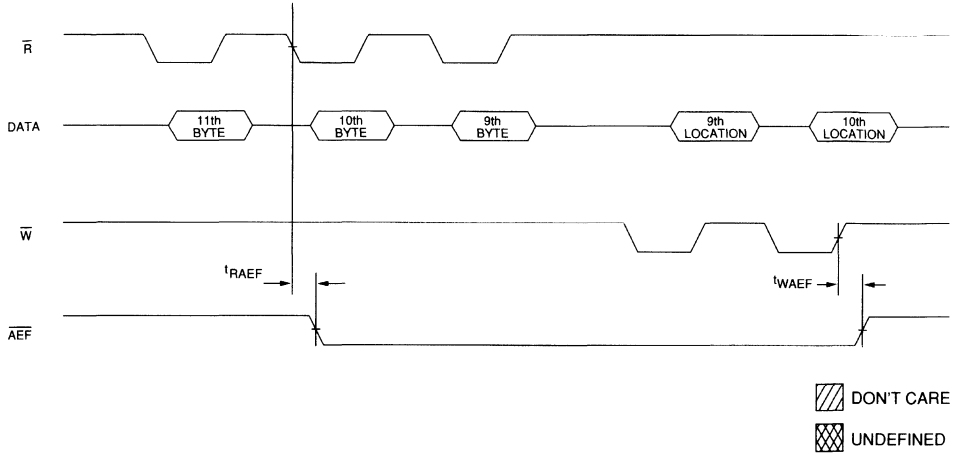
* When DIR = LOW, data is loaded from Q1-Q8; when DIR = HIGH, data is loaded from D1-D9.

ALMOST-FULL FLAG (2-BYTE OFFSET)



FIFO

ALMOST-EMPTY FLAG (10-BYTE OFFSET)



FIFO

FIFO

4K x 9, 8K x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin- and function-compatible with other standard FIFOs

OPTIONS MARKING

- Timing

15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35

- Packages

Plastic DIP (300 mil)	None
PLCC	EJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- Density

4K x 9	MT52C4K9A1
8K x 9	MT52C8K9B2

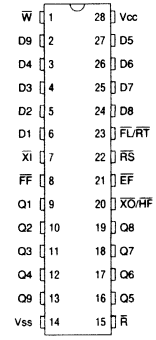
- Temperature

Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT

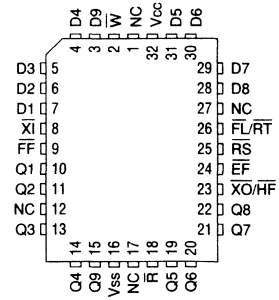
- Part Number Example: MT52C4K9A1EJ-20

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



32-Pin PLCC
(SC-1)



GENERAL DESCRIPTION

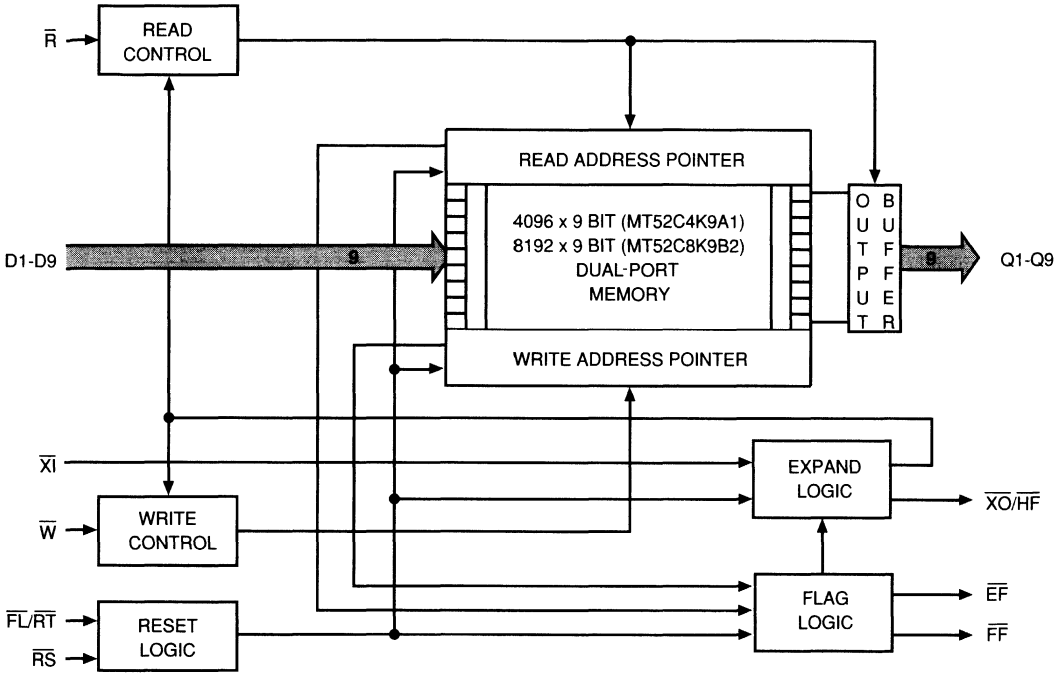
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO may be expanded by cascading multiple devices.

NEW FIFO

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBERS	DIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to $\overline{XO}$ of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$ if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied low for the first FIFO in the chain, tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location; the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical READ. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than Half Full; will stay LOW until the FIFO becomes Half Full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

NEW FIFO

FUNCTIONAL DESCRIPTION

The MT52C4K9A1 and MT52C8K9B2 use dual port SRAM memory cell arrays with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$ when discussing the half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is tied to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the final empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (4,096/2 + 1 in the MT52C4K9A1, 8,192/2 + 1 in the MT52C8K9B2) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

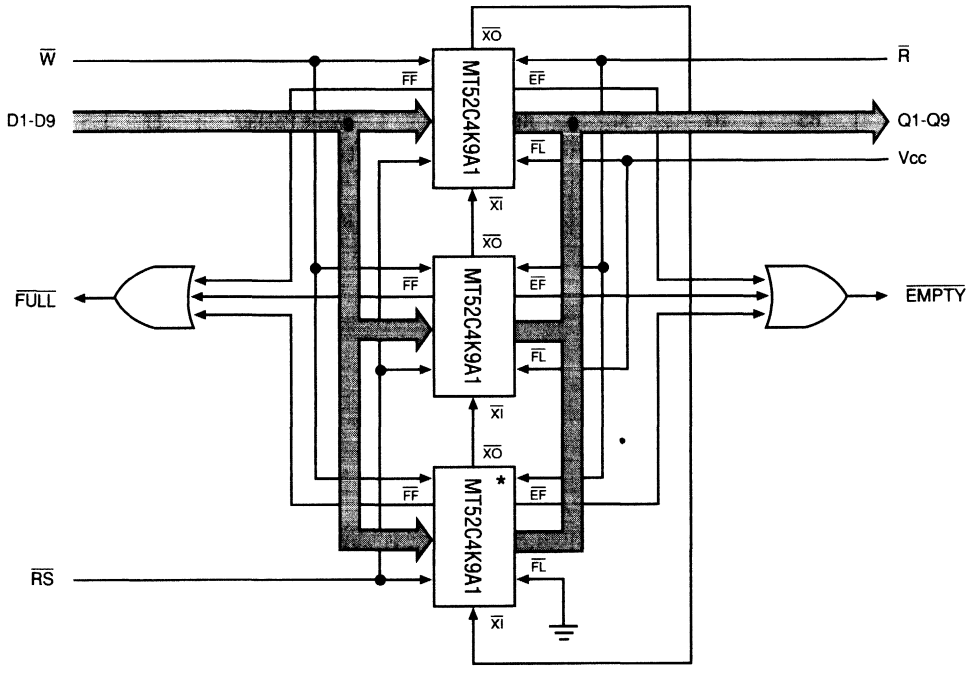
Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a READ is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C4K9A1 allows the receiving device to request that the data read earlier from the FIFO be repeated, when less than 4,096 writes have been performed between resets (less than 8,192 writes in the MT52C8K9B2). When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.



NOTE: MT52C8K9B2 may be used in place of MT52C4K9A1 in this application

* FIRST DEVICE LOADED

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple devices may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth: $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first device. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

NEW FIFO

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

NEW FIFO

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}/\overline{RT}$/DIR = First Load/Retransmit; $\overline{EF}$ = Empty Flag Output; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

NEW FIFO

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MAX -15	MAX -20	MAX -25	MAX -35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	150	140	130	120	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ V_{CC} -0.2; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	tA		15		20		25		35	ns	
READ cycle time	tRC	25		30		35		45		ns	
READ recovery time	tRR	10		10		10		10		ns	
READ pulse width	tRPW	15		20		25		35		ns	6
READ LOW to Low-Z	tRLZ	3		3		3		3		ns	
READ HIGH to High-Z	tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	tOH	5		5		5		5		ns	
WRITE cycle time	tWC	25		30		35		45		ns	
WRITE pulse width	tWPW	15		20		25		35		ns	6
WRITE recovery time	tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	tWLZ	5		5		5		5		ns	5
Data setup time	tDS	10		12		15		18		ns	
Data hold time	tDH	0		0		0		0		ns	
RESET cycle time	tRSC	25		30		35		45		ns	
RESET pulse width	tRSP	15		20		25		35		ns	6
RESET recovery time	tRSR	10		10		10		10		ns	
READ HIGH to Reset HIGH	tRRS	15		20		25		35		ns	
WRITE HIGH to Reset HIGH	tWRS	15		20		25		35		ns	
RETRANSMIT cycle time	tRTC	25		30		35		45		ns	
RETRANSMIT pulse width	tRT	15		20		25		35		ns	
RETRANSMIT recovery time	tRTR	10		10		10		12		ns	
RETRANSMIT setup time	tRTS	15		20		25		35		ns	
RESET to $\overline{AEF}$, $\overline{EF}$ LOW	tEFL		25		30		35		45	ns	
RESET to $\overline{AFF}$, $\overline{HF}$, $\overline{FF}$ HIGH	tHFH, tFFH		25		30		35		45	ns	
READ LOW to $\overline{EF}$ LOW	tREF		20		20		25		30	ns	
READ HIGH to $\overline{FF}$ HIGH	tRFF		20		20		25		30	ns	
WRITE LOW to $\overline{FF}$ LOW	tWFF		20		20		25		30	ns	
WRITE HIGH to $\overline{EF}$ HIGH	tWEF		20		20		25		30	ns	
WRITE LOW to $\overline{HF}$ LOW	tWHF		25		30		35		45	ns	
READ HIGH to $\overline{HF}$ HIGH	tRHF		25		30		35		45	ns	
READ HIGH after $\overline{EF}$ HIGH	tRPE	15		20		25		35		ns	5
WRITE HIGH after $\overline{FF}$ HIGH	tWPF	15		20		25		35		ns	5
READ/WRITE to $\overline{XO}$ LOW	tXOL		15		20		25		35	ns	
READ/WRITE to $\overline{XO}$ HIGH	tXOH		15		20		25		35	ns	
$\overline{XI}$ pulse width	tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time	tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	tXIR	10		10		10		10		ns	

NEW FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

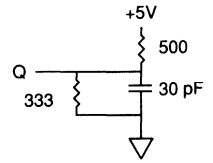
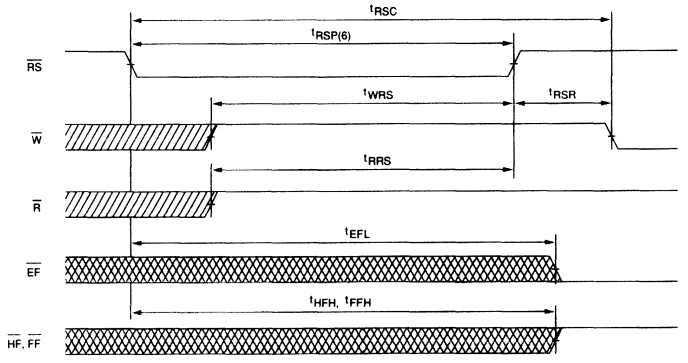
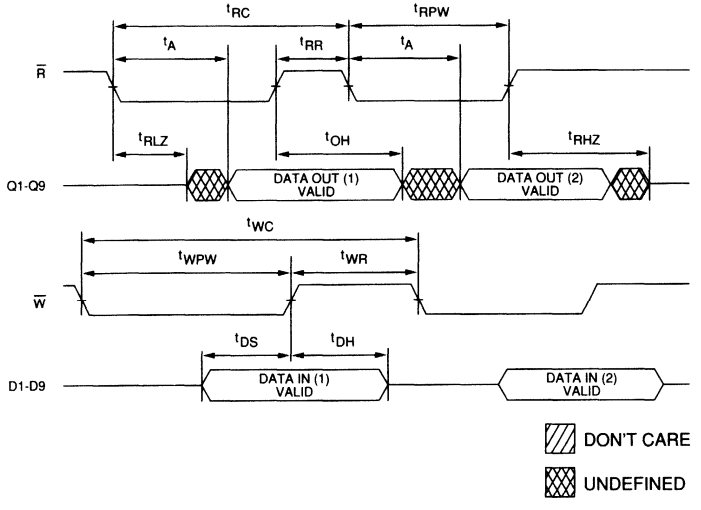


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET



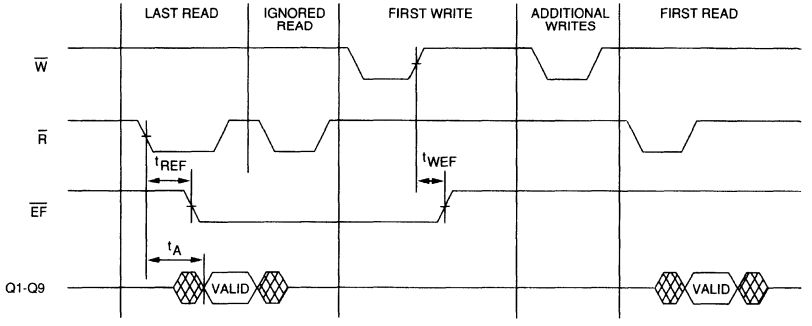
ASYNCHRONOUS READ AND WRITE



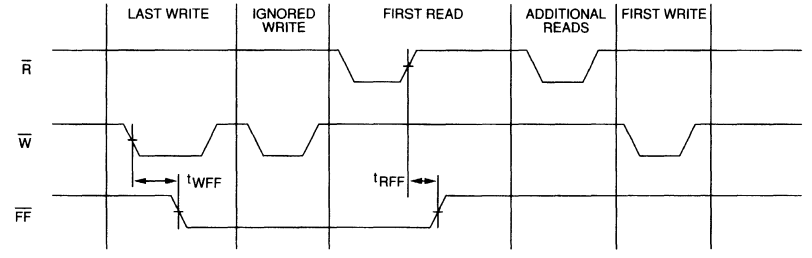
NEW FIFO

NEW FIFO

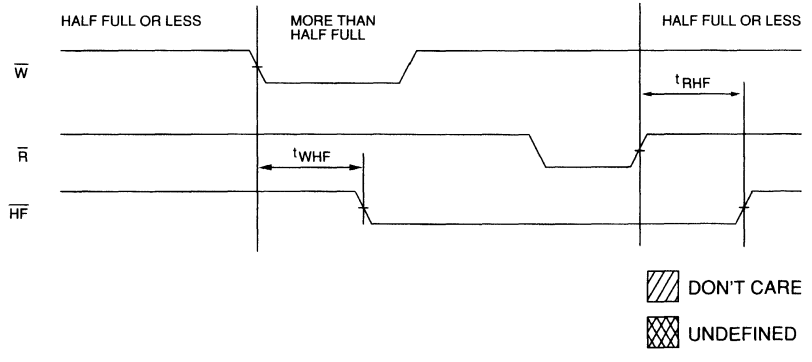
EMPTY FLAG



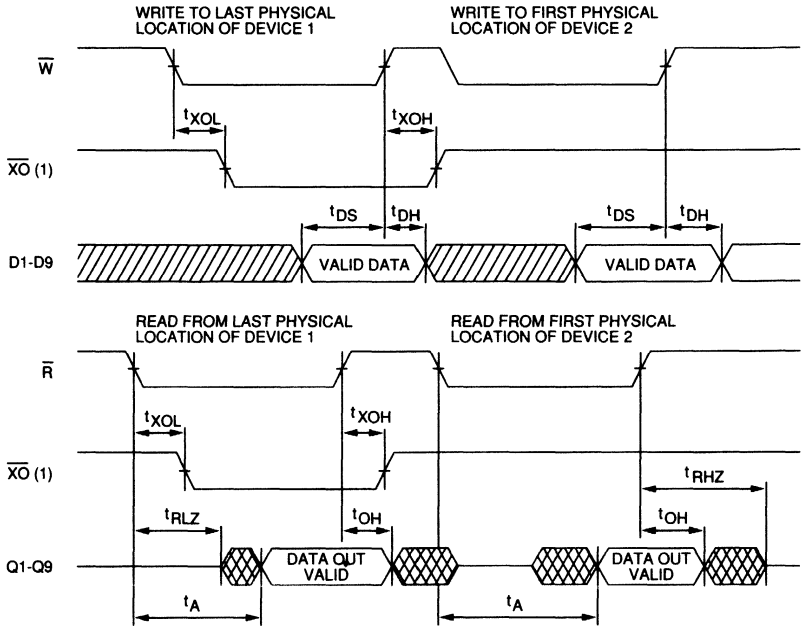
FULL FLAG



HALF-FULL FLAG

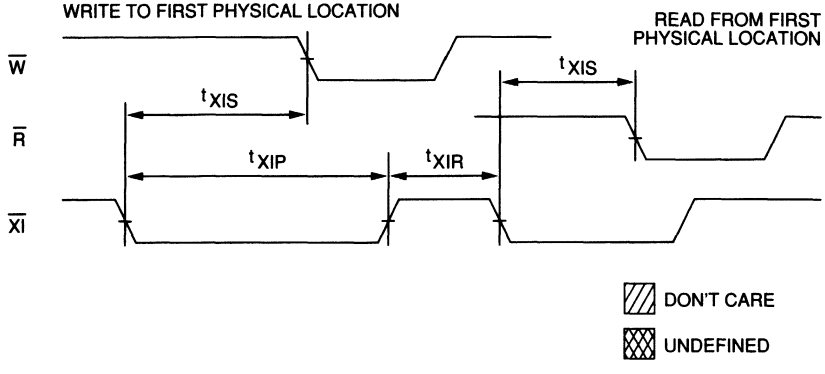


EXPANSION MODE ($\overline{XO}$)



NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

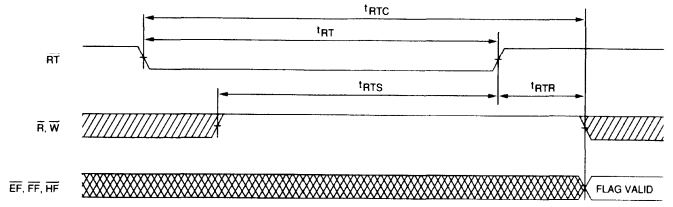
EXPANSION MODE ($\overline{XI}$)



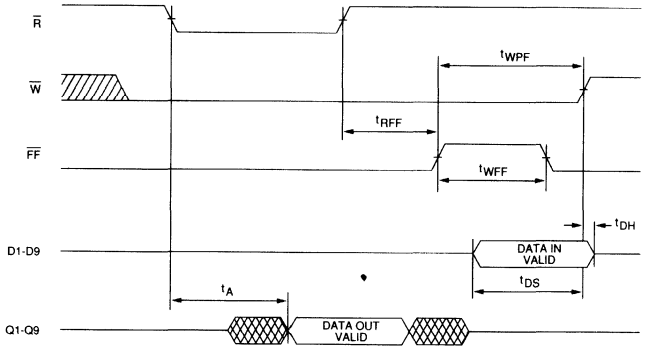
NEW FIFO

NEW FIFO

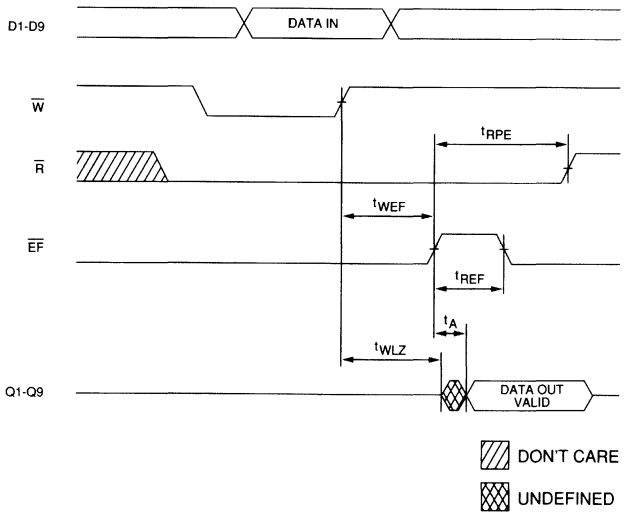
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



MICRON

MT53C51218A1/ 1K18B2/ 2K18C3/ 4K18D4
512 x 18, 1K x 18, 2K x 18, 4K x 18 Synchronous FIFO

FIFO

512 x 18, 1K x 18, 2K x 18 AND 4K x 18 SYNCHRONOUS FIFO

WITH CLOCKED, REGISTERED I/O

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous or simultaneous READ and WRITE clocks
- Empty, Half-Full and Full Flags
- Programmable Almost-Empty and Almost-Full Flags
- Half-Full Flag in STAND ALONE mode
- Fully expandable by width and depth
- Pin- and function-compatible with other FIFOs
- Output Enable for shared bus operation

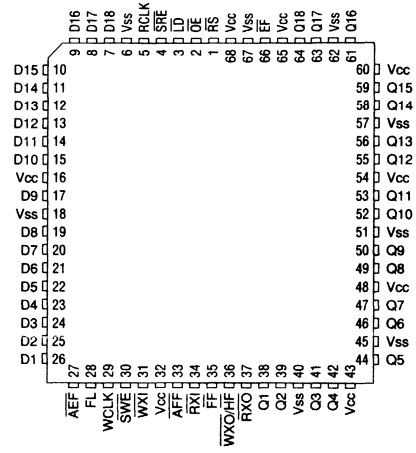
OPTIONS

	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
PLCC	EJ
• Density	
512 x 18	MT53C51218A1
1K x 18	MT53C1K18B2
2K x 18	MT53C2K18C3
4K x 18	MT53C4K18D4
• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT

- Part Number Example: MT53C4K18D4EJ-15

PIN ASSIGNMENT (Top View)

68-Pin PLCC
(SC-3)



GENERAL DESCRIPTION

The Micron synchronous FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

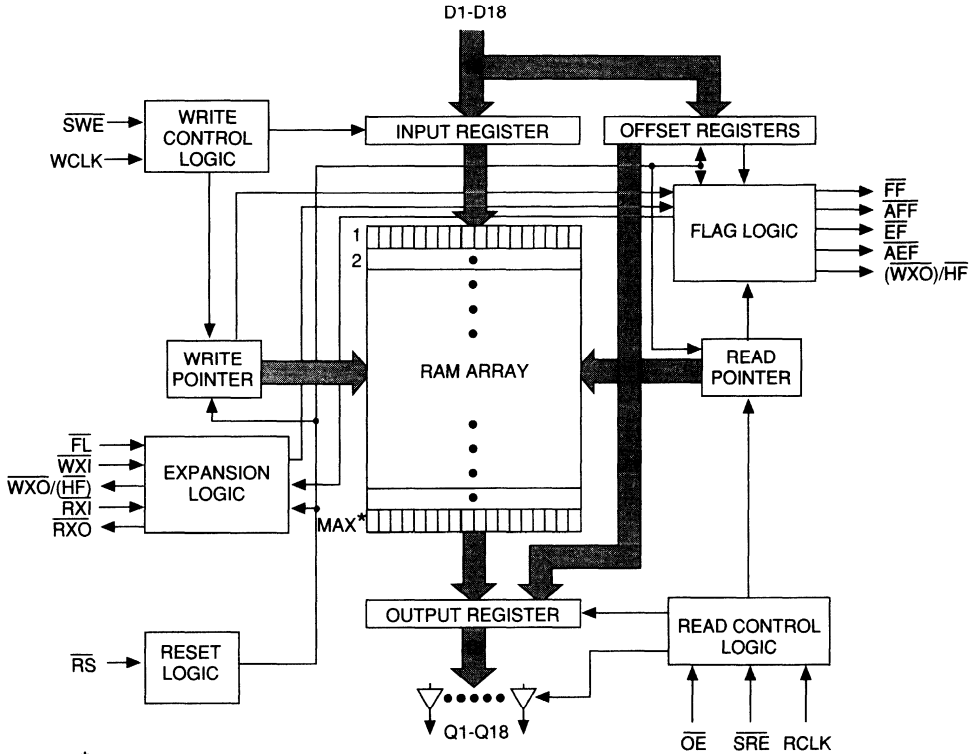
Micron synchronous FIFOs are written and read in a first-in-first-out sequence with clocked write and read control signals. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to the FIFO synchronously to the write clock as controlled by the write enable ($\overline{SWE}$). Information may be read from the FIFO synchronously to the read clock as controlled by the read enable ($\overline{SRE}$) and the asynchronous output enable pin ($\overline{OE}$). The write and read clocks may be tied together or supplied independently. This allows information to be transferred independently in and out of the FIFO at varying data rates.

Visibility of the memory volume is given through the two fixed flags, empty ($\overline{EF}$) and full ($\overline{FF}$), and the two programmable flags, almost-empty ($\overline{AEF}$) and almost-full ($\overline{AFF}$). The programmable flags are initialized using part of the input data bus (D1-D12) and load pin ($\overline{LD}$). While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Read and write expansion out, read and write expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A half full flag is available when the FIFO is in the STAND ALONE mode.

The depth of the FIFO may be expanded by cascading multiple devices using the expansion pins. Width expansion may be realized by using parallel devices.

NEW FIFO

FUNCTIONAL BLOCK DIAGRAM



***NOTE:** MAX = 512 in MT53C51218A1
MAX = 1024 in MT53C1K18B2
MAX = 2048 in MT53C2K18C3
MAX = 4096 in MT53C4K18D4

PIN DESCRIPTIONS

LCC PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	$\overline{RS}$	Input	Reset: This pin is used to reset the device. During device reset, all internal pointers and registers are cleared.
2	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
3	$\overline{LD}$	Input	Load: This active LOW input enables a write to the offset registers at the rising edge of WCLK if $\overline{SWE}$ is LOW. If $\overline{SRE}$ is LOW, a LOW on $\overline{LD}$ enables a read from the offset registers at the rising edge of RCLK.
4	$\overline{SRE}$	Input	Synchronous Read Enable: A LOW on this pin causes the oldest valid data word in the memory array to be read. The internal read pointer is incremented at the subsequent rising edge of RCLK. If this pin is HIGH, the previous data is held in the output register. Data will not be read from the FIFO if $\overline{EF}$ is LOW.
5	RCLK	Input	Read Clock: Data is read on a LOW-to-HIGH transition (rising edge) of this pin if the FIFO is not empty and $\overline{SRE}$ is LOW.
26,25,24,23,22,21, 20,19,17,15,14,13, 12,11,10,9,8,7	D1-D18	Input	Data Inputs: Data on these lines are stored in the memory array or offset registers during array WRITE or register programming, respectively.
27	$\overline{AEF}$	Output	Almost Empty Flag: A LOW on this output pin indicates the FIFO is almost empty. The almost empty offset defaults to 63 from empty in the MT53C512K18A1 and 127 from empty in the MT53C1K18B2/ 2K18C3/ 4K18D4 at reset or can be user programmed.
28	$\overline{FL}$	Input	First Load: In STAND ALONE mode (single device or width expansion mode), this pin is tied LOW. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
29	WCLK	Input	Write Clock: Data is written into the FIFO on a LOW-to-HIGH transition (rising edge) of this pin if the FIFO is not full and $\overline{SWE}$ is LOW.
30	$\overline{SWE}$	Input	Synchronous Write Enable: A LOW on this pin causes data to be written into the next available memory location at the rising edge of WCLK if the FIFO is not full. The internal write pointer is incremented at the following rising edge of WCLK.
31	$\overline{WXI}$	Input	Write Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to $\overline{WXO}$ of the previous device in the daisy chain.
33	$\overline{AFF}$	Output	Almost Full Flag: A LOW on this output pin indicates the FIFO is almost full. The almost full offset defaults to 63 from full in the MT53C512K18A1 and 127 from full in the MT53C1K18B2, 2K18C3 and 4K18D4 at reset or can be user programmed.
34	$\overline{RXI}$	Input	Read Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to $\overline{RXO}$ of the previous device in the daisy chain.

PIN DESCRIPTIONS (continued)

LCC PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
35	$\overline{FF}$	Output	Full Flag: A LOW on this pin indicates that the FIFO is full and further data writes to the FIFO are inhibited. $\overline{FF}$ is synchronized to WCLK.
36	$\overline{WXO}$ /$\overline{HF}$	Output	Write Expansion Out/Half Full Flag: In STAND ALONE mode, a LOW on this pin indicates that the FIFO is more than half full. In DEPTH EXPANSION mode, a pulse is output when the last location in the FIFO is written.
37	$\overline{RXO}$	Output	Read Expansion Out: In DEPTH EXPANSION mode, a pulse is output when the last location of the FIFO is read.
38,39,41,42,44,45, 47,49,50,52,53,55, 56,58,59,61,63,64	Q1-Q18	Output	Data Outputs: These lines output data read from the FIFO memory array or offset registers during array READ or register read, respectively. This 18-bit bus may be placed in high impedance state.
66	$\overline{EF}$	Output	Empty Flag: A LOW on this pin indicates that the FIFO is empty and further data reads from the output are inhibited. $\overline{EF}$ is synchronized to RCLK.
16,32,43,48, 54,60,65,68	Vcc	Supply	Power Supply: +5V ±10%
6,18,40,45, 51,57,62,67	GND	Supply	Ground

NEW FIFO

TRUTH TABLE

OPERATION	$\overline{LD}$	$\overline{SWE}$	$\overline{SRE}$	$\overline{OE}$	WCLK	RCLK	NOTE
Write to Offset Register	0	0	1	X	↑	X	1
Increment Offset Register write pointer (no write)	0	1	1	X	↑	X	1
Write to FIFO memory array	1	0	1	X	↑	X	
Read from Offset Register	0	1	0	0	X	↑	2
Increment Offset Register read pointer (no read)	0	1	1	X	X	↑	2
Read from FIFO memory array	1	1	0	0	X	↑	
Read previously latched output	1	1	1	0	X	X	3
No Operation	1	1	1	1	X	X	

NOTE:
1. First WCLK controlled access after reset points to empty offset register, successive accesses alternate between empty and full offset registers (only offset register write pointer is incremented).
2. First RCLK controlled access after reset points to empty offset register, successive accesses alternate between empty and full offset registers (only offset register read pointer is incremented).
3. Any FIFO read (memory array or offset register which requires that $\overline{SRE}$ is LOW) latches data into the output latch. Data in this latch may be placed on the output bus without initiating a new internal read cycle.

FUNCTIONAL DESCRIPTION

The Micron Synchronous FIFO uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, synchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function not being discussed will be surrounded by parentheses. For example, the WXO/HF pin will be shown as (WXO) HF when discussing half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW with $\overline{SRE}$, $\overline{SWE}$ and $\overline{LD}$ HIGH to initialize the read and write pointers and flags. This also initializes the internal registers (both the Almost Empty Offset Register and Almost Full Offset Register are initialized to 63 in the MT53C51218A1 and 127 in the MT53C1K18B2/ 2K18C3/ 4K18D4). The internal read and write pointers which select these registers is initialized to point to the Almost Empty Offset Register. The full flag, half-full flag and almost full flag will be forced HIGH after reset. The empty flag and almost empty flag will be forced LOW after reset. During Reset, RCLK and WCLK may be free running.

WRITING THE FIFO

A write cycle is initiated at the LOW to HIGH transition (rising edge) of the write clock (WCLK). Data set-up and hold times must be met around that edge for Data (D1-D18) and $\overline{SWE}$ for data to be loaded into the input register (the input register is not altered if $\overline{SWE}$ is HIGH, nor is the FIFO written). Data is written into the FIFO if the FIFO is not full. If the location to be written is the final empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) ^tWKFF after the rising edge of WCLK. While the $\overline{FF}$ is asserted, all writes to the FIFO memory array are inhibited and previously stored data are unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH ^tWKFF after the rising edge of WCLK. When operating in the DEPTH EXPANSION mode, the final location write to a FIFO will cause $\overline{WXO}(\overline{HF})$ to pulse LOW which, when connected to $\overline{WXI}$ of the next FIFO in the chain, facilitates expansion. When operating in the STAND ALONE mode, if the FIFO is exactly half full, then the next write to the FIFO memory array will cause the $(\overline{WXO})\overline{HF}$ flag to be asserted (LOW) ^tKHFF after the rising edge of WCLK. Note that all writes to the FIFO memory array must be performed with the load pin ($\overline{LD}$) HIGH.

READING THE FIFO

A read cycle from the FIFO memory array is initiated at the rising edge of the read clock (RCLK). $\overline{SRE}$ must meet set-up and hold times around the rising edge of RCLK. The output register will then be loaded with the oldest available data word if the FIFO is not empty ($\overline{EF}$ is HIGH). The data output (Q1-Q18) pins will go active (Low-Z) ^tLZOE after the falling edge of $\overline{OE}$. Valid data will appear ^tKQ after the rising edge of RCLK. After the last available data word is read, $\overline{EF}$ will go LOW ^tRKEF after the rising edge of RCLK. While $\overline{EF}$ is asserted LOW, any attempted read from the FIFO memory array will be inhibited. When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH ^tWKFF after the next rising edge of WCLK provided that $^tSKEW1$ from RCLK to WCLK is met; otherwise, $\overline{FF}$ going HIGH will be delayed by one WCLK period. When operating in the DEPTH EXPANSION mode, the last location read from a FIFO will cause $\overline{RXO}$ to pulse LOW. This will enable further reads from the next FIFO in the chain when this output is connected to $\overline{RXI}$ of the next FIFO. During STAND ALONE mode, when the FIFO is greater than half full by one data entry, then the next read from the FIFO memory array will cause the $(\overline{WXO})\overline{HF}$ flag to go HIGH ^tWKHF after the rising edge of RCLK. Note that all reads from the FIFO memory array must be performed with the load pin ($\overline{LD}$) HIGH.

READING/WRITING THE OFFSET REGISTERS

The FIFO contains two 12-bit offset registers (Empty Offset Register and Full Offset Register) and separate register read and write pointers, which allow alternate access to the two registers. A register is written via data bus pins D1-D12 at the rising edge of WCLK if $\overline{SWE}$ is LOW and $\overline{LD}$ is LOW, also incrementing the register write pointer. A register is read from output bus pins Q1-Q12 at the rising edge of RCLK if $\overline{SRE}$ is LOW, $\overline{LD}$ is LOW and $\overline{OE}$ is LOW, also incrementing the register read pointer. The register write pointer may be incremented without writing to a register at the rising edge of WCLK if $\overline{LD}$ is LOW and $\overline{SWE}$ is HIGH. Likewise, the register read pointer may be incremented without reading from a register at the rising edge of RCLK if $\overline{LD}$ is LOW and $\overline{SRE}$ is HIGH. The offset registers must not be read and written simultaneously. An offset value of zero should not be written to either offset register. The unused bits of the offset registers should be set to zero when writing the registers.

NEW FIFO

NEW FIFO

PROGRAMMABLE FLAG OPERATION

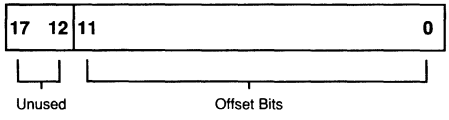
Two 12-bit internal registers have been provided for flag configuration. One is the almost full offset register (AFOR) and the other is the almost empty offset register (AEOR). Bit configurations of the two registers are shown below.

For this discussion, "e" will represent the empty offset contained in the AEOR, "f" will represent the full offset contained in the AFOR and "max" will represent the maximum number of words which can be held by the FIFO memory array.

Note that bits 0-11 are used for offset setting. The increment value ranges from 1 to max-1 words. Each increment value corresponds to a 1-word increment. The unused bits 12-17 are reserved for future expansion, and should be set to 0. An offest value of zero should not be used.

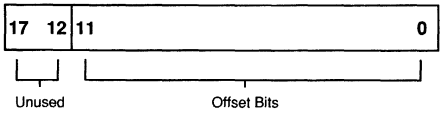
REGISTER SET

Almost Empty Offset Register (AEOR)



Default value: 03FH (MT53C51218A1)
07FH (MT53C1K18B2)
07FH (MT53C2K18C3)
07FH (MT53C4K18D4)

Almost Full Offset Register (AFOR)



Default value: 03FH (MT53C51218A1)
07FH (MT53C1K18B2)
07FH (MT53C2K18C3)
07FH (MT53C4K18D4)

The almost full flag ($\overline{AFF}$) will be asserted (LOW) ^{t}KAFF after the rising edge of WCLK when the almost full condition is met. The Status Flags table (see below) defines the conditions for which almost full is met or invalidated. For example, if f=127 and max=4,096, the almost full condition is met when the 3,969th word location is written in the FIFO. For this same example, when the 3,969th word location in the FIFO is read, the $\overline{AFF}$ will be HIGH ^{t}KAFF after the rising edge of WCLK.

The almost empty flag ($\overline{AEF}$) will be HIGH ^{t}KAEF after the rising edge of WCLK when the almost empty condition is invalidated. The Status Flags table (see below) defines the conditions for which almost full is met or invalidated. For example, if e=127, the almost empty condition is false when the 128th word location is written in the FIFO. For this same example, when the 128th word location in the FIFO is read (leaving 127 words in the FIFO), the $\overline{AEF}$ will be asserted (LOW) ^{t}KAEF after the rising edge of WCLK.

OPERATING CONFIGURATIONS

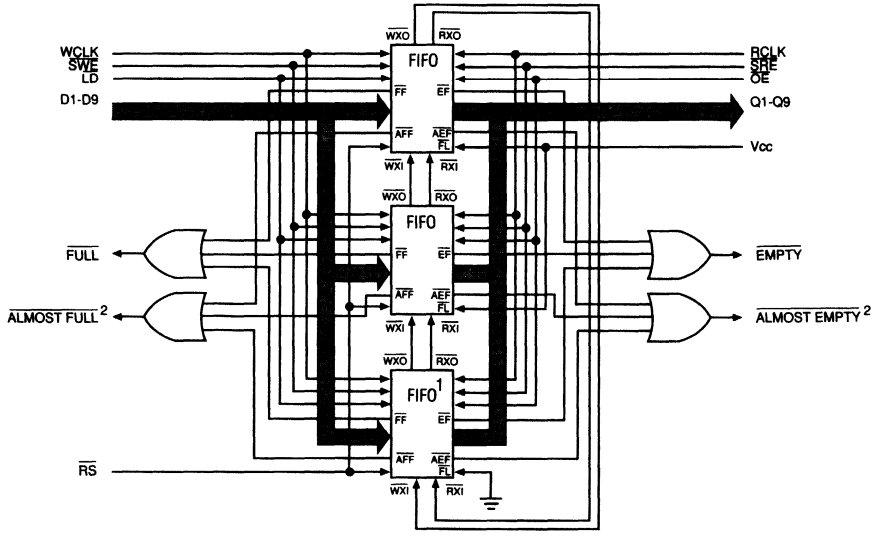
STAND ALONE MODE

Where a single FIFO provides sufficient memory for an application, the FIFO must be used with the following inputs grounded: $\overline{FL}$, $\overline{RXI}$ and $\overline{WXI}$. This places the FIFO in STAND ALONE MODE. All flags in this mode indicate precise internal FIFO status information.

STATUS FLAGS

Number of Words in FIFO								
MT53C51218A1	MT53C1K18B2	MT53C2K18C3	MT53C4K18D4	$\overline{FF}$	$\overline{AFF}$	$\overline{HF}$	$\overline{AEF}$	$\overline{EF}$
0	0	0	0	H	H	H	L	L
1 to e	1 to e	1 to e	1 to e	H	H	H	L	H
(e+1) to 256	(e+1) to 512	(e+1) to 1,024	(e+1) to 2,048	H	H	H	H	H
257 to (511-f)	513 to (1,023-f)	1,025 to (2,047-f)	2,049 to (4,095-f)	H	H	L	H	H
(512-f) to 511	(1,024-f) to 1,023	(2,048-f) to 2,047	(4,096-f) to 4,095	H	L	L	H	H
512	1,024	2,048	4,096	L	L	L	H	H

NOTE: e = Empty Offset
f = Full Offset



NOTE: 1. Format device loaded.
2. Almost empty, almost full flags are not precise in this mode of operation.

Figure 1
DEPTH EXPANSION

NEW FIFO

WIDTH EXPANSION

The FIFO word width may be expanded, in increments of 18 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all input control lines ($\overline{SWE}$, WCLK, $\overline{SRE}$, RCLK, $\overline{LD}$ and $\overline{OE}$) in common. The programmable flags are monitored from any one device in width expansion or one expanded depth group when expanding depth and width. Expanded width operation requires that the user logically AND all the $\overline{FF}$ lines and $\overline{EF}$ lines for a composite $\overline{FF}$ and $\overline{EF}$, respectively. This is necessary because variations in skew between RCLK and WCLK could otherwise result in flag assertion and deassertion to vary by one cycle between FIFOs.

DEPTH EXPANSION

Multiple FIFOs may be cascaded to expand the depth of the FIFO buffer. Five pins are used to expand the memory depth, $\overline{WXI}$, $\overline{WXO}$($\overline{HF}$), $\overline{RXI}$, $\overline{RXO}$ and $\overline{FL}$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{WXO}$($\overline{HF}$) pin of each device to the $\overline{WXI}$ pin of the next device in the chain, and $\overline{RXO}$ pin of each device to the $\overline{RXI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$ pin grounded. The remaining devices in the chain will have $\overline{FL}$ tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{WXO}$($\overline{HF}$) pin will pulse LOW. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first FIFO. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$ pins are LOW.

After the last physical READ of the first device, its $\overline{RXO}$ will pulse LOW, passing the read pointer to the next device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag is not available and the composite almost empty and almost full flags are imprecise.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7V
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NEW FIFO

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{SWE}$ or $\overline{SRE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	200	200	200	200	mA	3
Power Supply Current: Standby	$\overline{OE}$, $\overline{SWE}$ and $\overline{SRE}$ ≥ V_{IH}; V_{CC} = MAX; f = MAX = 1/^tRC Outputs Open	I_{SB1}	50	50	50	50	mA	
	$\overline{OE}$, $\overline{SWE}$ and $\overline{SRE}$ ≥ V_{CC} -0.2; V_{CC} = MAX; V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ V_{CC} -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
General											
Clock cycle frequency	^tFS		66.7		50		40		28.6	MHz	
Clock cycle time	^tKC	15		20		25		35		ns	
Clock HIGH time	^tKH	6.5		8		10		14		ns	
Clock LOW time	^tKL	6.5		8		10		14		ns	
Synchronous enable set-up time	^tSES	4		5		6		7		ns	
Synchronous enable hold time	^tSEH	1		1		1		2		ns	
READ Cycle											
Clock to output valid (data access time)	^tRKQ	2	10	2	12	2	15	2	20	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output Enable LOW to output valid	^tOEQ		8		9		12		15	ns	
Output Enable HIGH to output in High-Z	^tHZOE	1	8	1	9	1	12	1	15	ns	
Read Clock to Empty Flag	^tRKEF		10		12		15		20	ns	
WRITE Cycle											
Data set-up time	^tDS	4		5		6		7		ns	
Data hold time	^tDH	1		1		1		2		ns	
Write clock to Full Flag	^tWKFF		10		12		15		20	ns	
Flags											
Clock to Almost Full Flag	^tKAFF		28		30		35		40	ns	
Clock to Almost Empty Flag	^tKAEF		28		30		35		40	ns	
Clock to Half Full Flag	^tKHFF		28		30		35		40	ns	
Skew time between RCLK and WCLK for Full Flag	$^tSKEW1$	10		14		16		18		ns	
Skew time between RCLK and WCLK for Empty Flag	$^tSKEW2$	10		14		16		18		ns	
Expansion Logic											
Clock to Expansion Out	^tKXO		10		12		15		20	ns	
Expansion In Pulse Width	^tXIP	6.5		8		10		14		ns	5
Expansion In set-up time	^tXIS	5		8		10		15		ns	
RESET Cycle											
RESET set-up time	^tRSS	10		12		15		20		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	5
RESET recovery time	^tRSR	10		12		15		20		ns	
RESET to Flag and Output time	^tRSF		35		35		40		45	ns	

NEW FIFO

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	3ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

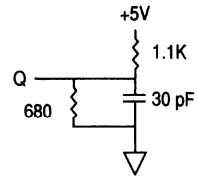
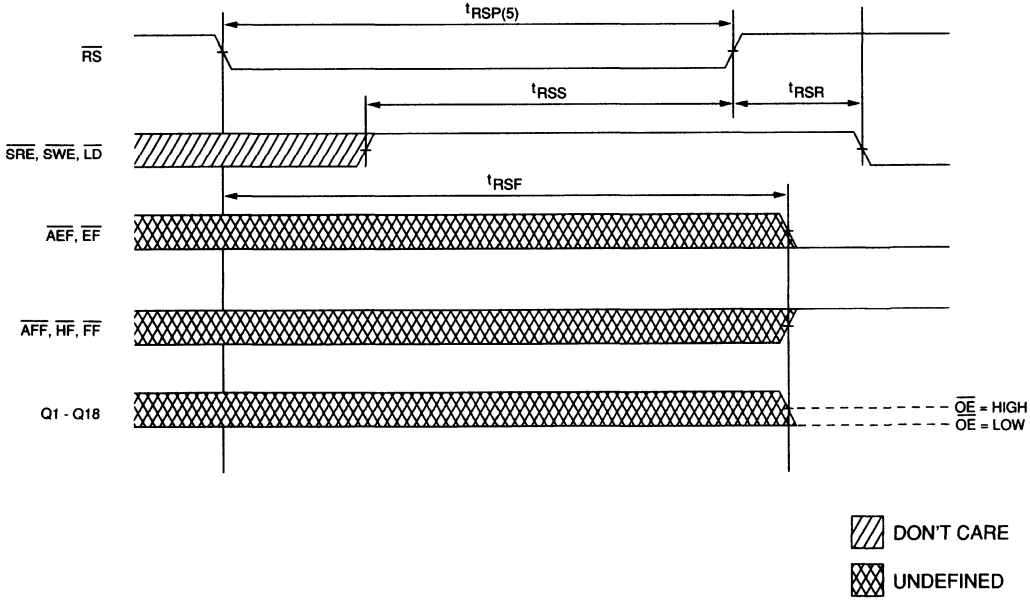


Figure 2
OUTPUT LOAD EQUIVALENT

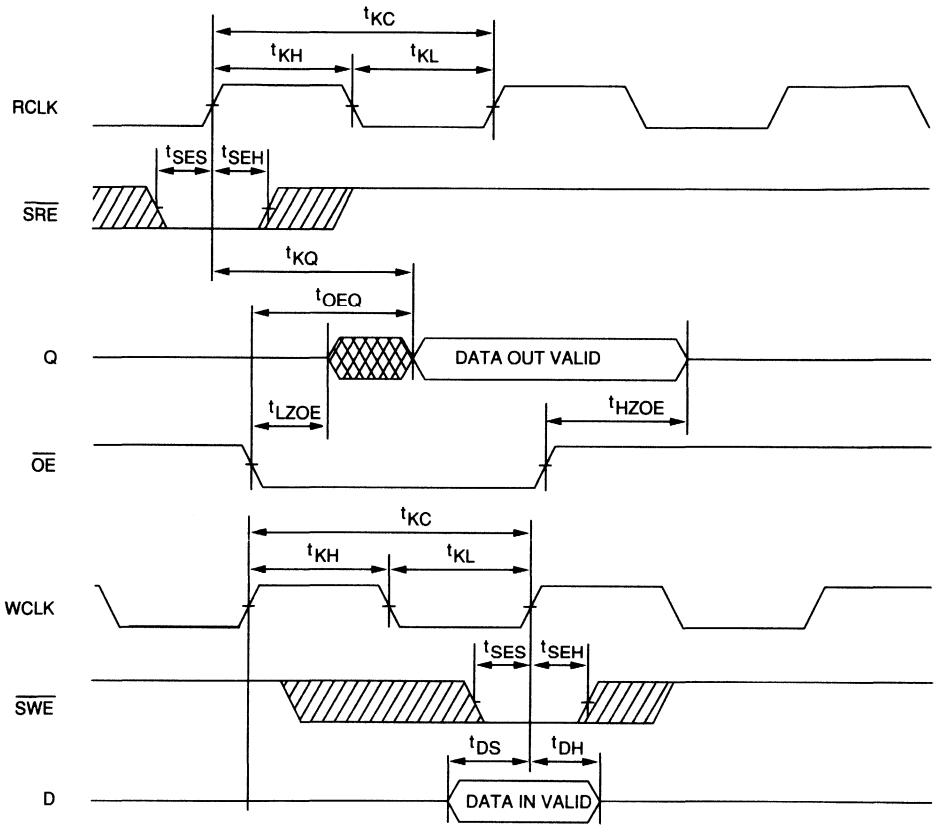
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Pulse widths less than minimum are not allowed.
6. Values guaranteed by design, not currently tested.
7. $\overline{LD}$ = HIGH.
8. FIFO read and write can occur simultaneously.

RESET



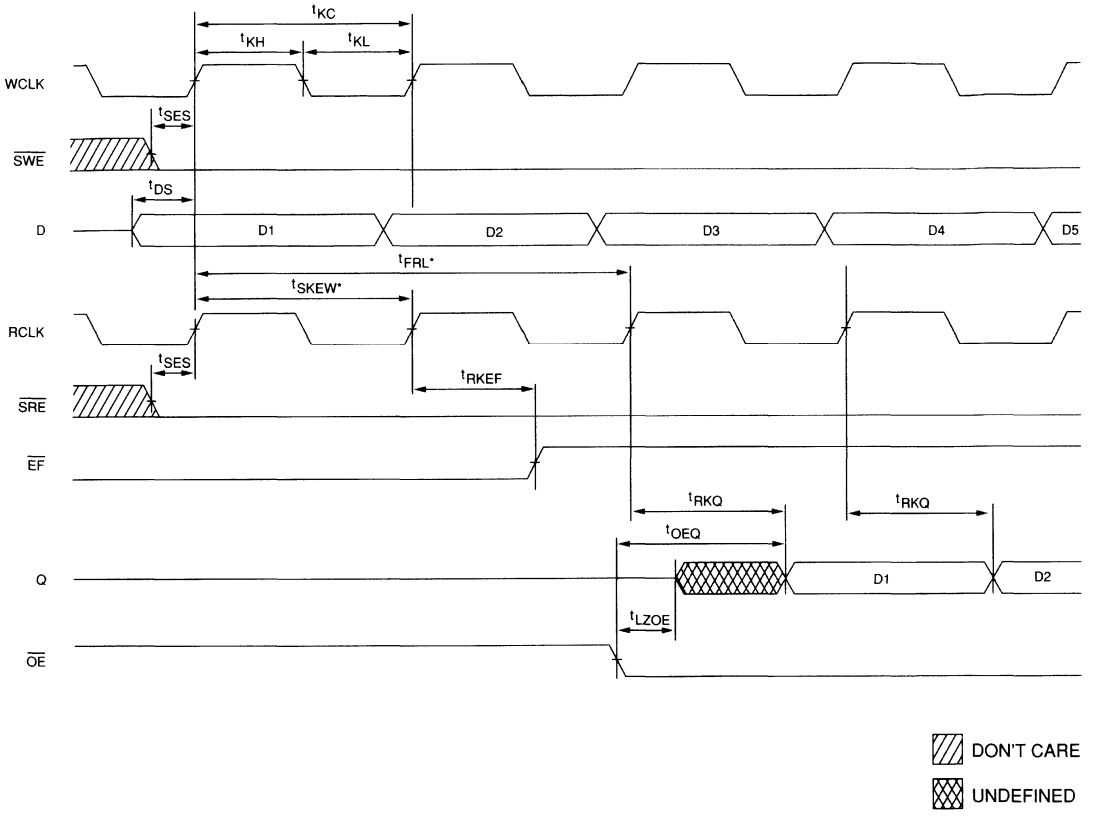
READ/WRITE CYCLE TIMING[7, 8]



NEW FIFO

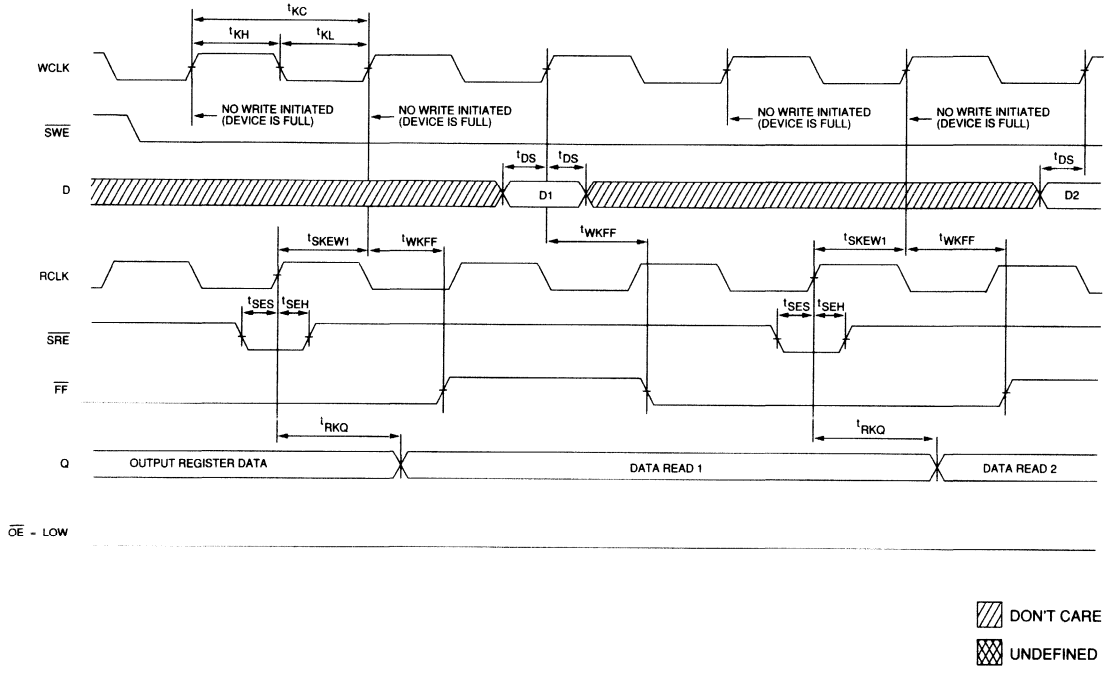
NEW FIFO

FIRST DATA WORD LATENCY AFTER RESET[7, 8]
(SIMULTANEOUS READ AND WRITE)



***NOTE:** When ^{t}SKEW ≥ ^{t}SKEW2 (MIN), then ^{t}FRL (MAX) = ^{t}KC (of RCLK) + ^{t}SKEW.
When ^{t}SKEW < ^{t}SKEW2 (MIN), then ^{t}FRL (MAX) = 2 * ^{t}KC (of RCLK) + ^{t}SKEW or ^{t}KC (of RCLK) + ^{t}SKEW.
The first word is available the cycle after $\overline{EF}$ goes HIGH.

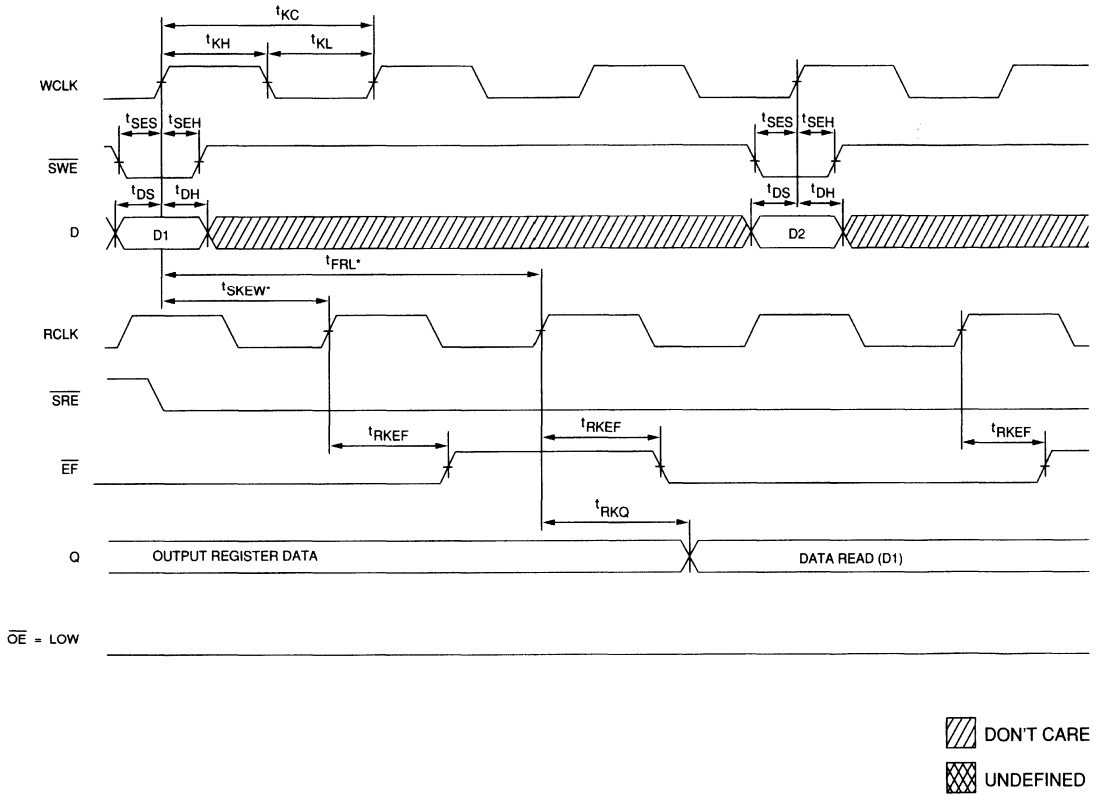
FULL FLAG TIMING[7, 8]



NOTE: tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge such that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{FF}$ may not change state until the next WCLK edge.

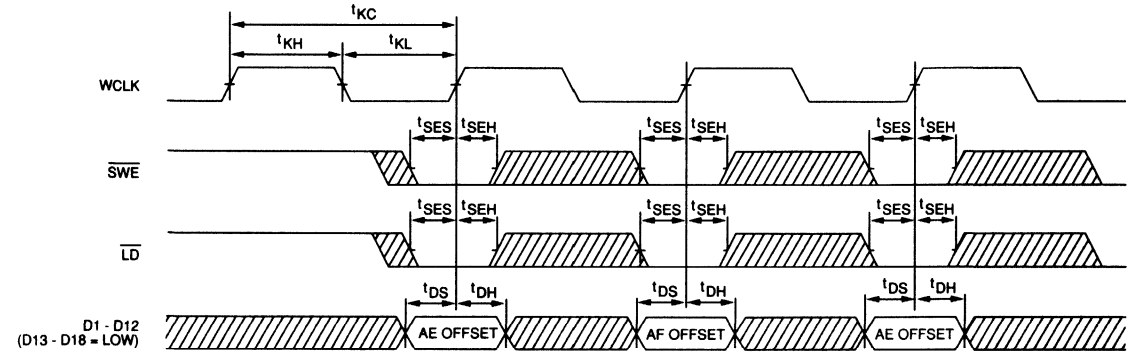
NEW FIFO

EMPTY FLAG TIMING[7, 8]

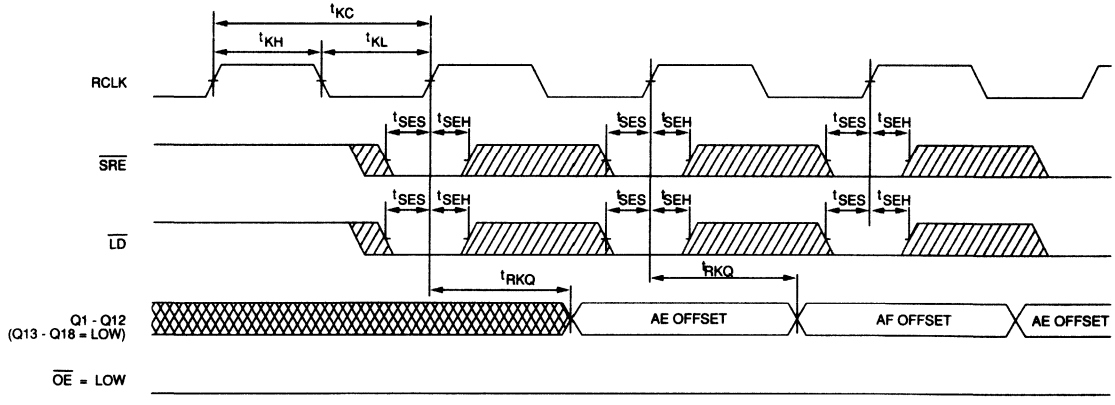


NOTE: When ^{t}SKEW ≥ ^{t}SKEW2 (MIN), then ^{t}FRL (MAX) = ^{t}KC (of RCLK) + ^{t}SKEW.
When ^{t}SKEW < ^{t}SKEW2 (MIN), then ^{t}FRL (MAX) = 2 * ^{t}KC (of RCLK) + ^{t}SKEW or ^{t}KC (of RCLK) + ^{t}SKEW.
The latency timing applies only at the empty boundary ($\overline{EF}$ = LOW).

OFFSET REGISTER WRITE TIMING



OFFSET REGISTER READ TIMING

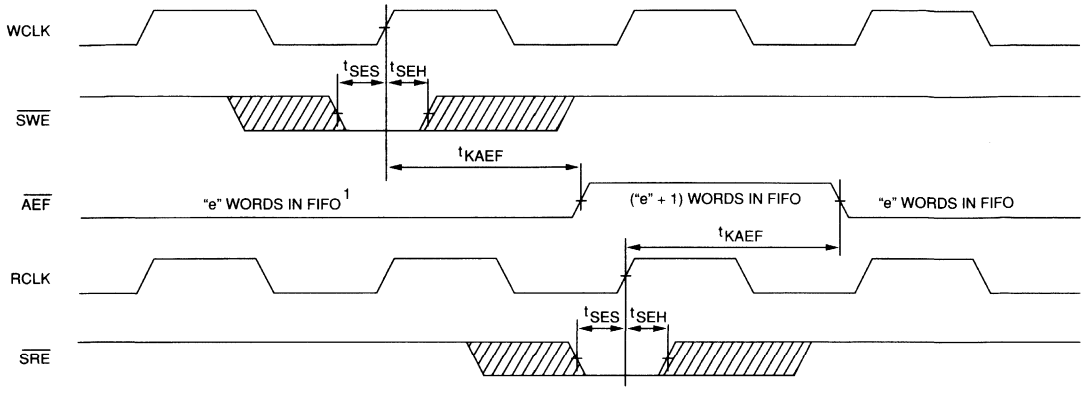


DON'T CARE

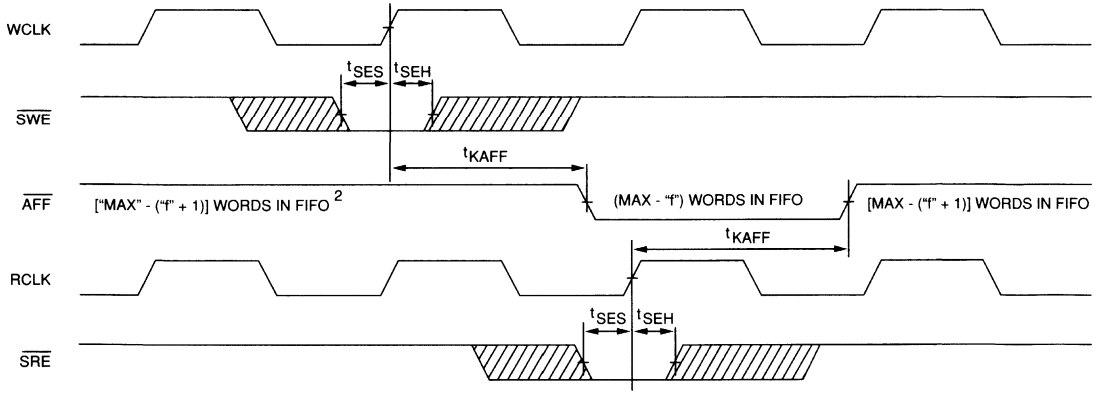
UNDEFINED

NEW FIFO

ALMOST EMPTY FLAG TIMING



ALMOST FULL FLAG TIMING

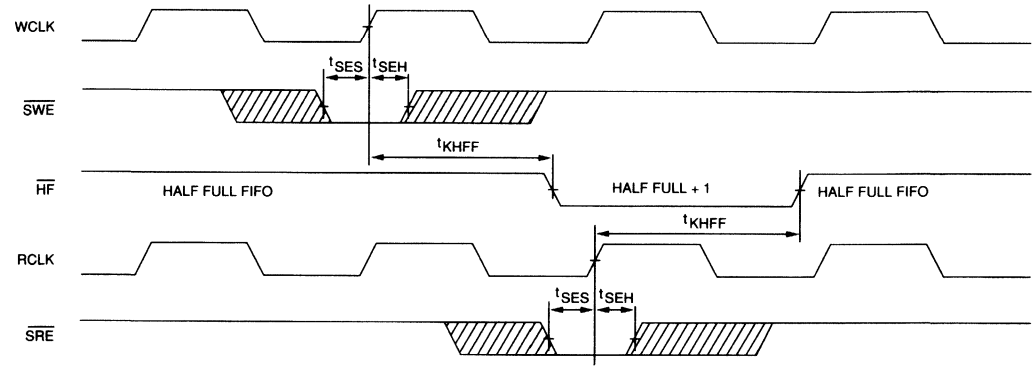


DON'T CARE

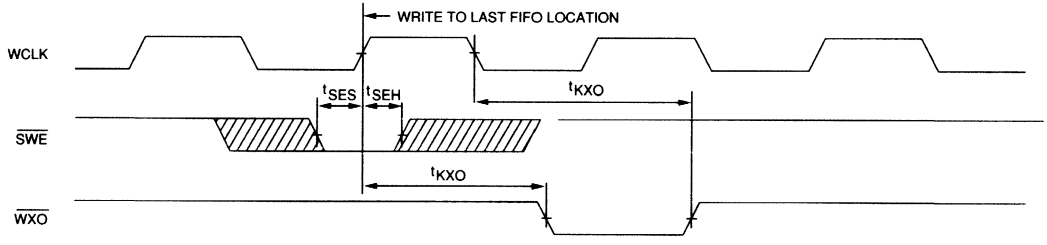
UNDEFINED

NOTE: 1. AEF Offset = "e". Number of data words stored in FIFO already = "e".
2. AFF Offset = "f". Number of data words stored in FIFO already = "MAX" - ("f" + 1) where "MAX" is the maximum number of words that may be held in the FIFO.

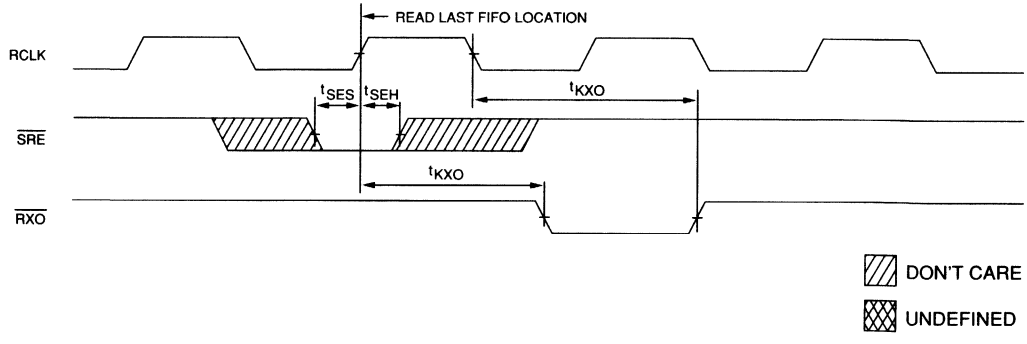
HALF FULL FLAG TIMING



WRITE EXPANSION OUT TIMING

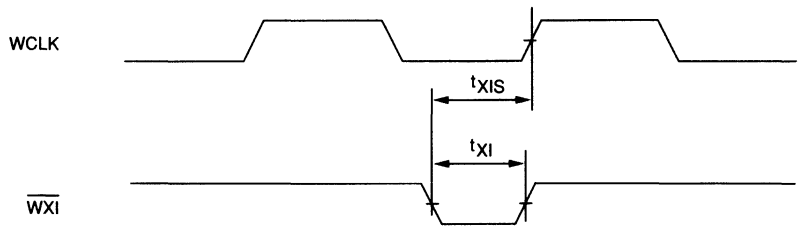


READ EXPANSION OUT TIMING

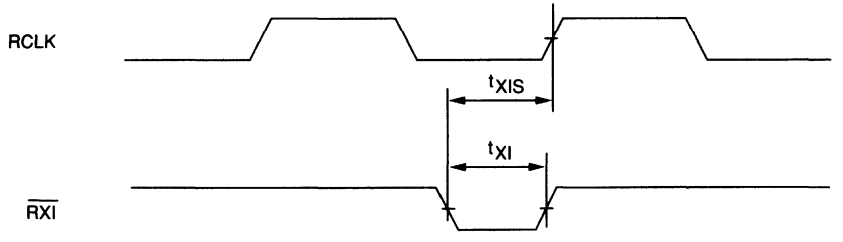


NEW FIFO

WRITE EXPANSION IN TIMING



READ EXPANSION IN TIMING



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -0.5V to +7V
IT ..... -40°C+85°C
AT ..... -40°C+125°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to Vss ..... -1V to Vcc +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS AND DC ELECTRICAL CHARACTERISTICS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-0.5	0.8	V	1, 2

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; Vcc = MAX f = MAX = 1/tRC Outputs Open	Icc	160	150	140	mA	3
Power Supply Current: Standby	W, $\overline{R} \ge V_{IH}$; Vcc = MAX f = MAX = 1/tRC Outputs Open	ISB1	20	20	20	mA	
	$\overline{W}, \overline{R} \ge$ Vcc -0.2; Vcc = MAX $V_{IN} \le$ Vss +0.2 or $V_{IN} \ge$ Vcc -0.2; f = 0	ISB2	7	7	7	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	ILI	-10	10	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	ILO	-10	10	µA	
Output High Voltage	IOH = -2.0mA	VOH	2.4		V	1
Output Low Voltage	IOL = 8.0mA	VOL		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	CI	8	pF	4
Output Capacitance	Vcc = 5V	CO	8	pF	4

NEW FIFO

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-20		-25		-35			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		33.3		28.5		22.2	MHz	
Access time	^tA		20		25		35	ns	
READ cycle time	^tRC	30		35		45		ns	
READ recovery time	^tRR	10		10		10		ns	
READ pulse width	^tRPW	20		25		35		ns	6
READ LOW to Low-Z	^tRLZ	3		3		3		ns	
READ HIGH to High-Z	^tRHZ		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	^tOH	5		5		5		ns	
WRITE cycle time	^tWC	30		35		45		ns	
WRITE pulse width	^tWPW	20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		ns	5
Data setup time	^tDS	12		15		18		ns	
Data hold time	^tDH	0		0		0		ns	
RESET cycle time	^tRSC	30		35		45		ns	
RESET pulse width	^tRSP	20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		ns	
READ HIGH to RESET HIGH	^tRRS	20		25		35		ns	
WRITE HIGH to RESET HIGH	^tWRS	20		25		35		ns	
RETRANSMIT cycle time	^tRTC	30		35		45		ns	
RETRANSMIT pulse width	^tRT	20		25		35		ns	
RETRANSMIT recovery time	^tRTR	10		10		12		ns	
RETRANSMIT setup time	^tRTS	20		25		35		ns	
RESET to $\overline{AEF}$, $\overline{EF}$ LOW	^tEFL		30		35		45	ns	
RESET to $\overline{AEF}$, $\overline{HF}$, $\overline{FF}$ HIGH	^tHFH, ^tFFH		30		35		45	ns	
READ LOW to $\overline{EF}$ LOW	^tREF		20		25		30	ns	
READ HIGH to $\overline{FF}$ HIGH	^tRFF		20		25		30	ns	
WRITE LOW to $\overline{FF}$ LOW	^tWFF		20		25		30	ns	
WRITE HIGH to $\overline{EF}$ HIGH	^tWEF		20		25		30	ns	
WRITE LOW to $\overline{HF}$ LOW	^tWHF		30		35		45	ns	
READ HIGH to $\overline{HF}$ HIGH	^tRHF		30		35		45	ns	
READ HIGH after $\overline{EF}$ HIGH	^tRPE	20		25		35		ns	5
WRITE HIGH after $\overline{FF}$ HIGH	^tWPF	20		25		35		ns	5
READ/WRITE to $\overline{XO}$ LOW	^tXOL		20		25		35	ns	
READ/WRITE to $\overline{XO}$ HIGH	^tXOH		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	20		25		35		ns	
$\overline{XI}$ setup time	^tXIS	12		15		15		ns	
$\overline{XI}$ recovery time	^tXIR	10		10		10		ns	

NEW FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through mode only.
6. Pulse widths less than minimum are not allowed.

MICRON

SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins			Page
				DIP	ZIP	SIMM	
128K x 8	$\overline{CE}$ and $\overline{OE}$	MT4S1288	20*, 25, 30	32	-	-	8-1
32K x 16	$\overline{CE}$ and $\overline{OE}$	MT2S3216	20*, 25, 30	40	-	-	8-9
64K x 16	$\overline{CE}$ and $\overline{OE}$	MT4S6416	20*, 25, 30	40	-	-	8-17
16K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S1632	10*, 15, 20, 25, 35	-	64	64	8-25
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S6432	15*, 20, 25, 30, 35	-	64	64	8-33
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4S12832	15*, 20, 25, 35	-	64	64	8-41
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S25632	15*, 20, 25, 35	-	64	64	8-49

*Preliminary

SRAM MODULE

128K x 8 SRAM

FEATURES

- High speed: 20*, 25 and 30ns
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL compatible
- Pin compatible with monolithic 1 Meg SRAM

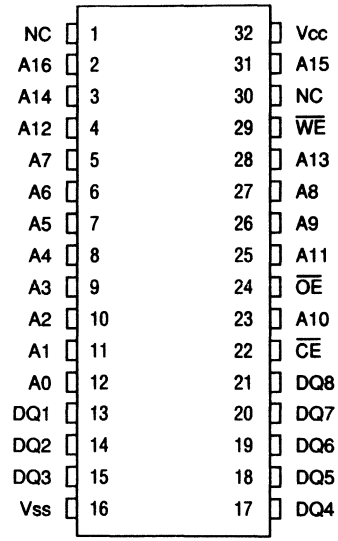
OPTIONS — MARKING

- Timing
  - 20ns access — -20*
  - 25ns access — -25
  - 30ns access — -30
- Packages
  - 32-pin DIP (600 mil) — D
- Part Number Example: MT4S1288D-20

*Preliminary

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SI-1)



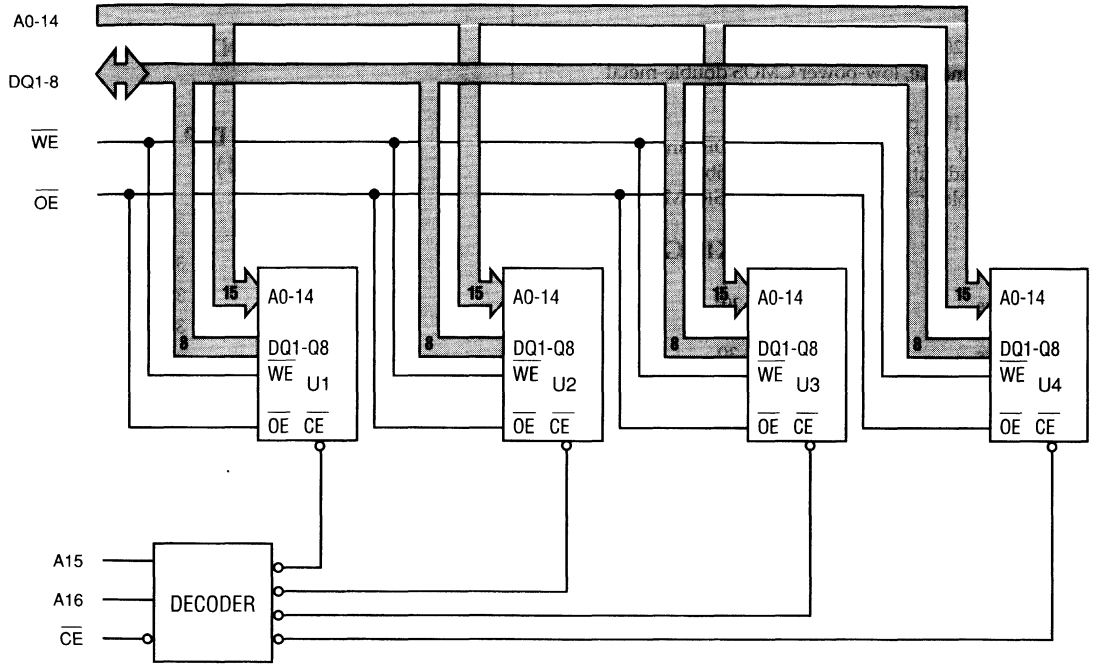
GENERAL DESCRIPTION

The MT4S1288 is a high-speed SRAM memory module containing 131,072 words organized in a x8-bit configuration. The module consists of four 32K x 8 fast static RAMs and a single decoder mounted on a 32-pin DIP, FR4 printed circuit board.

The decoder interprets the higher order address bits (A15 and A16) to select one of the four fast static RAMs. Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading is accomplished when $\overline{WE}$ remains HIGH, and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ sets the output in High-Z for additional system design flexibility and memory expansion may be achieved through use of the $\overline{OE}$ and $\overline{CE}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C2568DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A14, $\overline{WE}$, $\overline{OE}$	I_{LI}	-20	20	µA	
		A15, A16, $\overline{CE}$			600	µA	
Input/Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	DQ1-DQ8	I_{LO}	-20	20	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		1	
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}	0.4	0.4	V	1
Supply Voltage			V_{CC}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX			UNITS	NOTES
				-20*	-25	-30		
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	170	320	280	210	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	60	120	120	120	mA	13
Standby Current: CMOS Input Levels	$\overline{CE} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2 or $V_{IN} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	40	40	40	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A14 $\overline{WE}$,& $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_{I1}	28	pF	4
Input Capacitance: A15, A16 & $\overline{CE}$		C_{I22}	5	pF	4
Input/Output Capacitance: DQ1-DQ8		C_{IO}	8	pF	4

SRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION		-20*		-25		-30			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		30		ns	
Address access time	^tAA		20		25		30	ns	
Chip Enable access time	^tACE		20		25		30	ns	
Output hold from address change	^tOH	3		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	4		6		6		ns	7
Chip Enable to output in High-Z	^tHZCE		8		9		20	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		20		25		30	ns	
Output Enable access time	^tAOE		8		8		10	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		7		7		10	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		20		25		ns	
Chip Enable to end of write	^tCW	15		15		25		ns	
Address valid to end of write	^tAW	15		15		18		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	10		15		25		ns	
WRITE pulse width	$^tWP2$	12		15		25		ns	
Data setup time	^tDS	7		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	4		5		5		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		7		10		12	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

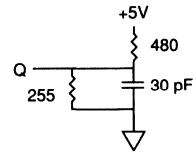


Fig. 1 OUTPUT LOAD EQUIVALENT

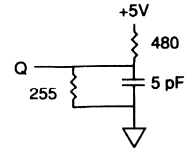
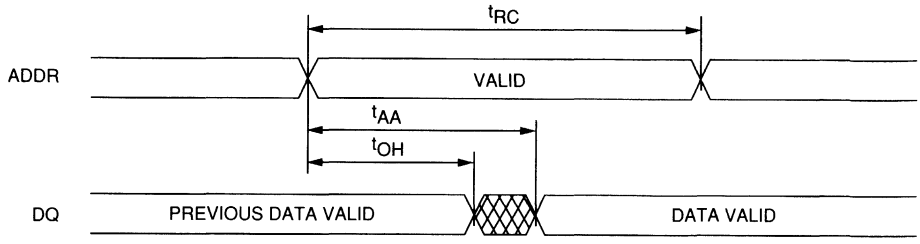


Fig. 2 OUTPUT LOAD EQUIVALENT

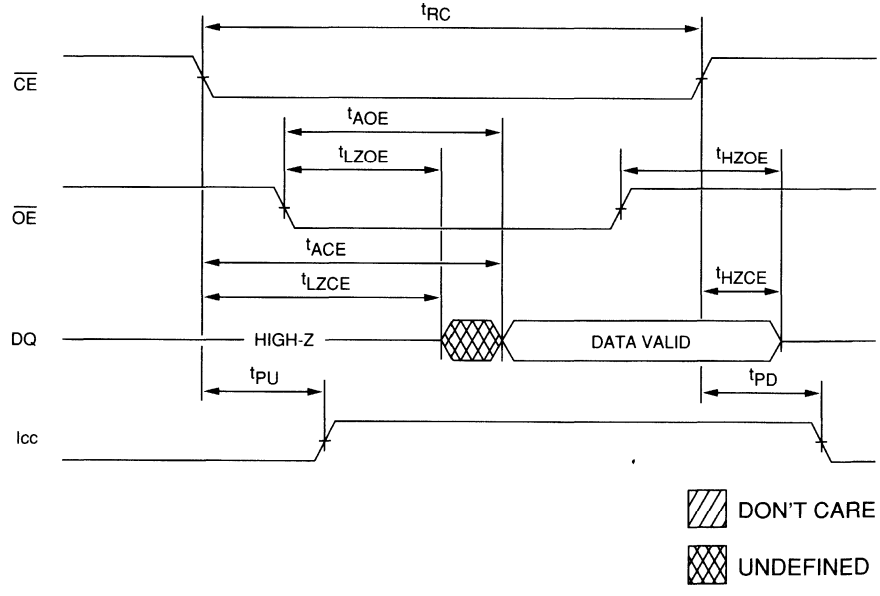
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

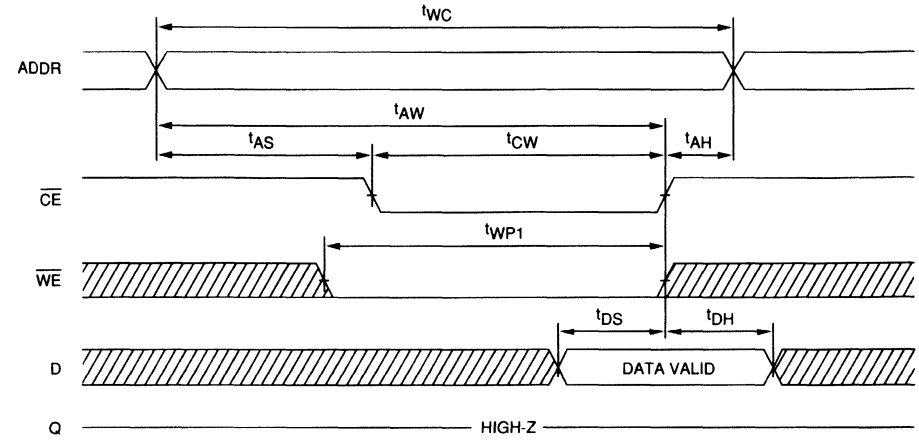
READ CYCLE NO. 1 [8, 9]



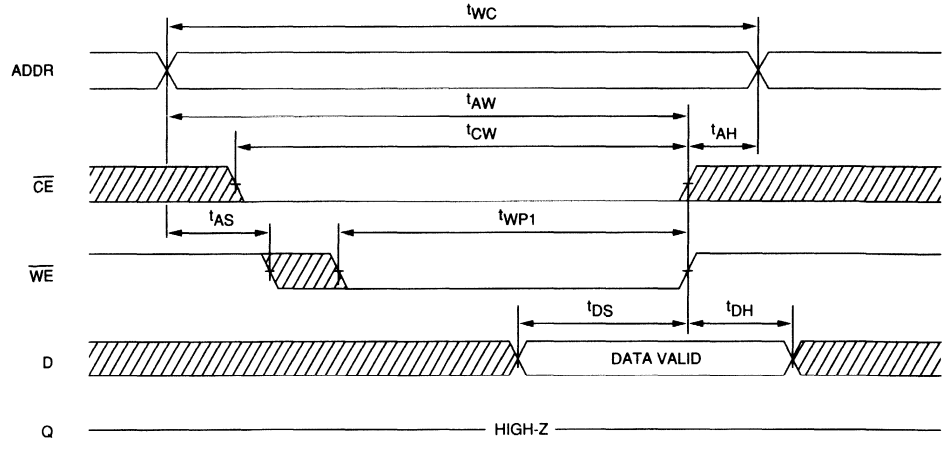
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

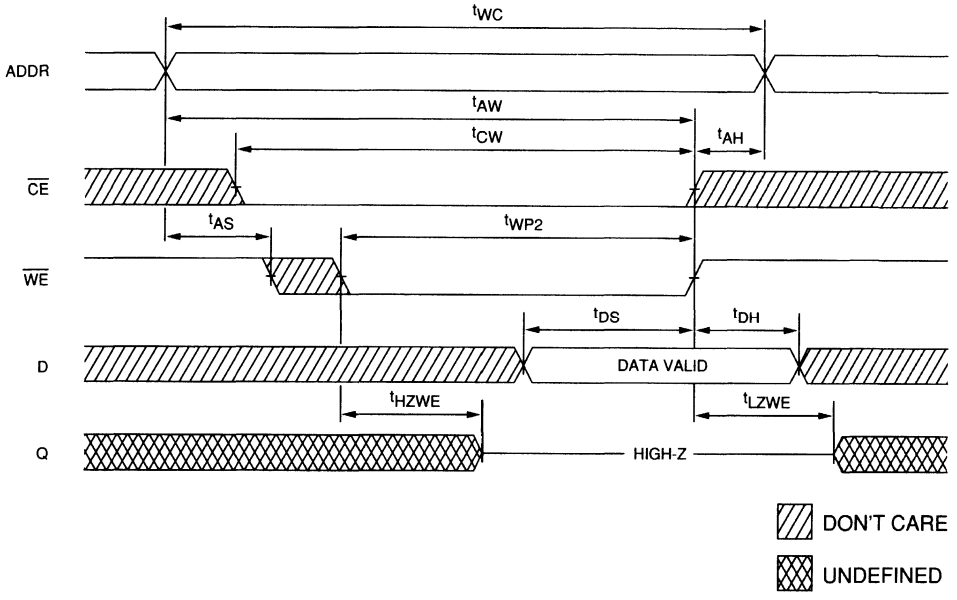


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

32K x 16 SRAM

FEATURES

- High speed: 20*, 25 and 30ns
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Upper and lower byte select
- All inputs and outputs are TTL compatible

OPTIONS

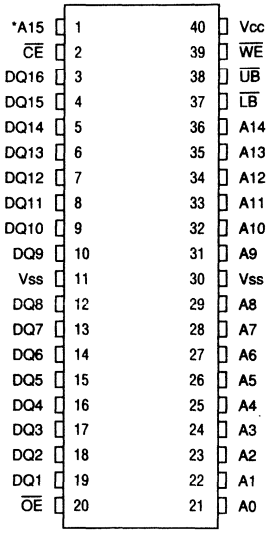
	MARKING
• Timing	
20ns access	-20*
25ns access	-25
30ns access	-30
• Packages	
40-pin DIP (600 mil)	D

- Part Number Example: MT2S3216D-20

*Preliminary

PIN ASSIGNMENT (Top View)

40-Pin DIP
(SI-2)



*Address A15 must be connected to Vss.

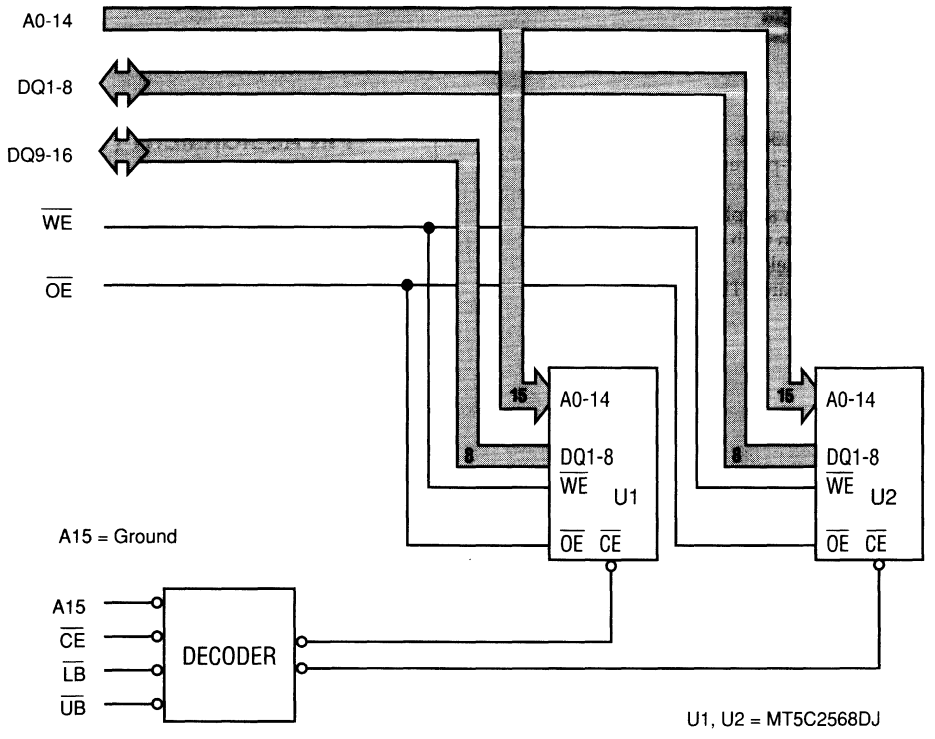
GENERAL DESCRIPTION

The MT2S3216 is a high-speed SRAM memory module containing 32,768 words organized in a x16-bit configuration. The module consists of two 32K x 8 fast static RAMs and a single decoder mounted on a 40-pin DIP, FR4 printed circuit board.

Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ sets the output in High-Z for additional system design flexibility, and memory expansion may be achieved through use of the $\overline{OE}$ and $\overline{CE}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	A15	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	L	HIGH-Z	STANDBY
STANDBY	L	H	H	X	X	L	HIGH-Z	STANDBY
READ: WORD	L	L	L	L	H	L	Q1-16	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	L	H	L	Q1-8	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	L	H	L	Q9-16	ACTIVE (x8)
READ: WORD	L	L	L	H	H	L	HIGH-Z	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	H	H	L	HIGH-Z	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	H	H	L	HIGH-Z	ACTIVE (x8)
WRITE: WORD	L	L	L	X	L	L	D1-16	ACTIVE (x16)
WRITE: LOWER BYTE	L	H	L	X	L	L	D1-8	ACTIVE (x8)
WRITE: UPPER BYTE	L	L	H	X	L	L	D9-16	ACTIVE (x8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IH}	2.2	Vcc+1	V	1
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IH}	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IL}	-0.5	0.8	V	1, 2
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A14, $\overline{WE}$, $\overline{OE}$	I_{LI}	-10	10	µA	
		A15, $\overline{CE}$			1,200	µA	
		$\overline{UB}$, $\overline{LB}$			600	µA	
Input/Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ16	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		1	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	4.5	5.5	V	1

DESCRIPTION		CONDITIONS	SYMBOL	TYP	MAX -20*	MAX -25	MAX -30	UNITS	NOTES
Operating Current: TTL Input Levels	(x16)	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	Icc	170	280	260	210	mA	3, 13
	(x8)			85	140	140	140	mA	3, 13
Standby Current: TTL Input Levels		$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX =1/ ^tRC Outputs Open	I_{SB1}	30	70	70	70	mA	13
Standby Current: CMOS Input Levels		$\overline{CE}$ ≥ Vcc -0.2; Vcc = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ Vcc -0.2; f = 0	I_{SB2}	5	35	35	35	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A14, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	14	pF	4
Input Capacitance: A15, $\overline{CE}$		C_{I2}	10	pF	4
Input Capacitance: $\overline{UB}$, $\overline{LB}$		C_{I3}	5	pF	4
Input/Output Capacitance: DQ		C_{IO}	8	pF	4

SRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20*		-25		-30			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		30		ns	
Address access time	^tAA		20		25		30	ns	
Chip Enable access time	^tACE		20		25		30	ns	
Output hold from address change	^tOH	3		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	4		6		5		ns	7
Chip Enable to output in High-Z	^tHZCE		8		9		20	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		20		25		30	ns	
Output Enable access time	^tAOE		8		8		10	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		7		7		10	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		20		25		ns	
Chip Enable to end of write	^tCW	15		15		25		ns	
Address valid to end of write	^tAW	15		15		18		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	10		15		25		ns	
WRITE pulse width	$^tWP2$	12		15		25		ns	
Data setup time	^tDS	7		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	4		5		5		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		7		10		12	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

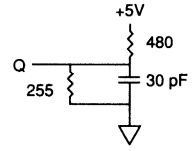


Fig. 1 OUTPUT LOAD EQUIVALENT

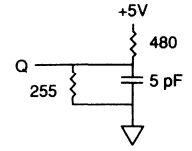
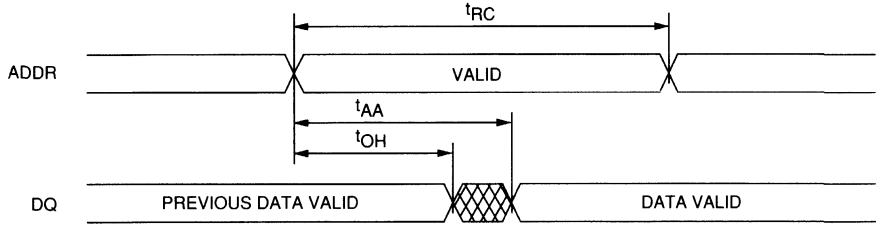


Fig. 2 OUTPUT LOAD EQUIVALENT

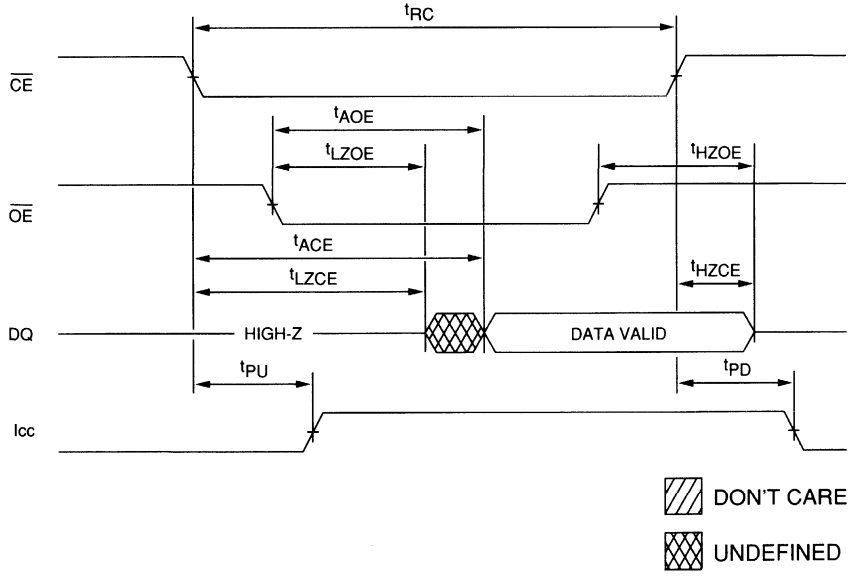
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}HZCE$, $^{t}HZOE$ and $^{t}HZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}HZCE$ is less than $^{t}LZCE$, $^{t}HZWE$ is less than $^{t}LZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

READ CYCLE NO. 1 [8, 9]

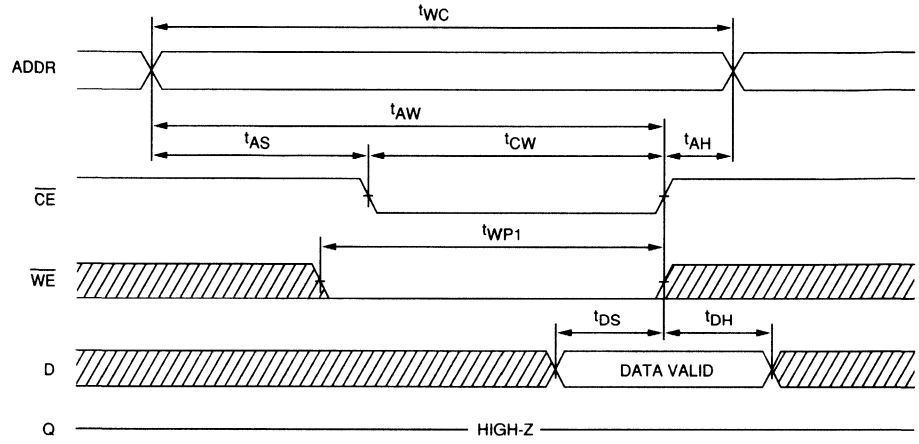


READ CYCLE NO. 2 [7, 8, 10]

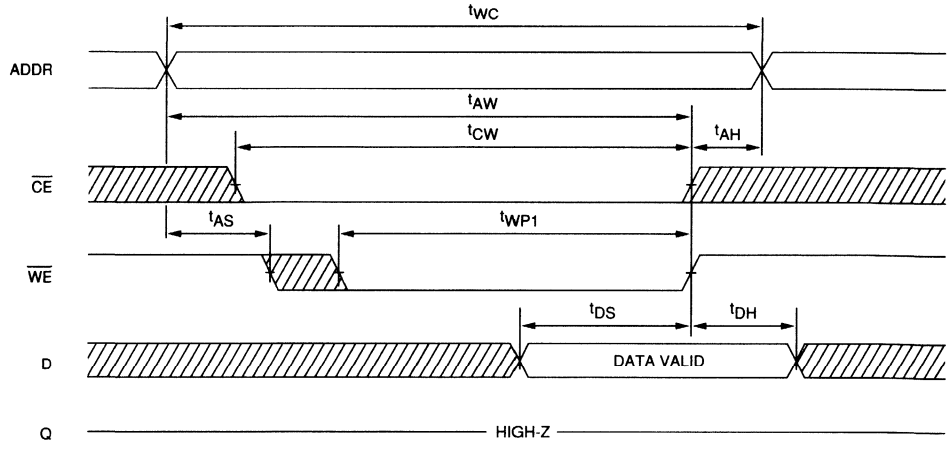


SRAM MODULE

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

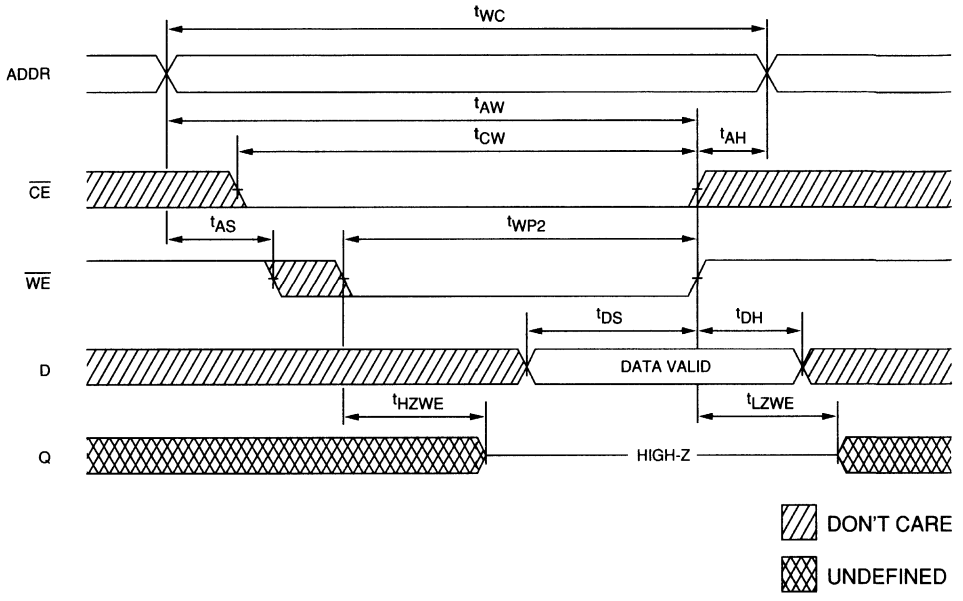


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

64K x 16 SRAM

FEATURES

- High speed: 20*, 25 and 30ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Upper and lower byte select
- All inputs and outputs are TTL compatible

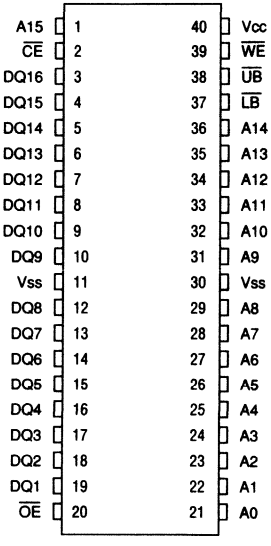
OPTIONS — MARKING

- Timing
  - 20ns access — -20*
  - 25ns access — -25
  - 30ns access — -30
- Packages
  - 40-pin DIP (600 mil) — D
- Part Number Example: MT4S6416D-20

*Preliminary

PIN ASSIGNMENT (Top View)

40-Pin DIP
(SI-3)



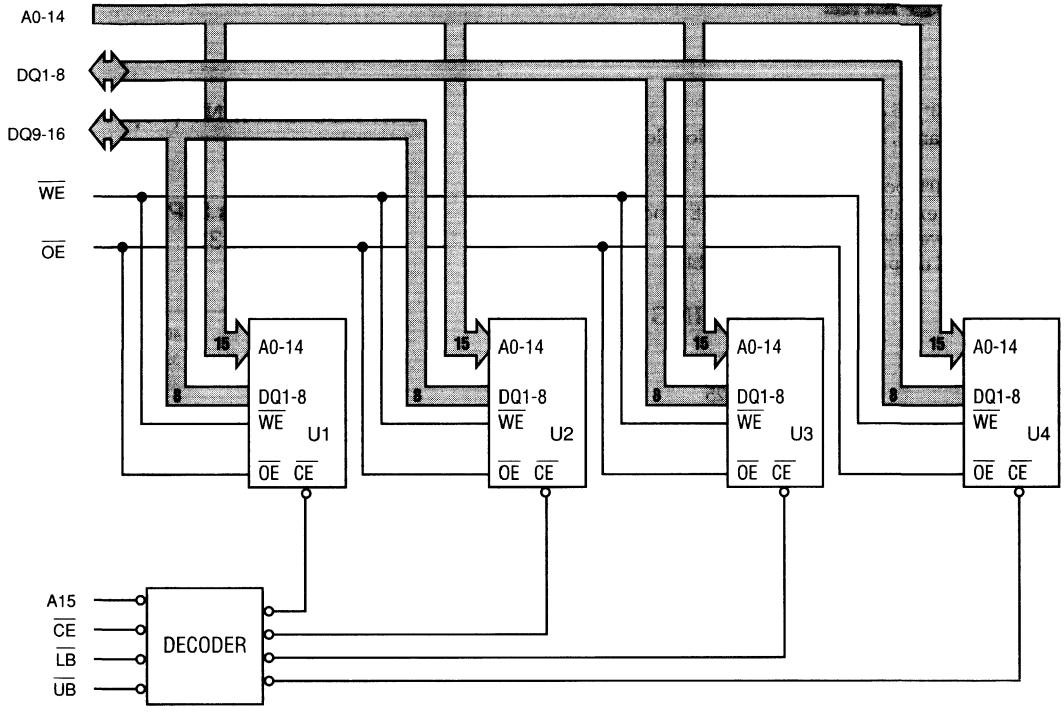
GENERAL DESCRIPTION

The MT4S6416 is a high-speed SRAM memory module containing 65,536 words organized in a x16-bit configuration. The module consists of four 32K x 8 fast static RAMs and a single decoder mounted on a 40-pin DIP, double-sided FR4 printed circuit board.

The decoder interprets the higher order address bit (A15) to select two of the four fast static RAMs. Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ sets the output in High-Z for additional system design flexibility and memory expansion may be achieved through use of the $\overline{OE}$ and $\overline{CE}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components can be powered from a single +5V supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C2568DJ

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	HIGH-Z	STANDBY
STANDBY	L	H	H	X	X	HIGH-Z	STANDBY
READ: WORD	L	L	L	L	H	Q1-16	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	L	H	Q1-8	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	L	H	Q9-16	ACTIVE (x8)
READ: WORD	L	L	L	H	H	HIGH-Z	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	H	H	HIGH-Z	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	H	H	HIGH-Z	ACTIVE (x8)
WRITE: WORD	L	L	L	X	L	D1-16	ACTIVE (x16)
WRITE: LOWER BYTE	L	H	L	X	L	D1-8	ACTIVE (x8)
WRITE: UPPER BYTE	L	L	H	X	L	D9-16	ACTIVE (x8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IH}	2.2	Vcc+1	V	
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IH}	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IL}	-0.5	0.8	V	1, 2
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A14	I_{LI}	-20	20	µA	
		A15, $\overline{CE}$			1,200	µA	
		$\overline{UB}$, $\overline{LB}$			600	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc		I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	4.5	5.5	V	1

DESCRIPTION		CONDITIONS	SYMBOL	TYP	MAX -20*	MAX -25	MAX -30	UNITS	NOTES
Operating Current: TTL Input Levels	(x16)	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX =1/ ^tRC Outputs Open	Icc	170	310	290	250	mA	3, 13
	(x8)			85	140	140	140	mA	13
Standby Current: TTL Input Levels		$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX =1/ ^tRC Outputs Open	I_{SB1}	60	120	120	120	mA	13
Standby Current: CMOS Input Levels		$\overline{CE}$ ≥ Vcc -0.2; Vcc = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ Vcc -0.2; f = 0	I_{SB2}	5	40	40	40	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A14, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	32	pF	4
Input Capacitance: A15, $\overline{CE}$		C_{I2}	10	pF	4
Input Capacitance: $\overline{UB}$, $\overline{LB}$		C_{I3}	5	pF	4
Input/Output Capacitance: DQ		C_{IO}	16	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20*		-25		-30			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		30		ns	
Address access time	^tAA		20		25		30	ns	
Chip Enable access time	^tACE		20		25		30	ns	
Output hold from address change	^tOH	3		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	4		6		5		ns	7
Chip Enable to output in High-Z	^tHZCE		8		9		20	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		20		25		30	ns	
Output Enable access time	^tAOE		8		8		20	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		7		7		20	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		20		30		ns	
Chip Enable to end of write	^tCW	15		15		25		ns	
Address valid to end of write	^tAW	15		15		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	10		15		25		ns	
WRITE pulse width	$^tWP2$	12		15		25		ns	
Data setup time	^tDS	7		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	4		5		5		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		7		10		20	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

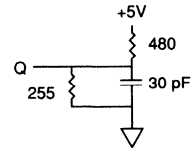


Fig. 1 OUTPUT LOAD EQUIVALENT

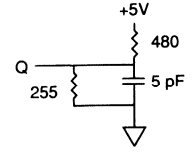
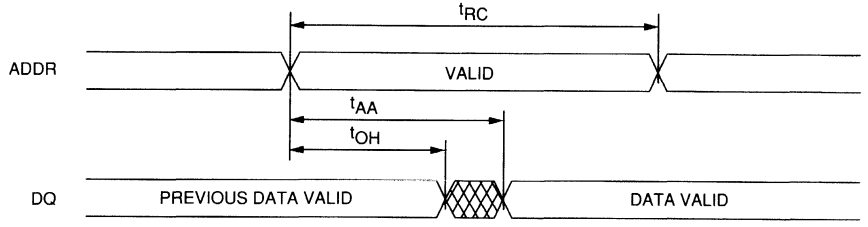


Fig. 2 OUTPUT LOAD EQUIVALENT

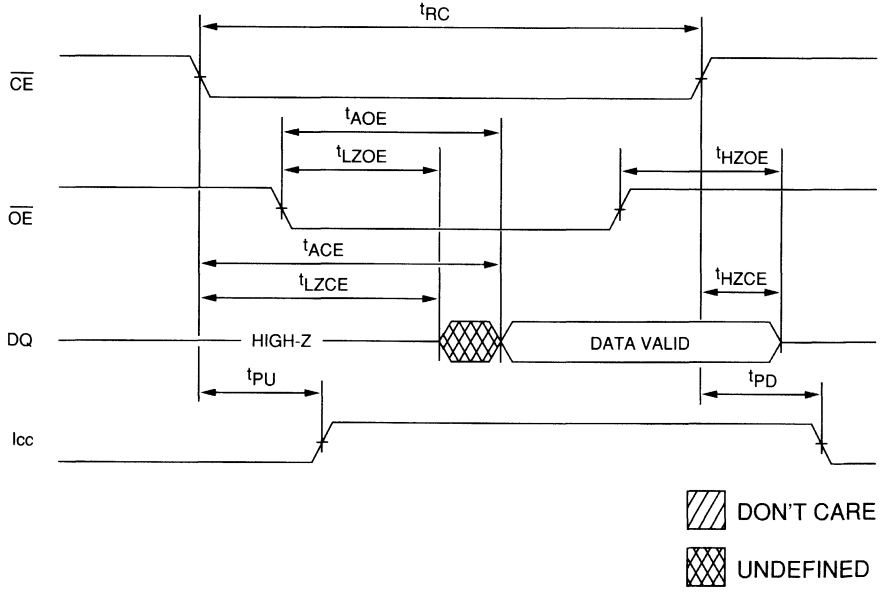
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE and ^{t}HZWE are less than ^{t}LZCE and ^{t}LZWE respectively.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

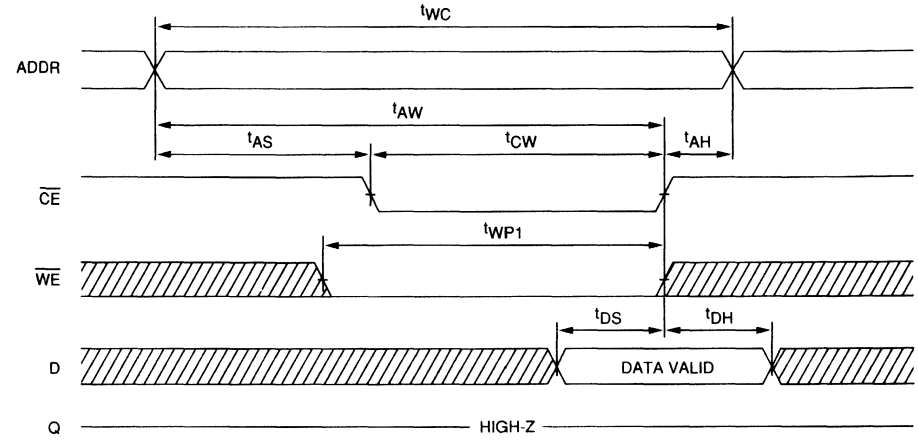
READ CYCLE NO. 1 [8, 9]



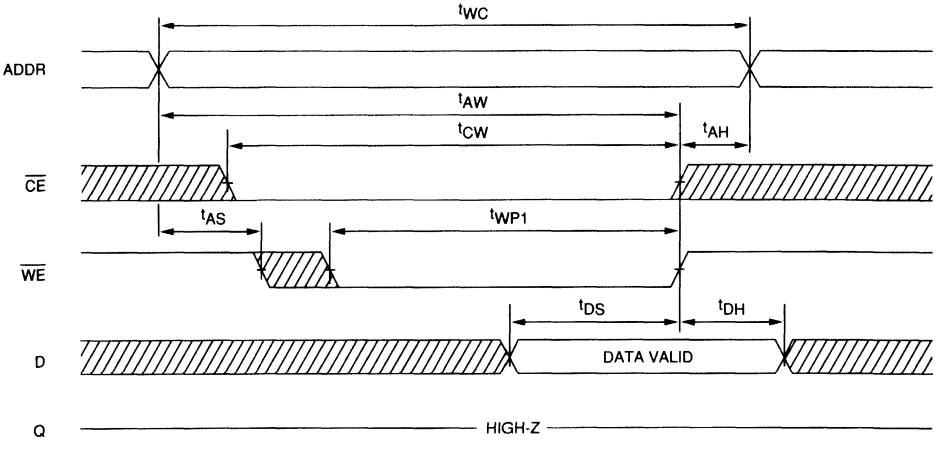
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

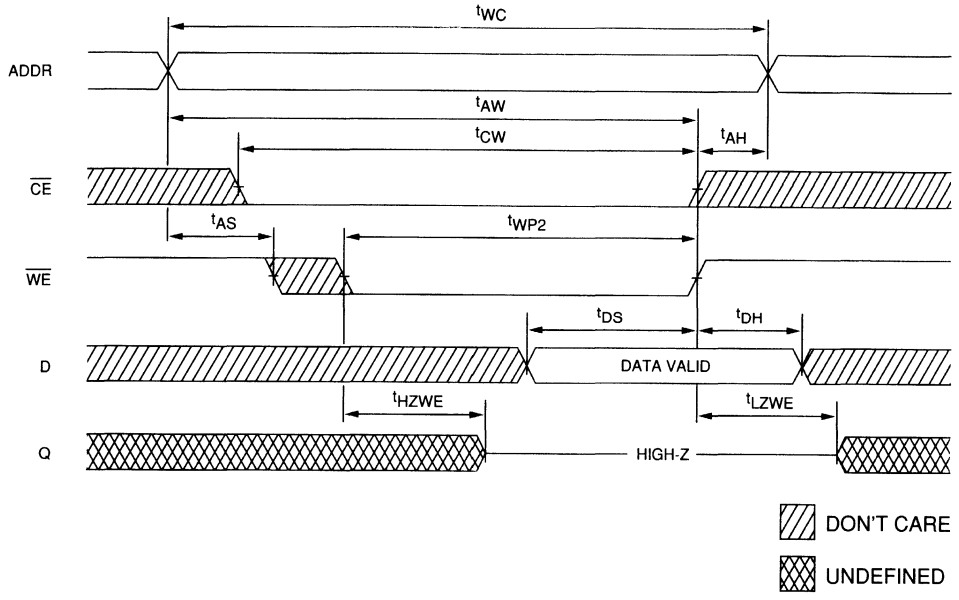


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

16K x 32 SRAM

FEATURES

- High speed: 10*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile
- All inputs and outputs are TTL compatible
- Industry standard pinout
- Upgradable with 64K x 32, 128K x 32 and 256K x 32 modules

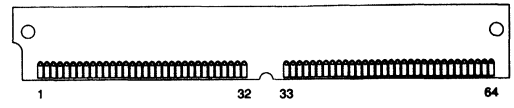
OPTIONS MARKING

- Timing
  - 10ns access -10*
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
  - 35ns access -35
- Packages
  - 64-pin SIMM M
  - 64-pin ZIP Z
- 2V data retention L
- Part Number Example: MT8S1632M-10 L

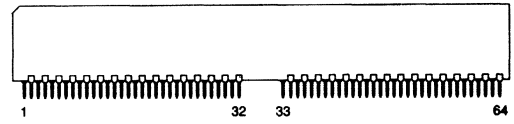
*Preliminary

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SG-1)



64-Pin ZIP
(SH-2)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	NC	45	DQ28	61	DQ31
14	A7	30	NC	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

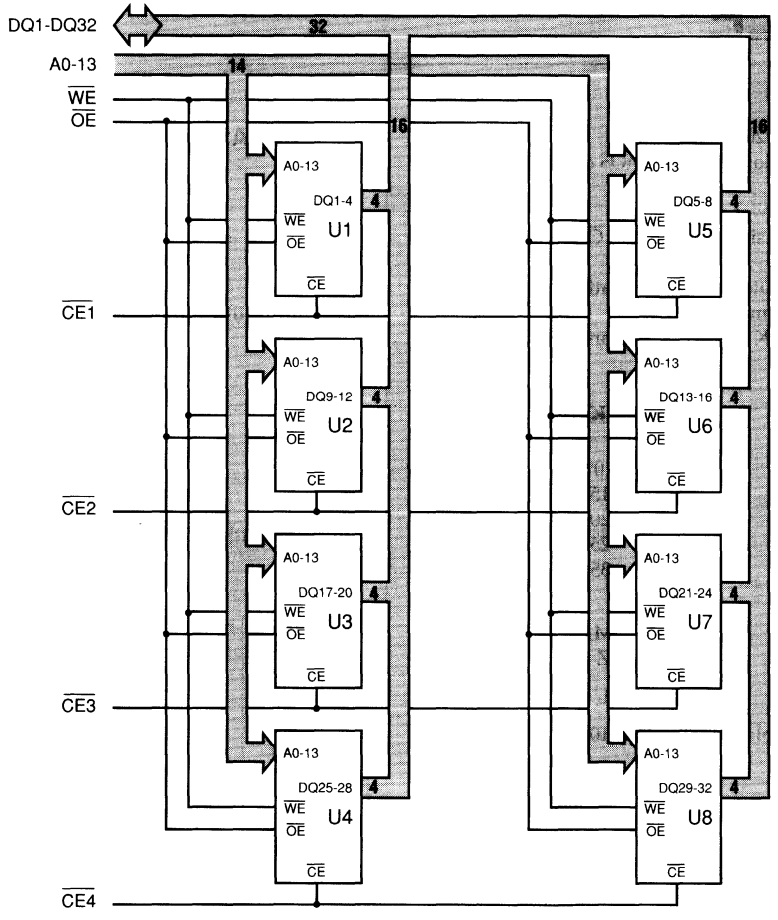
The MT8S1632 is a high-speed SRAM memory module containing 16,384 words organized in a x32-bit configuration. The module consists of eight 16K x 4 fast static RAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ can set the output in High-Z for additional flexibility in system design, and memory expansion is accomplished by use of the $\overline{OE}$ and $\overline{CE}$ functions.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate-density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$), are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = Vss
PD1 = No Connect

U1-U8 = MT5C6405DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10*	-15	-20	-25	-35	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	520	1,280	960	880	800	720	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	160	440	320	280	240	200	mA	13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	3.2	24	24	24	40	24	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A13, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz	C_I	70	pF	4
Input/Output Capacitance: DQ1-DQ32	V_{CC} = 5V	$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	tRC	10		15		20		25		35		ns	
Address access time	tAA		10		15		20		25		35	ns	
Chip Enable access time	tACE		8		12		15		20		30	ns	
Output hold from address change	tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE†	2		2		2		2		2		ns	7, 14
Chip Enable to output in High-Z	tHZCE		5		7		8		8		8	ns	6, 7
Chip disable to power-up time	tPU	0		0		0		0		0		ns	
Chip Enable to power-down time	tPD		10		15		20		25		35	ns	
Output Enable access time	tAOE		4		6		7		8		15	ns	
Output disable to output in Low-Z	tLZOE	0		0		0		0		0		ns	
Output Enable to output in High-Z	tHZOE		4		6		7		8		8	ns	6
WRITE Cycle													
WRITE cycle time	tWC	10		15		20		25		35		ns	
Chip Enable to end of write	tCW	8		12		15		20		25		ns	
Address valid to end of write	tAW	8		12		15		20		25		ns	
Address setup time	tAS	0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		ns	
WRITE pulse width	tWP1	7		10		12		15		20		ns	
WRITE pulse width	tWP2	9		14		18		20		25		ns	
Data setup time	tDS	6		8		9		10		12		ns	
Data hold time	tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	tHZWE		5		6		8		8		8	ns	6, 7

*Preliminary

†The difference between the shaded and unshaded parameters is explained in note 14 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

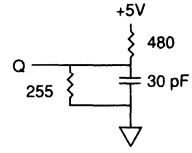


Fig. 1 OUTPUT LOAD EQUIVALENT

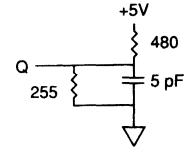


Fig. 2 OUTPUT LOAD EQUIVALENT

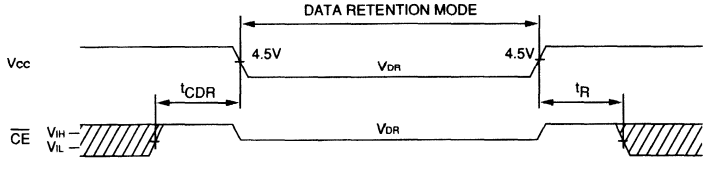
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		760	2,000	µA	
		Vcc = 3V			1,000	3,200	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

LOW Vcc DATA-RETENTION WAVEFORM

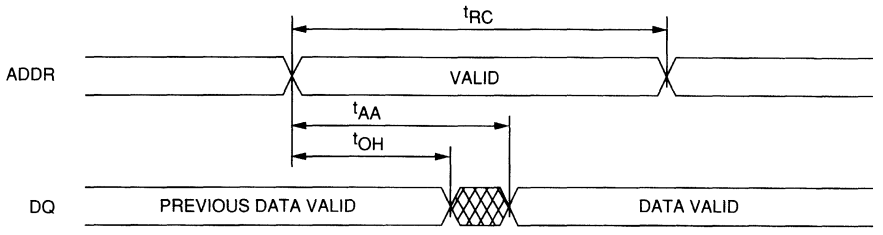


DON'T CARE

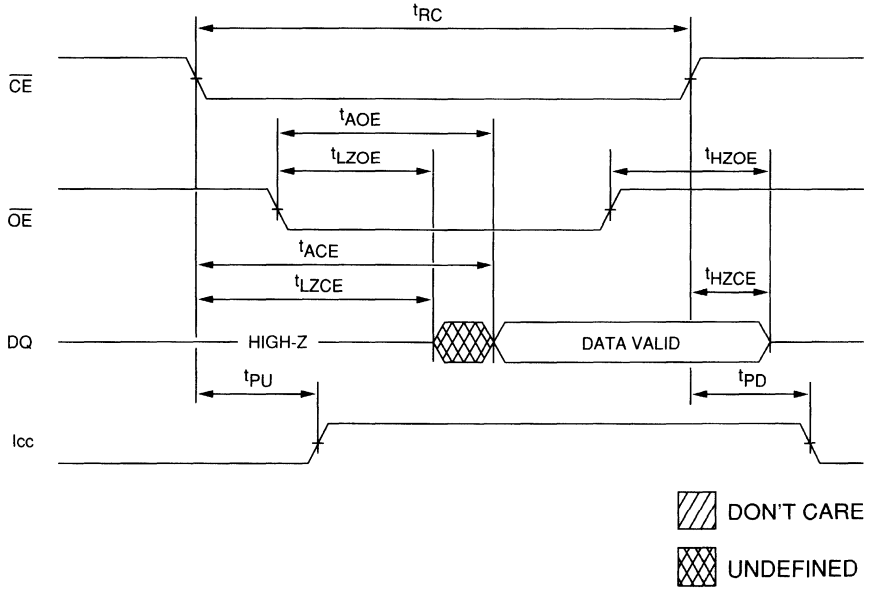
UNDEFINED

SRAM MODULE

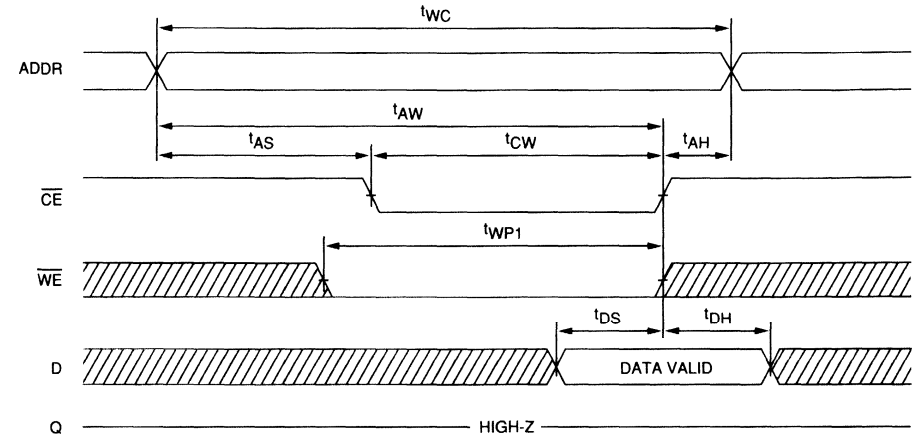
READ CYCLE NO. 1 [8, 9]



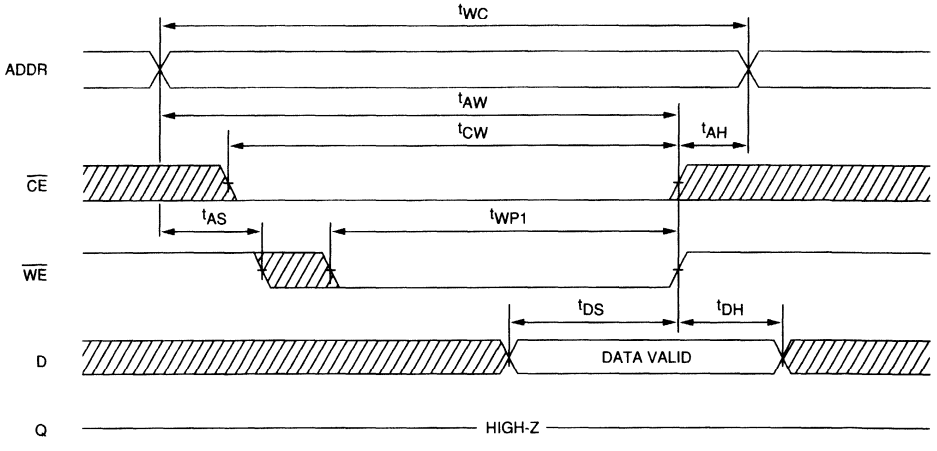
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

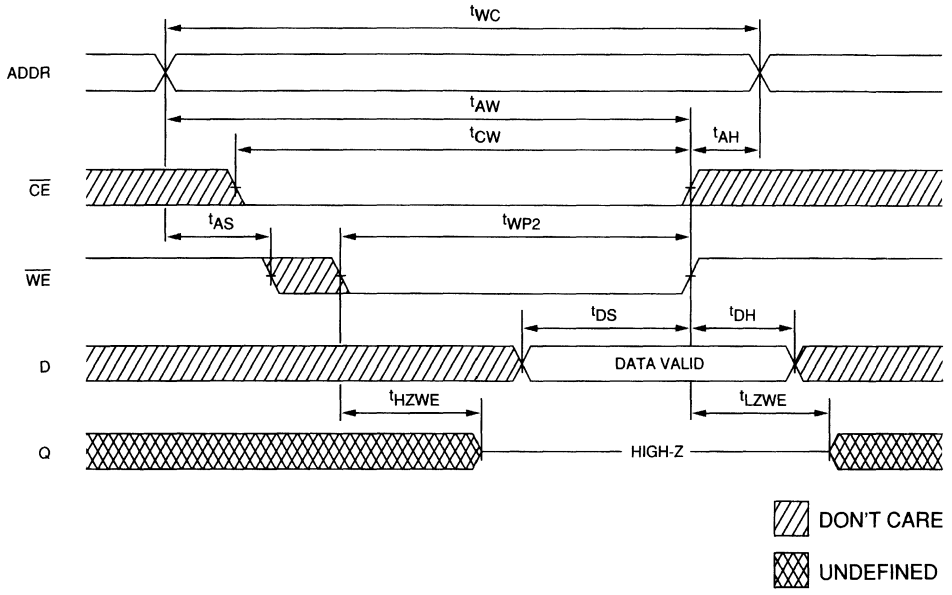


WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

64K x 32 SRAM

FEATURES

- High speed: 15*, 20, 25, 30 and 35ns
- High-performance, low-power CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile
- Industry standard pinout
- All inputs and outputs are TTL compatible
- Upgradable with 128K x 32 and 256K x 32 modules

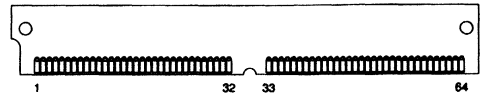
OPTIONS — MARKING

- Timing
  - 15ns access — -15*
  - 20ns access — -20
  - 25ns access — -25
  - 30ns access — -30
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention — L
- 2V data retention, low power — LP
- Part Number Example: MT8S6432Z-15 LP

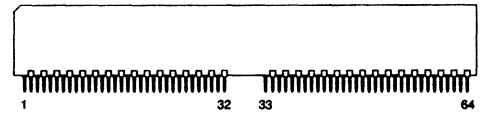
*Preliminary

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SG-2)



64-Pin ZIP
(SH-3)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8S6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

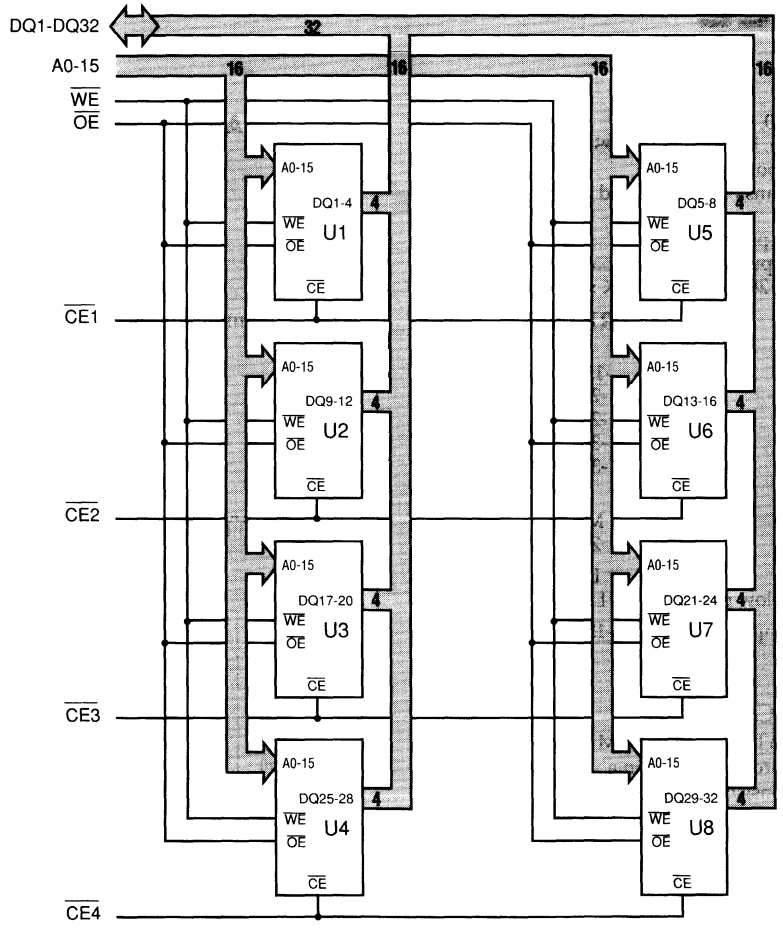
Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5C2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15*†	-20	-25	-30	-35	UNITS	NOTES
Operating Current TTL Input Levels	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	680	1,280	960	880	760	720	mA	3, 13
	"LP" VERSION	I_{CC}	520	-	880	800	720	640	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	88	320	240	200	200	200	mA	13
	"LP" VERSION	I_{SB1}	24	-	56	56	56	56	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	4.8	40	40	40	40	56	mA	13

*Preliminary
† LP version not available with this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A15, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz	C_I	70	pF	4
Input/Output Capacitance: DQ1-DQ32	Vcc = 5V	$C_{I/O}$	10	pF	4

SRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15*		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	15		20		25		30		35		ns	
Address access time	^tAA		15		20		25		30		35	ns	
Chip Enable access time	^tACE		15		20		25		30		35	ns	
Output hold from address change	^tOH	3		3		5		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	4		4		6		6		6		ns	7
Chip Enable to output in High-Z	^tHZCE		8		9		9		12		15	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		15		20		25		30		35	ns	
Output Enable access time	^tAOE		8		8		8		10		12	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		6		7		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	15		20		20		25		30		ns	
Chip Enable to end of write	^tCW	10		15		15		18		20		ns	
Address valid to end of write	^tAW	10		15		15		18		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	10		15		15		18		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		18		20		ns	
Data setup time	^tDS	7		10		10		12		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	4		5		5		5		5		ns	7
Write Enable HIGH to output in High-Z	^tHZWE	0	7	0	10	0	10	0	12	0	15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

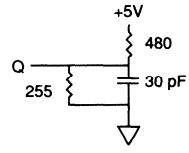


Fig. 1 OUTPUT LOAD EQUIVALENT

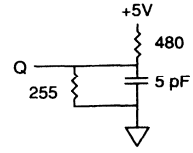


Fig. 2 OUTPUT LOAD EQUIVALENT

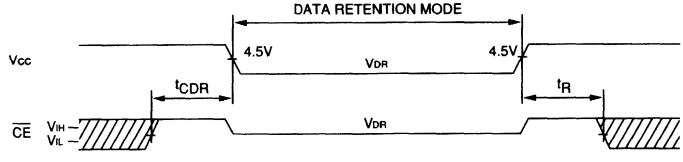
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		280	2,400	µA	
		Vcc = 3V			720	4,000	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

LOW Vcc DATA-RETENTION WAVEFORM

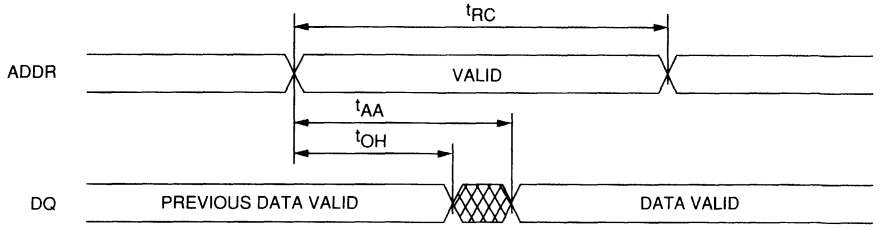


DON'T CARE

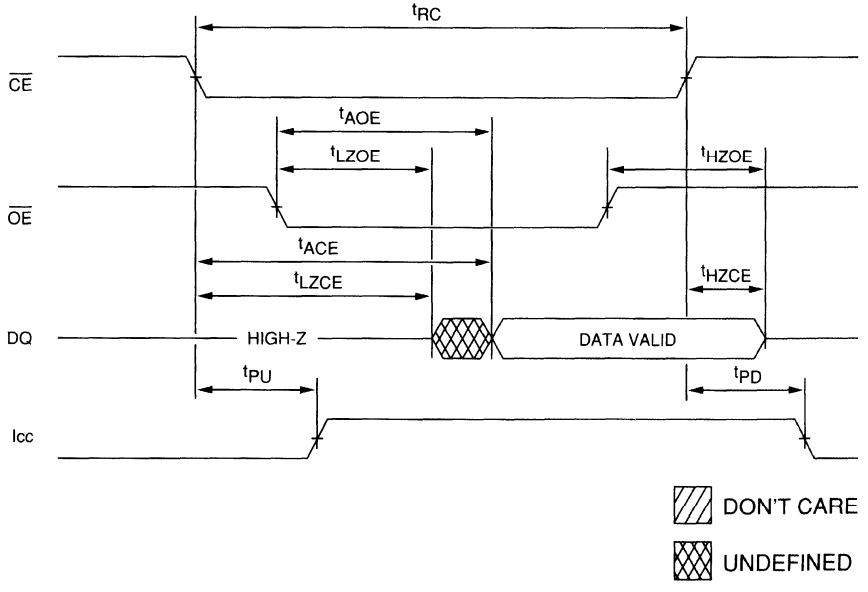
UNDEFINED

SRAM MODULE

READ CYCLE NO. 1 [8, 9]

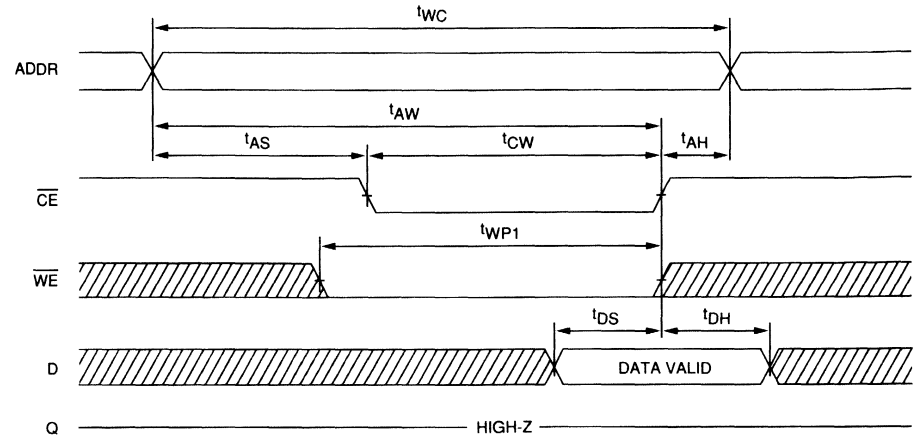


READ CYCLE NO. 2 [7, 8, 10]

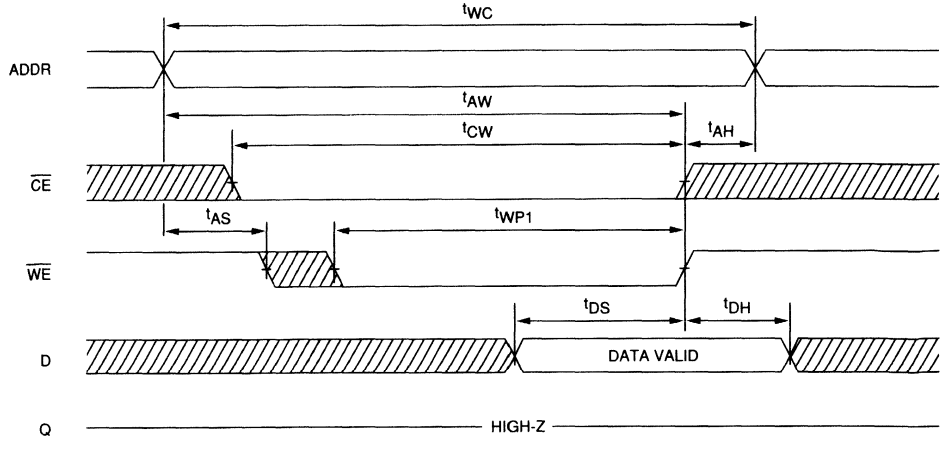


SRAM MODULE

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)

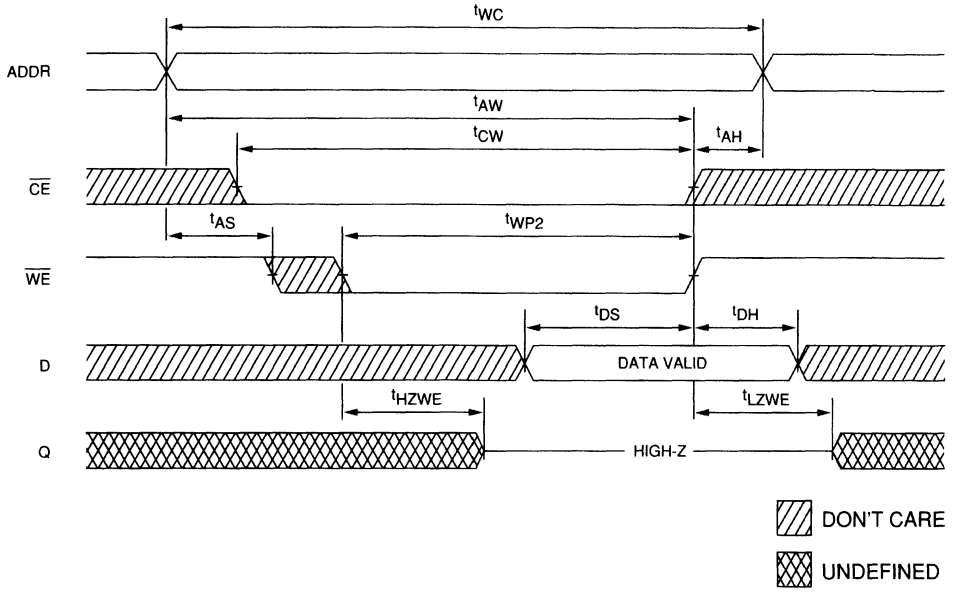


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

128K x 32 SRAM

FEATURES

- High speed: 15*, 20, 25 and 35ns
- High-density 512KB design
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL compatible
- Industry standard pinout
- Low profile
- Upgradable to a 256K x 32 module

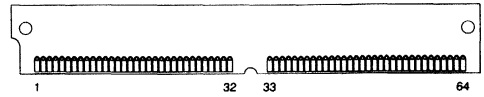
OPTIONS — MARKING

- Timing
  - 15ns access — -15*
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- Optional, 2V data retention — L
- 2V data retention, low power — LP
- Part Number Example: MT4S12832M-15 LP

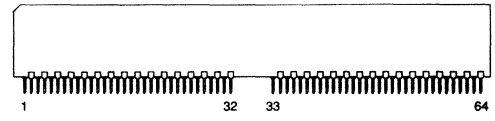
*Preliminary

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SG-3)



64-Pin ZIP
(SH-4)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT4S12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four 128K x 8 fast static RAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

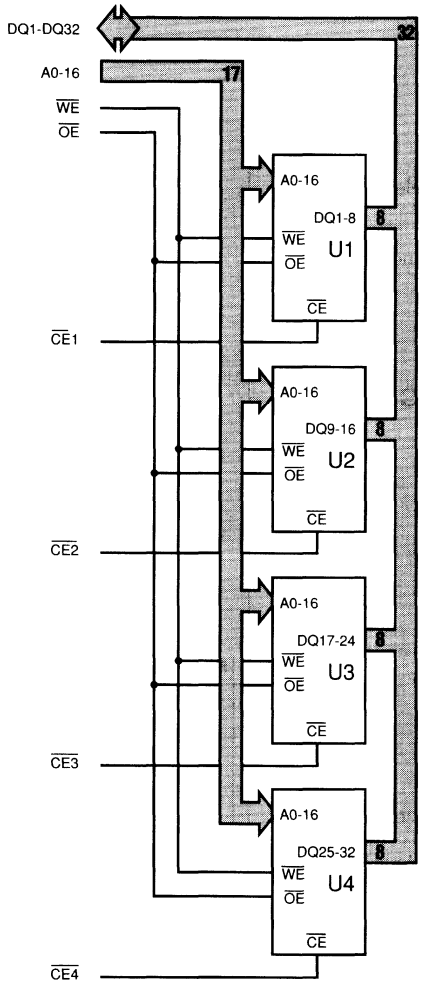
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL compatible.

The "L" and "LP" versions each provide a 70% reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C1008DJ

PRESENCE DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-20	20	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15*	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	380	760	620	500	460	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	68	180	160	120	100	mA	13
	"L" Version Only	I_{SB1}	5.2	12	12	12	12	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IL} ≤ Vss +0.2V V_{IH} ≥ Vcc -0.2V; f = 0	I_{SB2}	1.6	20	20	20	20	mA	13
	"L" and "LP" Versions Only	I_{SB2}	1.2	6	6	6	6	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A16, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_I	35	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15*		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	tRC	15		20		25		35		ns	
Address access time	tAA		15		20		25		35	ns	
Chip Enable access time	tACE		15		20		25		35	ns	
Output hold from address change	tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	tHZCE		6		8		10		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		ns	
Chip disable to power-down time	tPD		15		20		25		35	ns	
Output Enable access time	tAOE		5		6		8		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		5		6		10		12	ns	6
WRITE Cycle											
WRITE cycle time	tWC	15		20		25		35		ns	
Chip Enable to end of write	tCW	10		12		15		20		ns	
Address valid to end of write	tAW	10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		ns	
WRITE pulse width	tWP1	9		12		15		20		ns	
WRITE pulse width	tWP2	12		15		15		20		ns	
Data setup time	tDS	7		8		10		15		ns	
Data hold time	tDH	0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	tHZWE		6		8		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

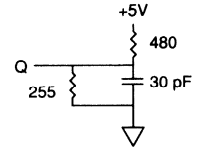


Fig. 1 OUTPUT LOAD EQUIVALENT

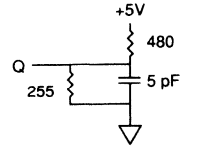


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

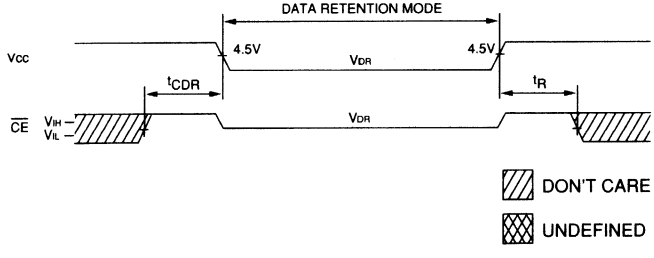
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		140	600	µA	
		Vcc = 3V			240	1,000	µA	
		Vcc = 3V*			120	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

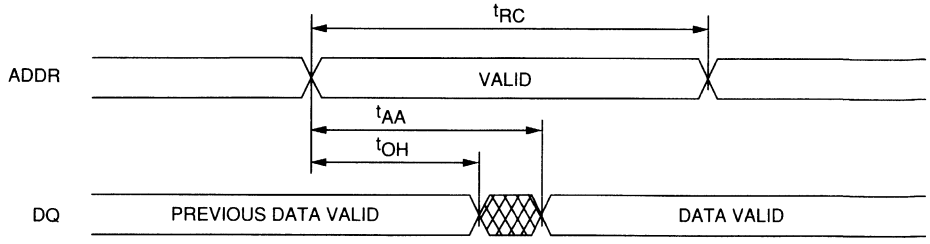
*Preliminary

LOW Vcc DATA-RETENTION WAVEFORM

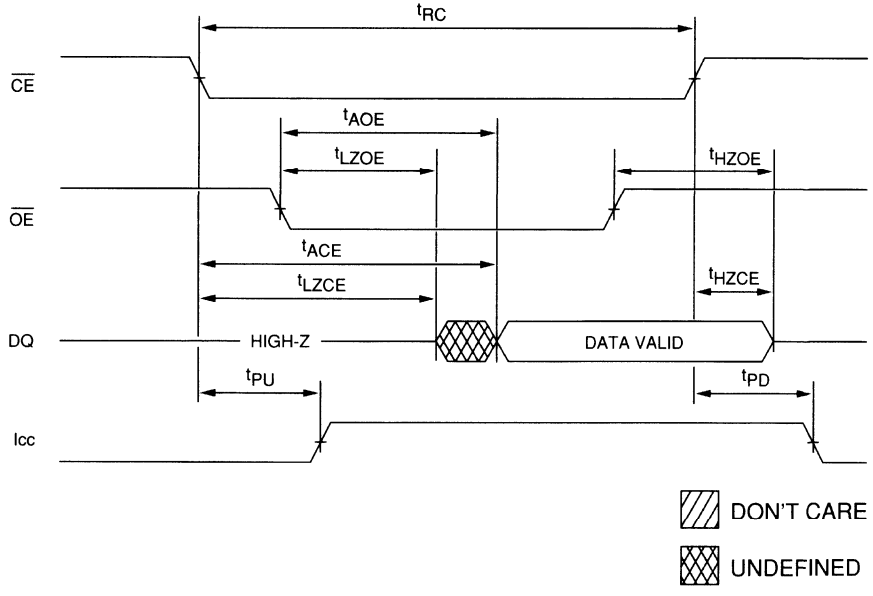


SRAM MODULE

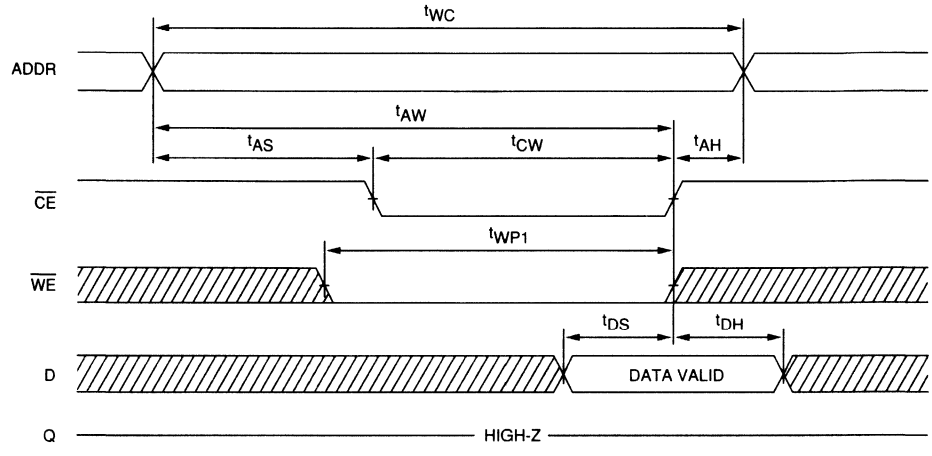
READ CYCLE NO. 1 [8, 9]



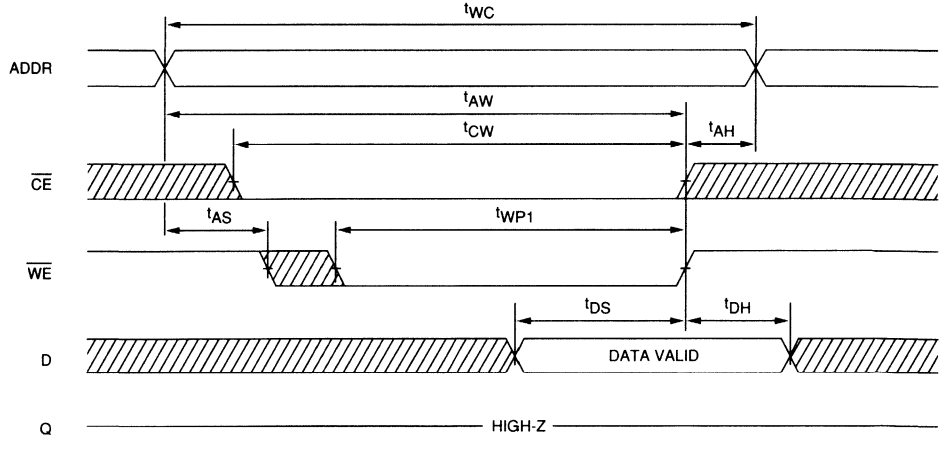
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



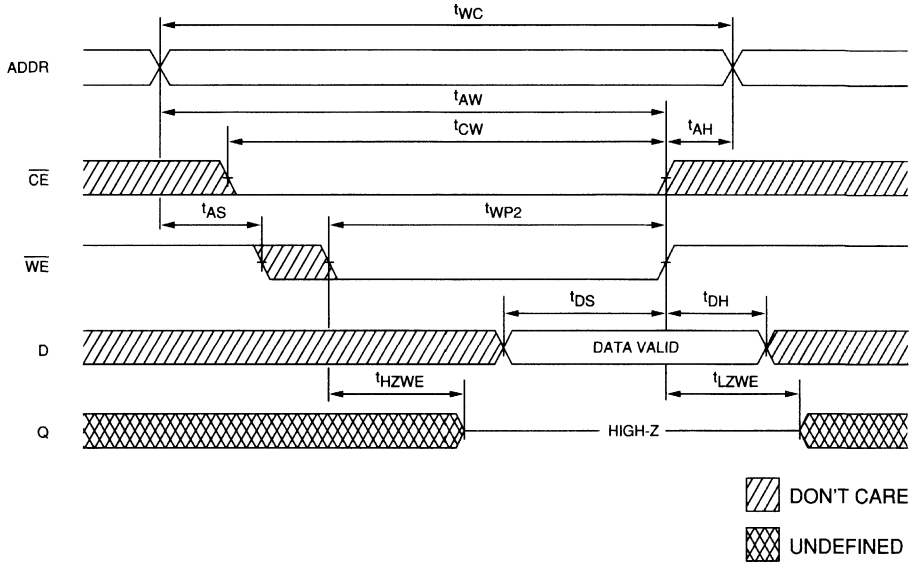
WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

SRAM MODULE

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

256K x 32 SRAM

FEATURES

- High speed: 15*, 20, 25 and 35ns
- High-density 1MB design
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Industry standard pinout
- All inputs and outputs are TTL compatible
- Low profile

OPTIONS MARKING

- Timing
  - 15ns access -15*
  - 20ns access -20
  - 25ns access -25
  - 35ns access -35
- Packages
  - 64-pin SIMM M
  - 64-pin ZIP Z
- Optional, 2V data retention L
  - 2V data retention, low power LP
- Part Number Example: MT8S25632Z-15 L

*Preliminary

GENERAL DESCRIPTION

The MT8S25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight 256K x 4 fast static RAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

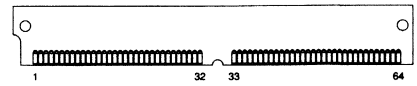
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

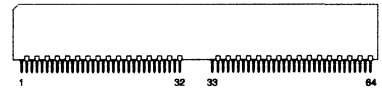
The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SG-4)



64-Pin ZIP
(SH-1)

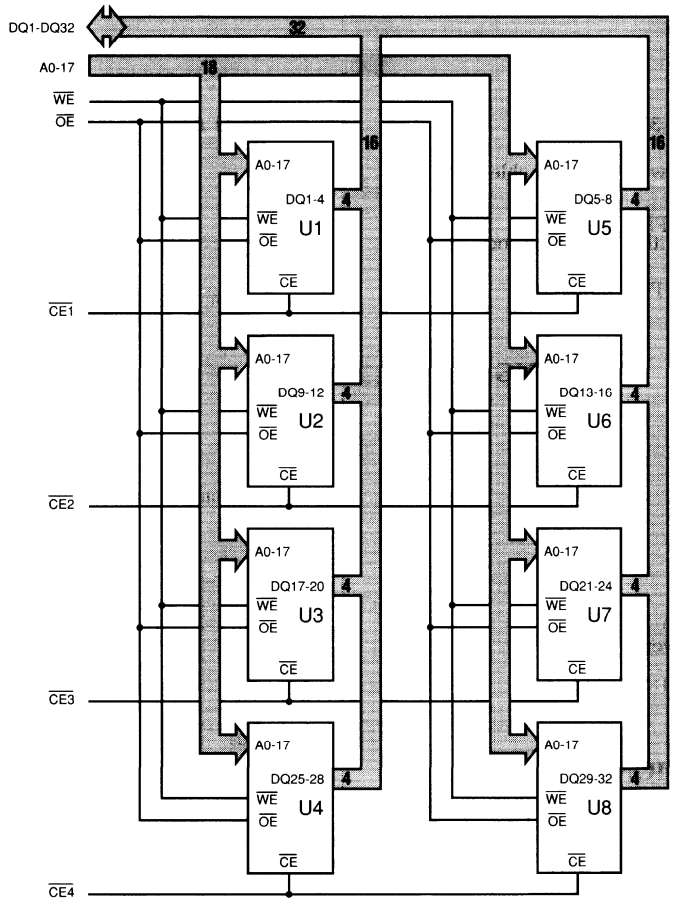


PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL compatible.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = Vss
PD1 = Vss

U1-U8 = MT5C1005DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-40	40	µA	
Input/Output Leakage Current	Output(s) Disabled DQ1-DQ32, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -15*	MAX -20	MAX -25	MAX -35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX, f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	760	1,520	1,240	1,000	920	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX, f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	136	360	320	240	200	mA	13
	"LP" Version Only	I_{SB1}	10.4	24	24	24	24	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX, V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	3.2	40	40	40	40	mA	13
	"L" and "LP" Versions Only	I_{SB2}	2.4	12	12	12	12	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance; A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz, V_{CC} = 5V	C_{I1}	70	pF	4
Input Capacitance; $\overline{CE1}$-$\overline{CE4}$		C_{I2}	18	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

SRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15*		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	tRC	15		20		25		35		ns	
Address access time	tAA		15		20		25		35	ns	
Chip Enable access time	tACE		15		20		25		35	ns	
Output hold from address change	tOH	3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	tHZCE		6		8		10		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		ns	
Chip disable to power-down time	tPD		15		20		25		35	ns	
Output Enable access time	tAOE		5		6		8		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		5		6		10		12	ns	6
WRITE Cycle											
WRITE cycle time	tWC	15		20		25		35		ns	
Chip Enable to end of write	tCW	10		12		15		20		ns	
Address valid to end of write	tAW	10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		ns	
WRITE pulse width	tWP1	9		12		15		20		ns	
WRITE pulse width	tWP2	12		15		15		20		ns	
Data setup time	tDS	7		8		10		15		ns	
Data hold time	tDH	0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	tHZWE		6		8		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

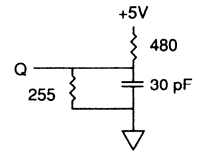


Fig. 1 OUTPUT LOAD EQUIVALENT

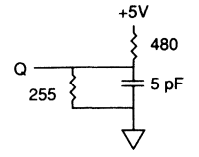


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

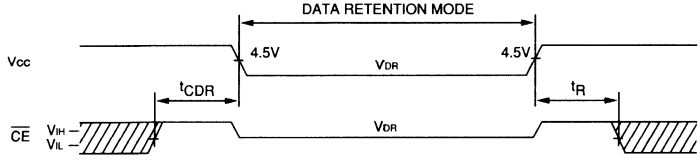
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		280	1,200	µA	
		Vcc = 3V			480	3,200	µA	
		Vcc = 3V*			240	800	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

*Preliminary

LOW Vcc DATA-RETENTION WAVEFORM

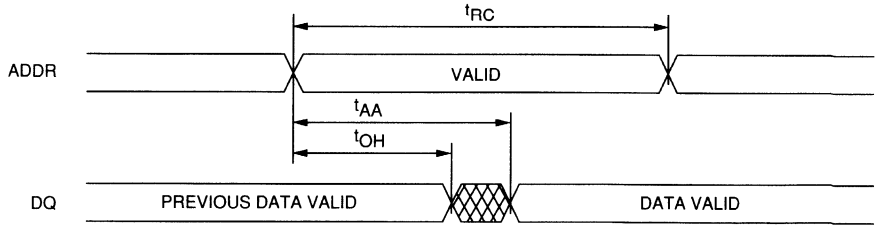


DON'T CARE

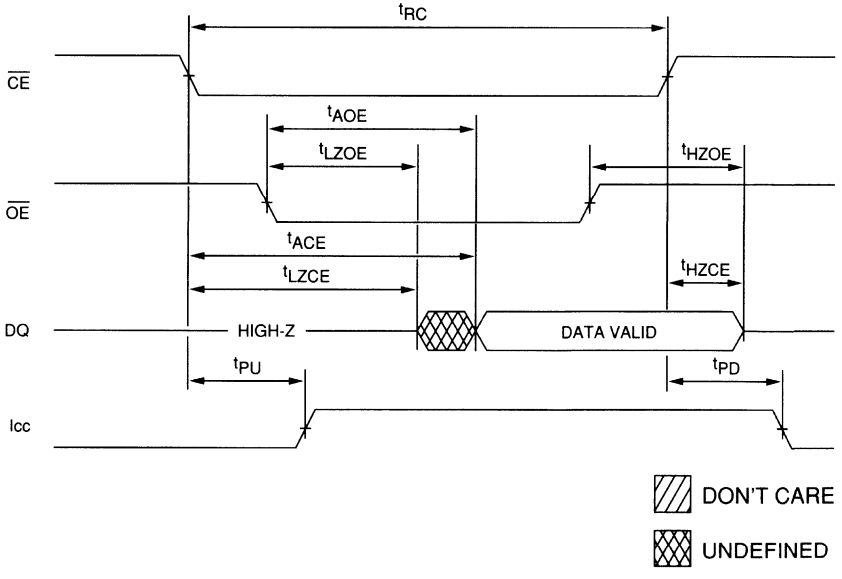
UNDEFINED

SRAM MODULE

READ CYCLE NO. 1 [8, 9]

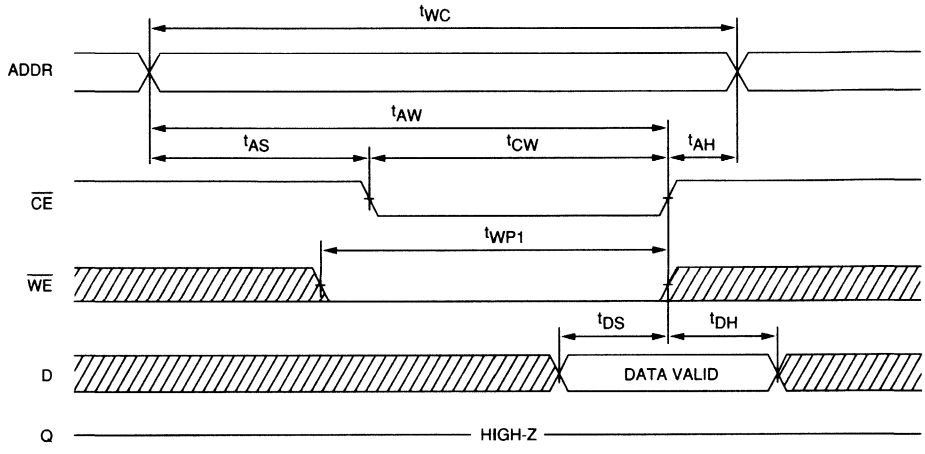


READ CYCLE NO. 2 [7, 8, 10]

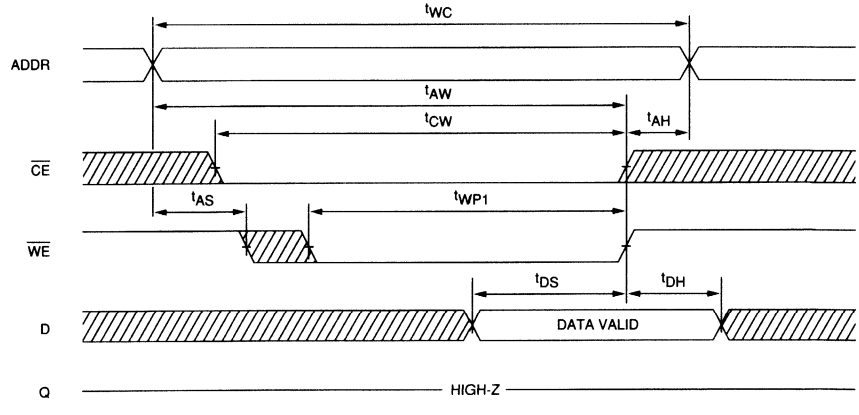


SRAM MODULE

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

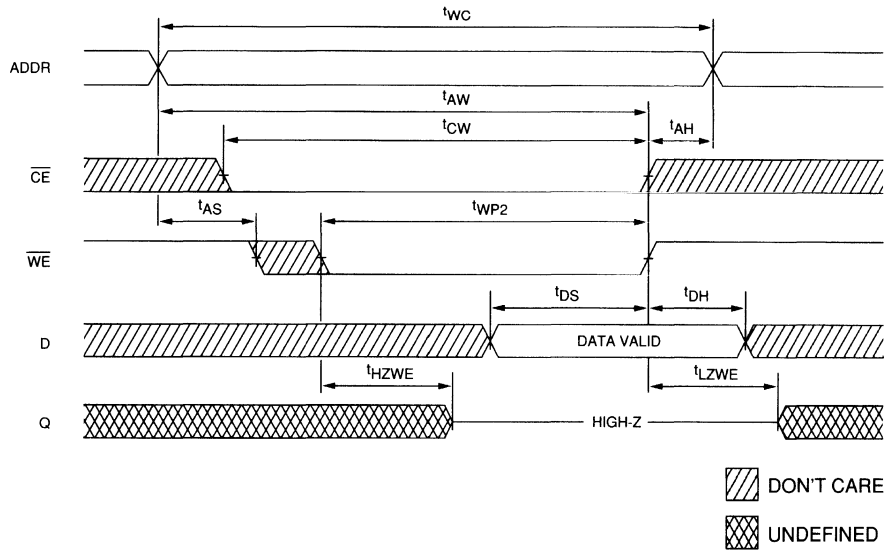


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON

APPLICATION/TECHNICAL NOTE SELECTION GUIDE

TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated circuit packages have a tendency to absorb moisture. During surface mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die, and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks, that might not be harmful initially, could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn failures with surface-mount packages by shipping all surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high humidity environment for long time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K. : et. al. : 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et. al. : 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et. al. : 26th Annual Proceeding, Reliability Physics, 1988.

TECHNICAL NOTE

TAPE AND REEL PROCEDURES

GENERAL DESCRIPTION

Tape and reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape and reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape and reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1*
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
52 Pin	32	16	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500

*These are examples of tape and reel sizes available. Please contact Micron for all available options.

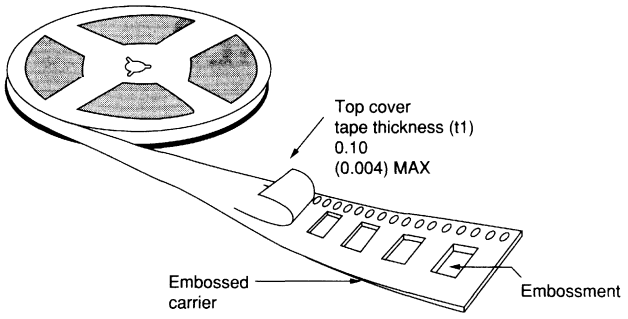


Figure 1
REEL

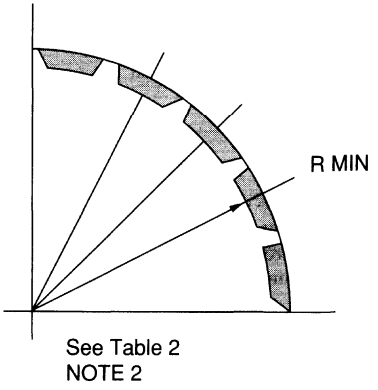
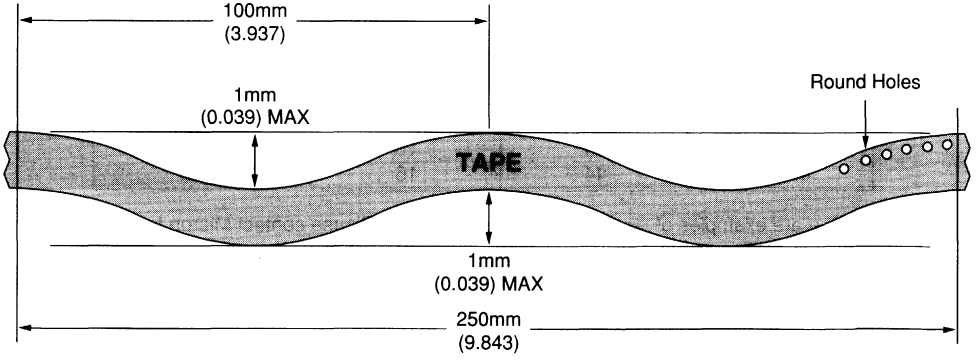


Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER (TOP VIEW)

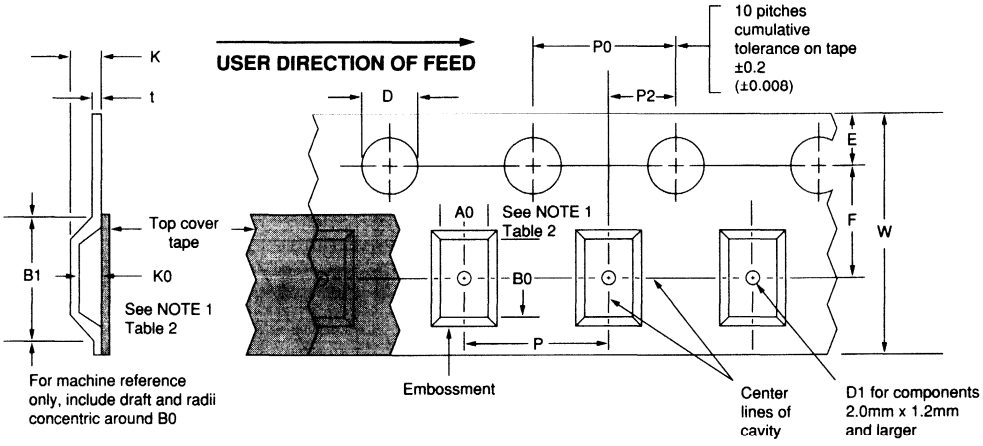


Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm Tape Only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS[3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	NOTE 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

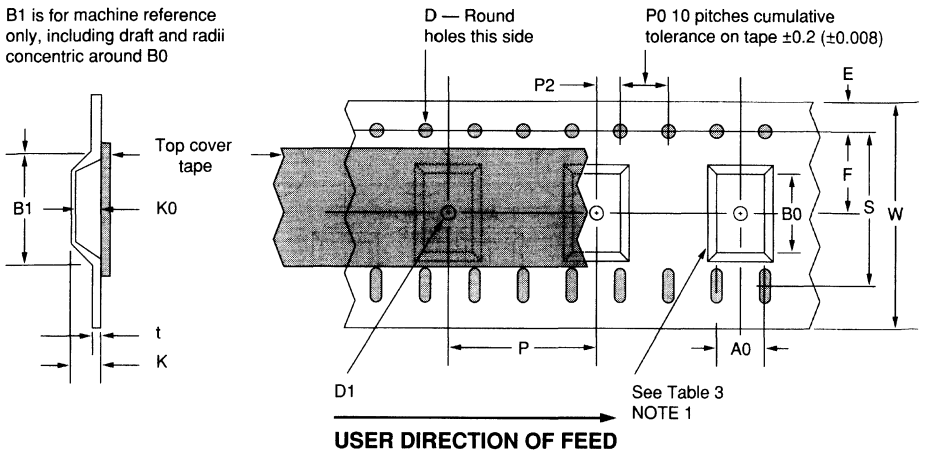


Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm Tape Only)

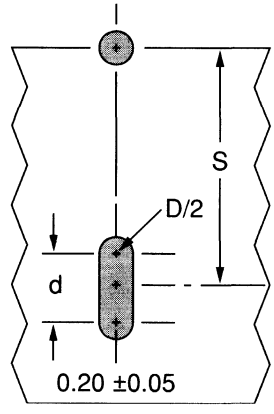


Figure 6
DETAIL ELONGATED HOLE

APPLICATION/TECHNICAL NOTE

Table 3
32 AND 44mm EMBOSSED TAPE [3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	1.5 $^{+0.10}_{+0.00}$ (0.059) $^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

TECHNICAL NOTE

SRAM BUS CONTENTION DESIGN CONSIDERATIONS

INTRODUCTION

High-speed SRAM memory systems normally share a common data bus with other memory devices, processors and memory management or caching devices. All of these devices are required to control data bus at one time or another. Turning off a device that is driving the bus before a new device takes control of the bus can be a difficult design problem when these systems are operating at minimum cycle times.

When two or more devices are driving the bus at the same time, a conflict known as "bus contention" occurs. This technical note discusses bus contention design issues and points out features in the design of Micron's fast SRAMs to help minimize bus contention problems.

BUS CONTENTION EFFECTS

System-design problems caused by bus contention are difficult to analyze. The effects are transient, normally not longer than 5ns. The most visible result of bus contention is observed as noise on power-supply lines and data lines connecting the contending devices. While these conflicts are not destructive, they potentially reduce long-term system reliability. However, in most cases, they do not affect system performance when all the active components are MOS.

MOS devices are inherently self-current limiting. As the current through a MOS transistor increases, the transistor heats up and its gain decreases. Bipolar transistors have the opposite behavior. When a bipolar transistor's temperature

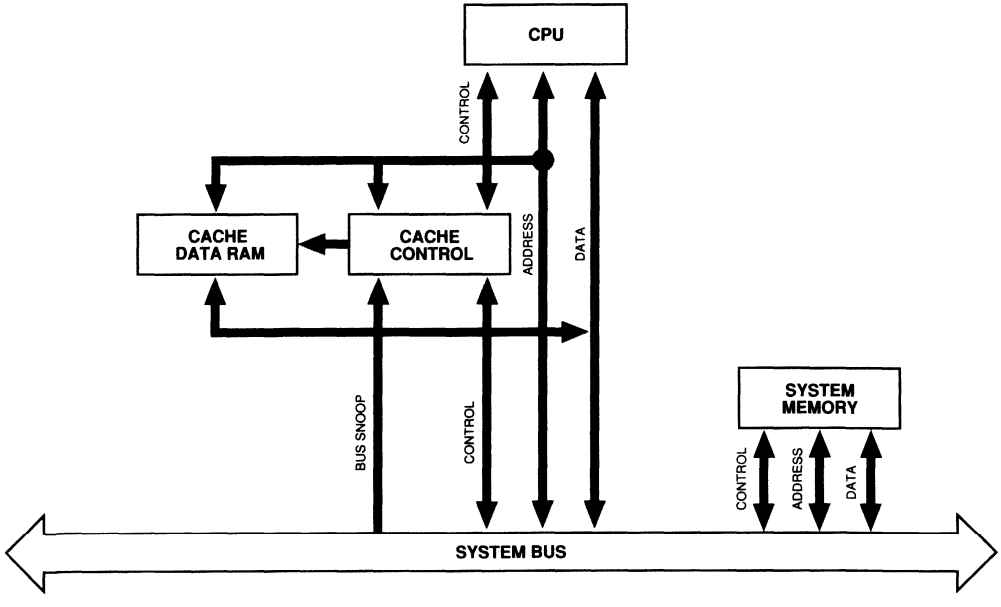


Figure 1
BLOCK DIAGRAM OF A CACHE MEMORY SYSTEM

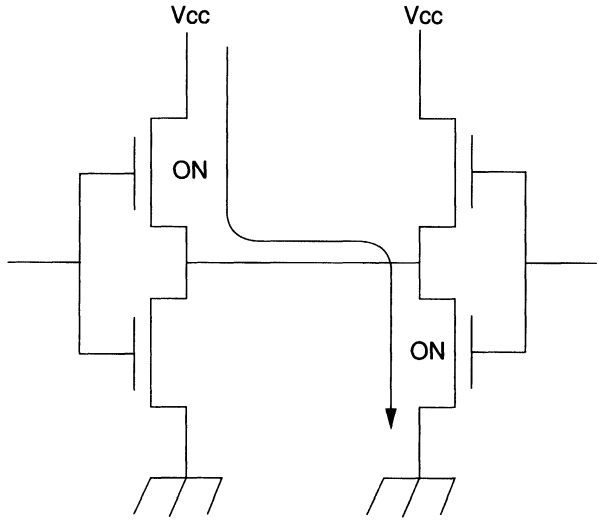


Figure 2
BUS CONTENTION CURRENT PATH

is elevated, the gain of the device increases, making it possible for the current through the transistor to increase to a destructive level. This phenomenon is known as "thermal runaway." If CMOS SRAMs share any data lines with bipolar or BiCMOS output devices, the system should be designed to eliminate any possibility of bus contention.

Figure 2 is a schematic diagram of two contending SRAM output buffers. A high current path has been created by two SRAM output buffers. The current is flowing between the "on" transistor connected to Vcc in the buffer on the left and the transistor connected to ground in the buffer on the right.

SRAM SPECIFICATIONS

The critical parameter for calculating the amount of bus contention for a high-speed SRAM system design is the time it takes for a device to go to low impedance (logic 1 or 0) on its output versus the time required for a contending output to go to high impedance. A typical SRAM has three control signals: chip enable (CE), write enable (WE) and output enable (OE). ^{t}LZCE, ^{t}LZWE and ^{t}LZOE are the times it takes for the outputs to become active or low impedance upon the assertion of CE, WE and OE. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are the times required for the outputs to become inactive or high impedance after CE, WE and OE are removed. These times are shown in the READ and WRITE cycle timing diagram (Figure 3). A preliminary review of a fast SRAM data sheet would imply that the worst case for bus contention could be calculated from the equation:

$$^{t}C = {}^{t}HZ\ (MAX) - {}^{t}LZ\ (MIN)$$

where ^{t}C is equal to the bus-contention overlap time. For an output enable change in an SRAM rated at 20ns access time, ^{t}HZ = 7ns and ^{t}LZ = 2ns; therefore ^{t}C = 5ns. If this calculation is correct, there would be a serious bus contention problem. Thus, for a system running with a 20ns cycle, almost 25 percent of the total cycle would be lost to bus contention and there would be a large increase in power dissipation in the output buffers.

Fortunately, the previous analysis is not valid because ^{t}HZ maximum occurs under completely different test conditions than ^{t}LZ minimum. ^{t}HZ maximum is worst-case at the highest operating temperature and the lowest power-supply voltage. On a commercial data sheet, this would be at 70° C and 4.5V. ^{t}LZ minimum is specified at the lowest

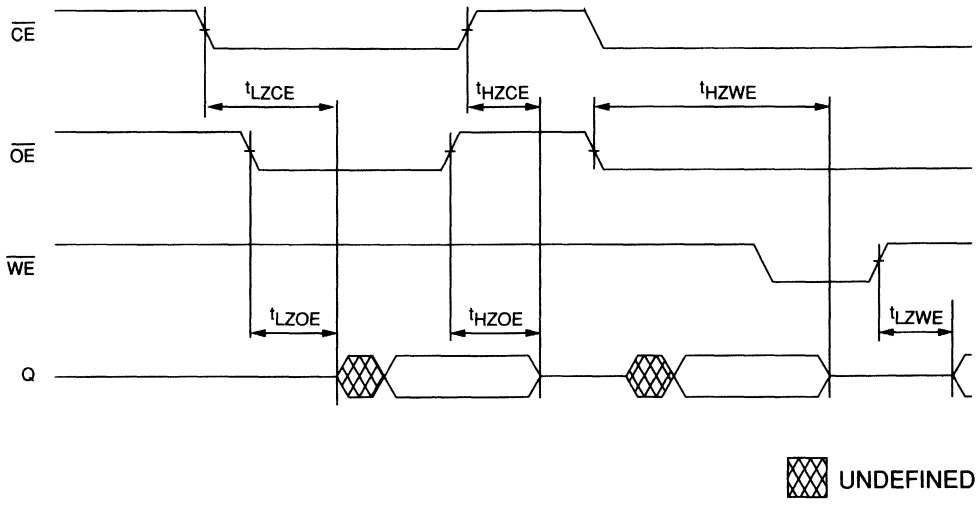


Figure 3
READ AND WRITE CYCLE TIMING

operating temperature and the highest voltage. Again, on the commercial data sheet, this would be 0° C and 5.5V. It is not possible for two SRAMs on the same board to be at such diverse temperatures and voltages. In a "real world" system — that is, one with an equal operating environment for temperature and power supply voltage — ^{t}HZ - ^{t}LZ is approximately 0.2ns.

Futhermore, Micron fast SRAMs have been designed to insure the outputs always turn off faster than they turn on when operating at the same voltage and temperature: ^{t}HZ < ^{t}LZ. Since the devices will normally be mounted on the same board, the bus contention associated with the SRAM control signals has been minimized.

Care must be taken when multiple vendors' SRAMs share the bus. An analysis of the output turn-off time must be done under the same operating and temperature conditions to insure that bus contention between the devices is minimized.

TECHNICAL NOTE

SRAM CAPACITIVE LOADING

INTRODUCTION

Many high-speed 16-bit and 32-bit microprocessor systems require fast SRAMs. SRAMs are used either in main memory or caching subsystems. In either case, the SRAMs are typically required to interface with a system bus that is shared by one or more microprocessors, several I/O devices and other types of memory (ROM, EPROM, etc.).

Even though transceivers and/or buffers interface with the actual bus, SRAMs are typically required to drive loads larger than what is specified in the data sheet timing parameters. Hence, the access time must be derated to reflect the actual performance of the SRAM under these circumstances.

SIMILARITY BETWEEN SRAM FAMILIES

Micron's 16K, 64K, 256K and 1 Meg SRAM families all have the same size output transistors and output architecture. Hence, all devices will have the same drive characteristics. The actual data presented in this technical note are derived from the 256K SRAM family.

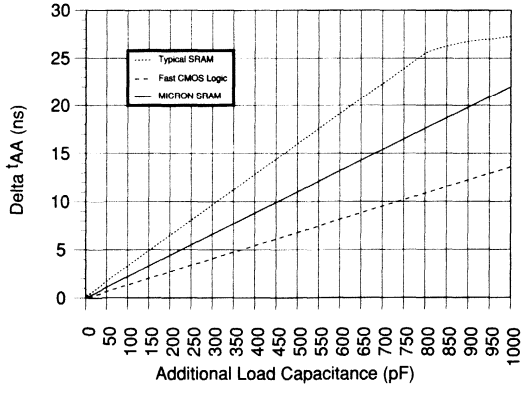


Figure 1
INCREASED ACCESS TIME vs. ADDITIONAL OUTPUT LOADING

COMPARISON OF DEVICES

Figure 1 compares the effects of capacitive loading on the Micron SRAM family with SRAMs from a typical memory supplier and discrete CMOS logic, designed to drive heavy loads. The graph illustrates the additional access time required to drive various capacitive loads.

As expected, the Micron SRAM family does not drive heavy loads as well as the discrete CMOS logic, but does drive faster than the typical SRAM from other suppliers.

The graph line representing the Micron SRAM family is based on data gathered on the Micron 256K SRAM. Access time measurements were taken with the SRAM subjected to various capacitive loads. In the range covered, the change in access time was seen to be a linear function of the capacitive load. The following equation may be used to determine the access time required for a specific load.

$$T_{AA}(\text{actual}) = T_{AA}(\text{data sheet}) + T_{AA}(\text{additional})$$

$$T_{AA}(\text{additional})\ (\text{ns}) = .022\ (\text{ns/pF})\ C_a$$

This applies where C_a is the additional capacitive load expressed in picofarads (pF). For example, the access time needed for a 100pF total capacitive load is:

T_{AA}(actual) = 20ns + T_{AA}(additional) =
20ns + .022 * (total load - rated load) =
20ns + .022ns/pF * (100pF - 30pF) =
20ns + 1.5ns = 21.5ns

SUMMARY

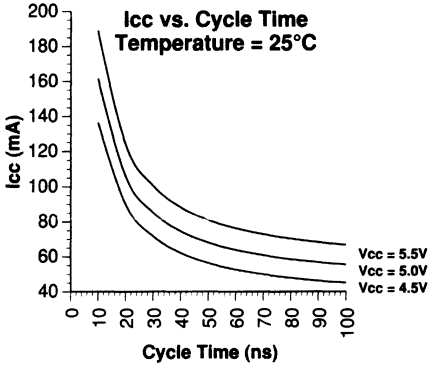
The SRAM timing specifications of all major vendors are based upon an industry standard capacitive load of 30pF. In most applications, the SRAMs are required to drive much larger capacitive loads. In addition, today's designs are implemented around higher frequencies. This requires the system timing to be more precise; hence, loading becomes a more important issue. Understanding how the SRAM will perform under specific loading conditions may result in a more reliable design.

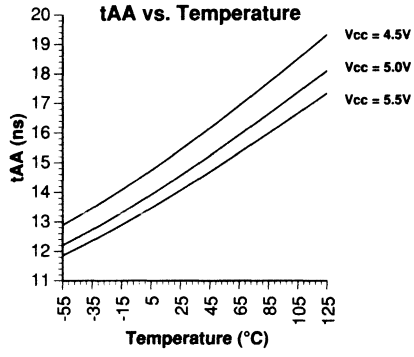
TECHNICAL NOTE

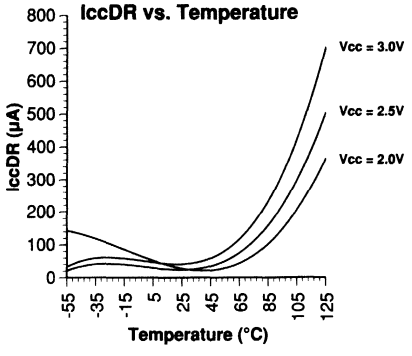
1 MEG FAST SRAM TYPICAL OPERATING CURVES

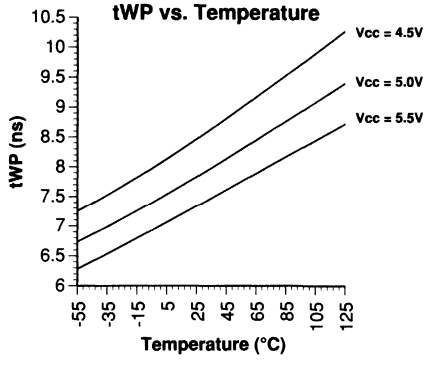
INTRODUCTION

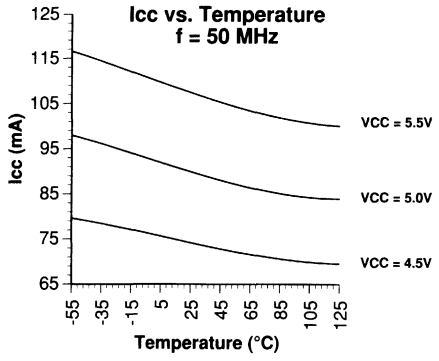
These curves represent the typical operating characteristics of Micron's 1 Meg, 20ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

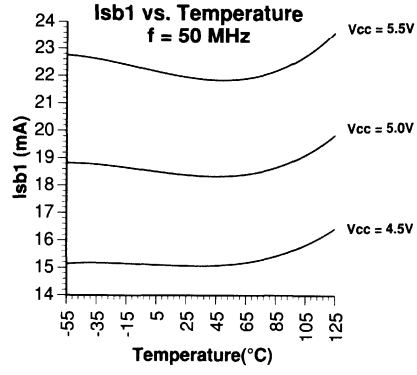


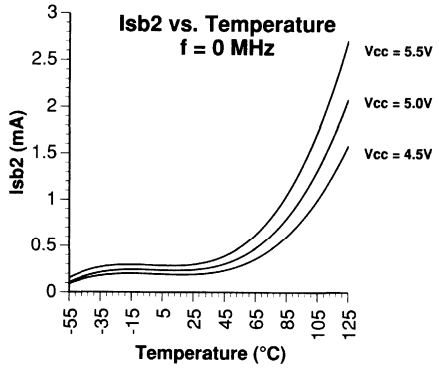












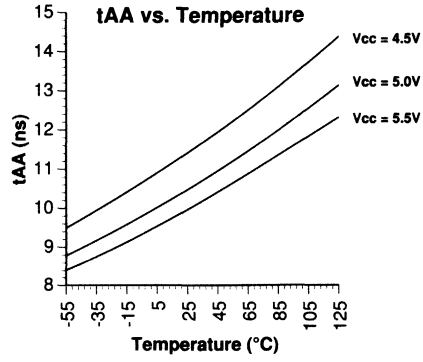
APPLICATION/TECHNICAL NOTE

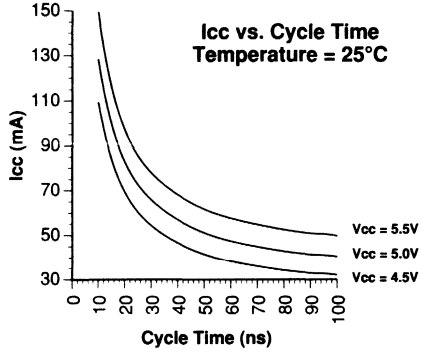
TECHNICAL NOTE

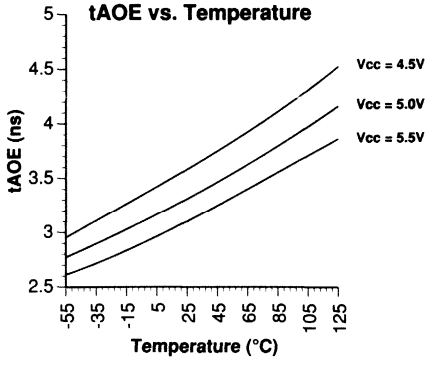
256K FAST SRAM TYPICAL OPERATING CURVES

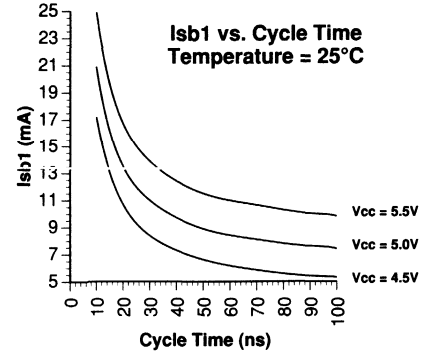
INTRODUCTION

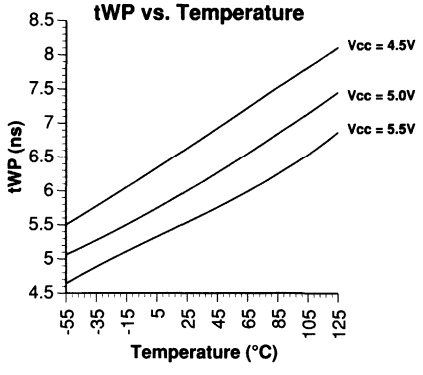
These curves represent the typical operating characteristics of Micron's 256K, 15ns SRAM and 20ns low power (LP) SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

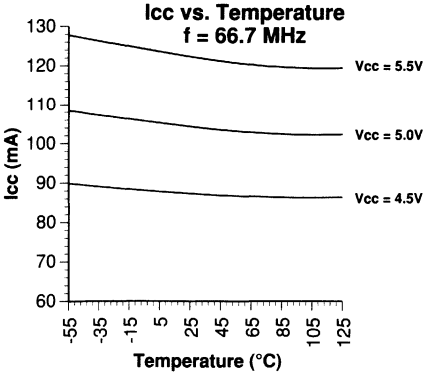


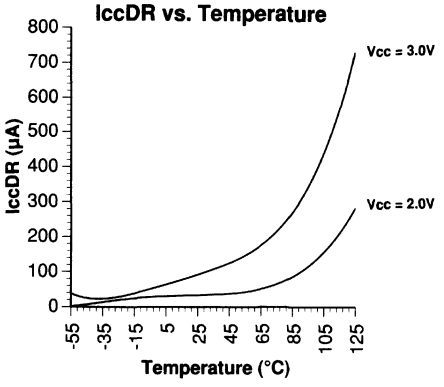


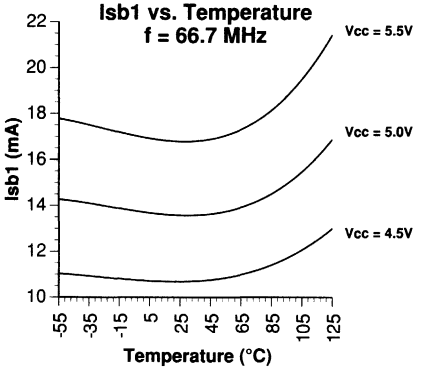


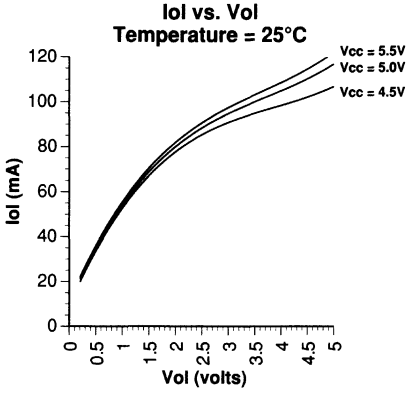


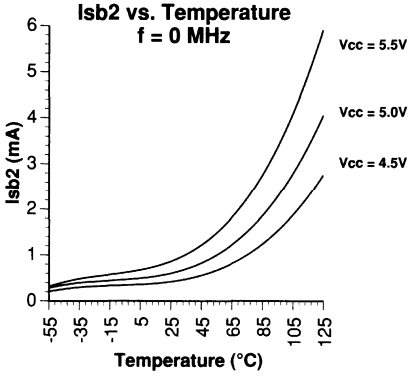


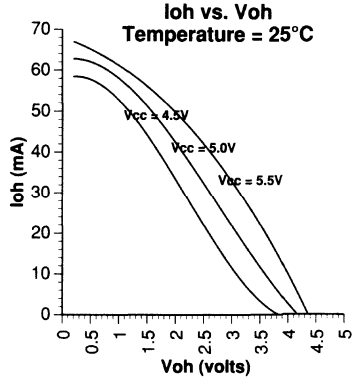




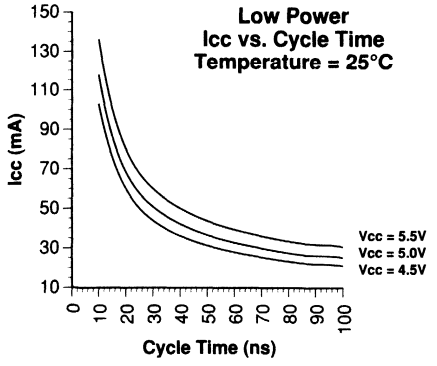


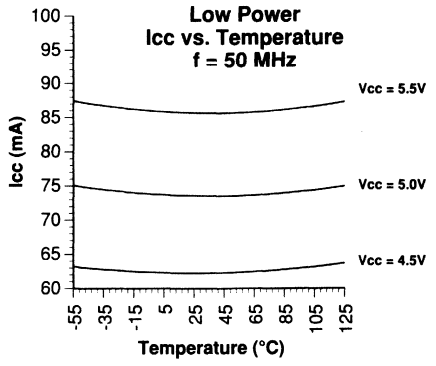


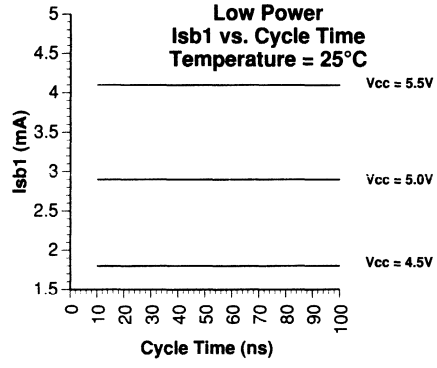


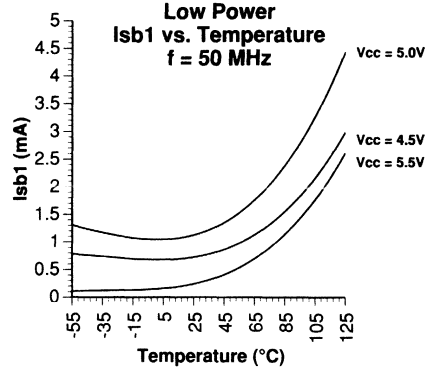


APPLICATION/TECHNICAL NOTE









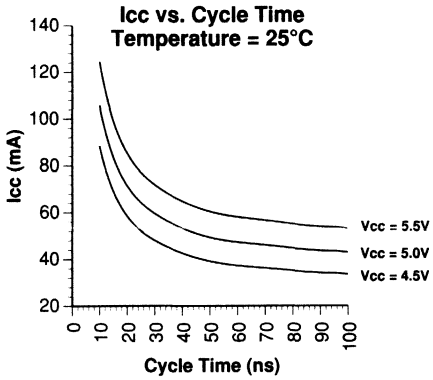
APPLICATION/TECHNICAL NOTE

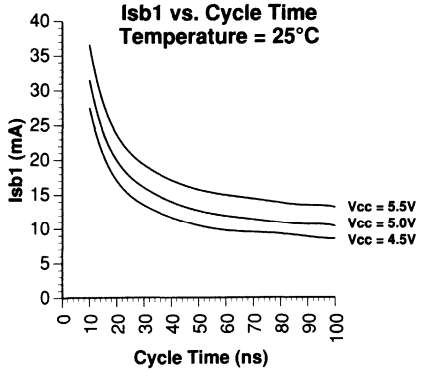
TECHNICAL NOTE

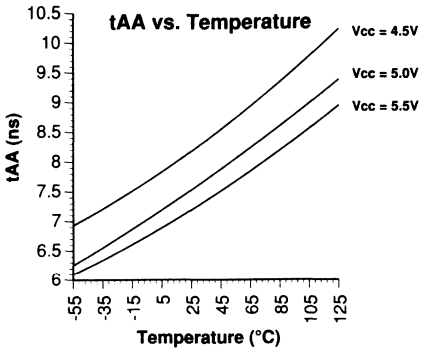
64K FAST SRAM TYPICAL OPERATING CURVES

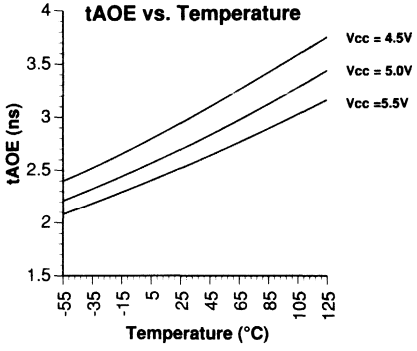
INTRODUCTION

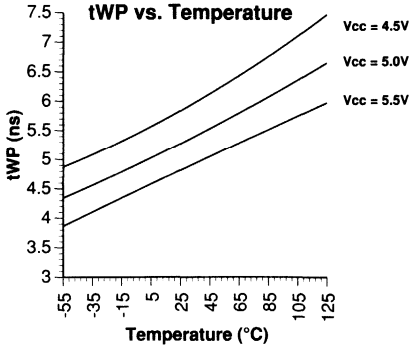
These curves represent the typical operating characteristics of Micron's 64K, 10ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

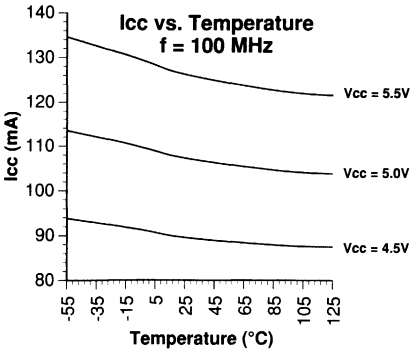


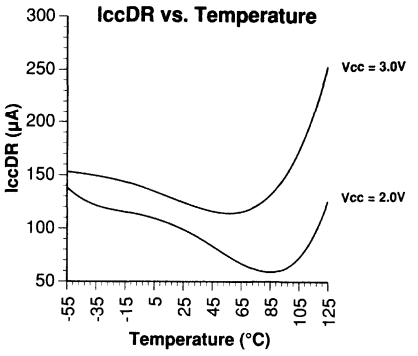


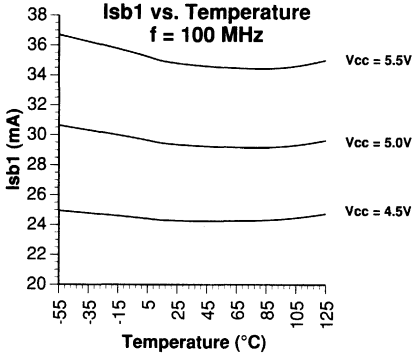


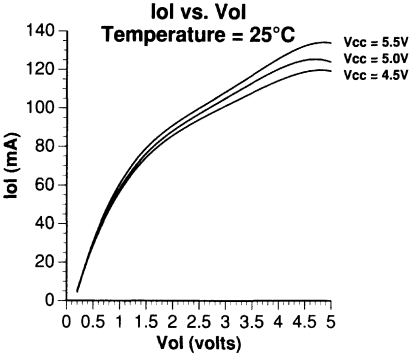


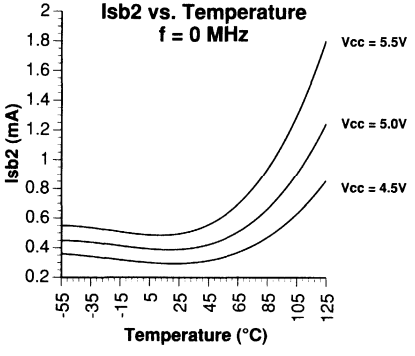


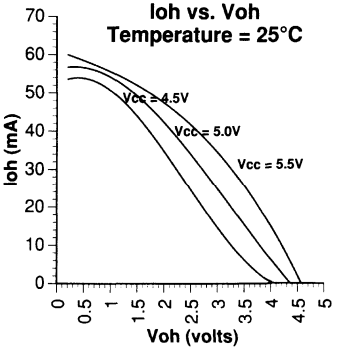












TECHNICAL NOTE

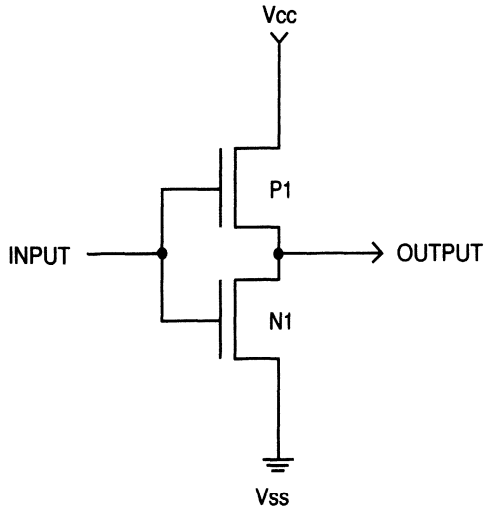
1 MEG LOW-POWER SRAMS

INTRODUCTION

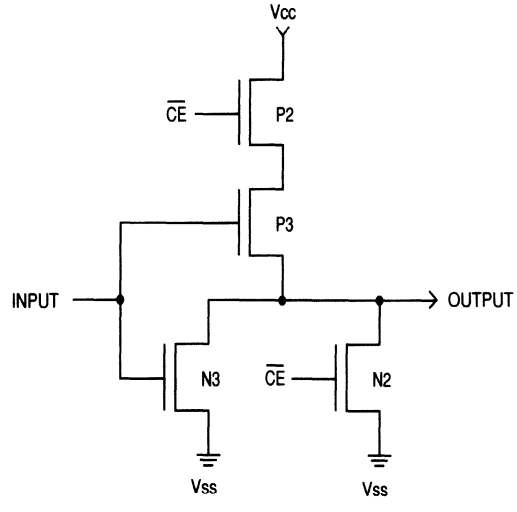
By using the low-power versions of the Micron 1 Meg SRAM family (MT5C100X LP), designers can reduce both operating power consumption and battery back-up power consumption in their systems. This technical note describes the physical differences between the low-power versions and the standard versions of the 1 Meg SRAM and how these differences affect the various current consumption specifications for the devices. The note then discusses the system-level benefits of low-power parts.

LOW-POWER vs STANDARD VERSIONS

The primary difference between the low-power versions and the standard versions of the 1 Meg SRAM is that the low-power versions contain gated inputs on the write enable ($\overline{WE}$), output enable ($\overline{OE}$) and address inputs. The difference between gated and non-gated inputs is shown in Figure 1. In the non-gated input buffer, current will flow from Vcc to Vss when both transistors are conducting (i.e. when the input is switching or is sitting at a level between Vcc and Vss). Current flow is at a minimum when the input is held at either the Vcc or Vss level. In the gated input buffer, $\overline{CE}$ is an internal chip enable signal derived from the chip enable pin(s) of the device. When the chip is selected, $\overline{CE}$ is LOW, P2 is ON and N2 is OFF. Operation in this mode is similar to the non-gated input buffer. When the chip is deselected, $\overline{CE}$ is HIGH, N2 is ON and P2 is OFF. In this case, both the logical operation of the buffer and the flow-through current are independent of the voltage level at the



NON-GATED INPUT BUFFER



GATED INPUT BUFFER

Figure 1
NON-GATED vs GATED INPUT BUFFERS

NEW APPLICATION/TECHNICAL NOTE

Table 1

OPERATING AND STANDBY CURRENT DEFINITIONS			
PARAMETER	**MODE**	**CHIP ENABLE INPUT CONDITIONS**	**WRITE ENABLE, OUTPUT ENABLE AND ADDRESS INPUT CONDITIONS**
I_{CC}	Chip Selected	$V_{IH} \geq 2.2V$; $V_{IL} \leq 0.8V$ switching at MAX frequency	$V_{IH} \geq 2.2V$; $V_{IL} \leq 0.8V$ switching at MAX frequency
I_{SB1} (Standard)	Chip Deselected	$V_{IH} \geq 2.2V$; $V_{IL} \leq 0.8V$ static	$V_{IH} \geq 2.2V$; $V_{IL} \leq 0.8V$ switching at MAX frequency
I_{SB1} (Low-Power)	Chip Deselected	$V_{IH} \geq 2.2V$; $V_{IL} \leq 0.8V$ static	$V_{SS} \leq V_{IN} \leq V_{CC}$ static or switching
I_{SB2} (Standard)	Chip Deselected	$V_{IH} \geq V_{CC} - 0.2V$; $V_{IL} \leq V_{SS} + 0.2V$ static	$V_{IH} \geq V_{CC} - 0.2V$; $V_{IL} \leq V_{SS} + 0.2V$ static
I_{SB2} (Low-Power)	Chip Deselected	$V_{IH} \geq V_{CC} - 0.2V$; $V_{IL} \leq V_{SS} + 0.2V$ static	$V_{SS} \leq V_{IN} \leq V_{CC}$ static or switching

input node. The output of the buffer is LOW because N2 is ON, and virtually no current flows from V_{CC} to V_{SS}, because the gate of P2 is held at the V_{CC} level.

Another difference from the standard versions found in the low-power versions is a process enhancement designed to reduce the current consumed by the memory cells under quiescent conditions. This means that the standby current attributed to the memory array is reduced.

Specifications are summarized in Table 1 to help illustrate the effects of these differences on the various current consumption specifications of the parts. The values for these parameters are shown in Table 2. Note that I_{SB1} and I_{SB2} are substantially reduced in the low-power version while I_{CC} remains the same. The I_{SB1} (MAX) limit is reduced by 90 percent, primarily through the use of gated inputs, and the I_{SB2} (MAX) limit is reduced by 70 percent due to the process enhancements. Icc is not affected by these changes because it is measured when the chip is selected and the memory array is being accessed.

Another way of looking at the effects of these changes on I_{SB1} and I_{SB2} for the low-power version is to note that the specified values for I_{SB1} approach the values for I_{SB2}. The remaining difference between the I_{SB1} and I_{SB2} values represents the amount of current consumed by the chip enable input buffers themselves. By definition, I_{SB1} is measured with the chip enable inputs at V_{IH} (MIN) or V_{IL} (MAX) levels. This causes more current to flow than if the inputs were within 0.2 volts of V_{CC} or V_{SS} levels, as is the case when measuring I_{SB2}.

Table 2

OPERATING AND STANDBY CURRENT SPECIFICATIONS						
DEVICE VERSION	**I_{CC}***		**I_{SB1}**		**I_{SB2}**	
	MAX	**TYP**	**MAX**	**TYP**	**MAX**	**TYP**
Standard	125 mA	95 mA	30 mA*	17 mA	5 mA	400 uA
Low-Power	125 mA	95 mA	3 mA	1.3 mA	1.5 mA	300 uA

* Specified at 40 MHz
Typical values are measured at V_{CC} = 5.0V and T_A = 25 °C

NEW APPLICATION/TECHNICAL NOTE

SYSTEM-LEVEL BENEFITS

The system-level benefits can be seen by examining two different modes of system operation. First, consider a system containing several banks of SRAMs where, in an effort to minimize operating current, only one bank will be selected at any given time during normal operation. While the active bank is being accessed, the address and control signals being switched appear on the inputs of SRAMs in all banks. This causes current consumption by input buffers in standard parts. When using low-power parts, the power consumption in the deselected banks will be reduced to one-tenth of the value for standard parts. This reduces the overall operating power consumption of the system. Next, consider a system with a battery back-up mode requiring data retention in the SRAMs while the devices that interface with the SRAMs are completely powered down. In addition to a 70 percent reduction in battery back-up power consumption, the low-power SRAMs facilitate the system design. When using standard devices, designers must take precautions to ensure that all the address and control inputs are taken to within 0.2 volts of V_{CC} or V_{SS}, while taking care to avoid powering-up other devices in the system. With the low-power devices, only the chip enable inputs need to be taken to these levels—the $\overline{WE}$, $\overline{OE}$ and address inputs may then be driven to, or allowed to assume, any value between V_{CC} and V_{SS}.

SUMMARY

The low-power versions of the Micron 1 Meg SRAMs offer a 90 percent reduction in TTL standby current and a 70 percent reduction in CMOS standby current. These reductions in component standby current lead to reductions in both operating power and battery back-up power consumption at the system level, while at the same time facilitating system design.

TECHNICAL NOTE

STANDARD/PROGRAMMABLE FLAG FIFOS

INTRODUCTION

A FIFO is a dual port memory that is accessed sequentially. Data is read from the FIFO in the same order that it is written. Both data ports are independent and can be accessed simultaneously. One port is dedicated to writing data, while the other port is dedicated to reading data. Both the read operation and write operation can occur simultaneously and asynchronously.

The control signals necessary to access the FIFO differ from the typical random access memories such as SRAMs. Random access memories require an address and control signals to access data. However, due to its sequential nature, the FIFO requires only read or write control signals to perform an access.

The sequential operation of the FIFO makes it ideal for temporary storage or "buffering" of data during a transfer between two hosts operating at different frequencies.

Figure 1

Buffering the transferred data allows both hosts to send and receive data, each at their independent rates. In the case of the fast host, the FIFO allows it to send new data at its rate without the necessity of waiting until the slow host has accepted the previous data. This eliminates the wait states, or dead time, that the fast host would incur otherwise. Hence the fast host accomplishes more work in a given time period. The independent and asynchronous nature of the read and write control signals allows both the fast and slow hosts to maximize their throughput and efficiency.

The required depth, width and speed of a FIFO is determined by the application. The frequency, length and speed of the data transfers as well as the speed of each host sets the criteria for the required FIFO. For example, suppose a fast host can transfer data 40 MHz (25ns per cycle) and the slow host can only accept data at 30 MHz (33ns per cycle) and the data transfer will require a 100 microsecond (μs) interval. In this example, the fast host will complete 4,000 writes and the slow host will complete only 3,030 reads during the data transfer interval. That leaves 970 data items that have been written but not yet read. If we assume that the remaining 970 data items will be read by the slow host before another transfer interval occurs and that the data path is 9 bits wide, then the appropriate FIFO would be a 25ns, 1K x 9 FIFO. This would ensure that the FIFO matches the necessary data width and that all data would be buffered until the slow host could accept it. It would also allow the fast host to send data at its maximum rate, 25ns per cycle. The slow host can read the data at its own rate, 33ns per cycle, without any loss of data. Figure 2 illustrates this example.

Figure 2

FLAG SELECTION

FIFO selection needs to closely match the requirements of the application to acheive the most cost-effective solution. The cost/performance requirements of the specific application determine whether the FIFO is allowed to become either completely full or empty. If the FIFO becomes full, a signal must alert the fast host that this condition exists so the data transfer can be suspended until a location becomes available. A data location will become available when the slow host executes one read from the FIFO. The fast host would also receive a signal when this condition occurs.

Conversely, the slow host must be signaled when the FIFO is completely empty to ensure that erroneous data is not read. When data does become available for reading, the slow host would again be signaled. This allows the slow host to maximize its time doing work instead of constantly checking for available data.

FIFOs use such signals, called "flags," to inform the hosts of extreme conditions. There are two classes of flags used by FIFOs: standard and programmable. The standard flags are full, empty and half-full. These flags respectively signal the hosts when the FIFO cannot receive (full flag) or send (empty flag) any more data, or when the FIFO has crossed its mid-point of storage capacity (half-full flag). The standard flags only indicate an extreme condition and can give no advance warning.

In applications where advance warning is preferred or required, the second type of FIFO flags are desired. The programmable flag FIFOs provide flags that indicate when an extreme condition is about to occur. The full and empty

standard flags are replaced by almost-full and almost-empty-flags respectively. The half-full flag is replaced with a flag that can be programmed to indicate either a half-full condition or a full/empty condition. The almost-full and almost-empty flags are programmable to vary the amount of advanced warning given before the FIFO becomes either full or empty. If these programmable flags are not utilized, the FIFO will default to the standard full, half-full and empty flags.

The Micron Programmable Flag FIFO family can be programmed for offsets ranging from one to (n/8 - 1) increments where "n" equals the depth of the FIFO. Each increment contains two data words: an increment of one equals an offset of two data words, an increment of two equals an offset of four data words, and so on.

For example, the 1K FIFO can have an offset ranging from two data words from the extreme condition to 254 data words from the extreme condition. This corresponds to offset of one and 127 respectively. Hence, the 1K FIFO's programmable flags can be programmed to one of 127 increments of two data-word offsets from the extreme condition. Note that an offset of zero is not used. This would mean that the FIFO is full/empty. That condition is handled by the full/empty flag, if desired. Table 1 illustrates the possible offsets for the 1K x 9 FIFO, expressed in terms of increments and data words from the extreme condition (full/empty).

Table 1

OFFSETS FOR 1K x 9 FIFO	
INCREMENT	DATA WORDS
1	2
2	4
3	6
4	8
•	•
•	•
•	•
127	254

SUMMARY

Micron offers a number of FIFO densities and organizations which employ standard flag and programmable flag versions. Micron FIFOs are expandable in both depth and width for flexibility in tailoring to application requirements.

FIFOs are a valuable tool to maximize performance when transferring data between two hosts of varied frequencies. FIFOs also enable both hosts to maximize performance while ensuring that data is delivered reliably. The standard flags inform the host that an extreme condition has been reached. If advanced warning is required, use programmable flag FIFOs. Each programmable flag is programmed with an offset from the extreme condition. This allows the FIFO to tailor the amount of notice given due to an impending condition so that both hosts may achieve maximum efficiency.

APPLICATION NOTE

MT56C0816 CACHE DATA SRAM FAMILY

INTRODUCTION

The Micron MT56C0816 Cache Data SRAM family was developed in response to a need for compact cache subsystems for the Intel™ 80386 microprocessor. Applications using the 80386 demand maximum performance, and DRAM technology cannot meet the fast access times required for zero-wait-state operation. Statistics show that a small cache subsystem allows the majority of 80386 memory accesses to be completed within the 80386 cycle time. This eliminates the need for wait states[1] to be added to the memory cycle, allowing the 80386 to operate at its maximum performance level. The cache can be designed using fast commodity SRAMs.

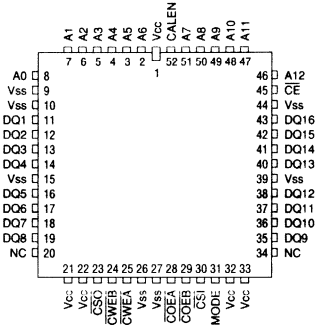
However, the Micron Cache Data SRAM allows cache subsystem designs requiring less space, using less power and offering greater reliability than the fast SRAM implementation. Design and debug times are also reduced, because the Micron MT56C0816 is designed to connect directly to off-the-shelf 80386 cache controllers.

This application note explores why caching is needed. It then discusses how a cache subsystem works, what influences the performance of the cache, and how different cache organizations and architectures compare.

In addition, this application note looks at the most popular off-the-shelf controllers available to implement a cache subsystem. It compares several fast SRAM and cache data SRAM implementations with those controllers. Finally, cache data SRAM advantages are summarized.

MT56C0816
PIN ASSIGNMENT (Top View)

52-Pin PLCC
52-Pin PQFP



BACKGROUND

Microprocessors have typically interfaced directly to DRAM (dynamic random-access memory) main memory due to their relatively slow clock speeds and multiple clock instruction cycles. But over the past few years, complex-instruction-set computer (CISC) microprocessors have driven the clock frequencies into the 20, 25 and 33 megahertz (MHz) range. The two most dominant CISC architectures are the 80X86 and 680X0. The number of clock cycles needed to execute a specific instruction has steadily decreased and is now approaching a single clock cycle for many instructions.

The introduction of reduced-instruction-set computer (RISC) architectures has fueled the quest for higher clock frequencies and reduced clock cycles for each instruction executed. Some of the predominant RISC architectures include SPARC®, 80960, R3000, 29000 and 88000. RISC architectures requiring the absolute minimum number of clock cycles for each instruction are not only approaching single clock execution, but in some cases are able to sustain multiple instruction execution in a single clock cycle. CISC microprocessors are not far behind, and the competition between the CISC and RISC camps is driving processor designers to continuously reach for maximum performance.

This new era of performance is placing heavy demands on memory subsystems that heretofore have been able to

[1] Wait states are one or more additional processor clock cycles added to the memory access cycle. These extra clock cycles keep the processor idling while memory has time to respond to the memory request. For a given processor's clock speed, the number of wait states needed to complete a memory access is directly related to how fast the memory can respond to a read or write request initiated by the microprocessor.

For example, the 80386 can complete a memory cycle in two clock periods. With a 25 MHz processor, this allows 80ns for the processor to output its address to the memory array. It also provides time for the decode circuitry to supply the necessary signals to the memory and enables the memory to respond once it has received the necessary signals. In typical applications, the speed of the memory array that is needed to avoid any wait states is 35ns.

keep pace. For example, an 80386 processor operating at 25 MHz requires a memory access time of close to 40ns if it is to operate at maximum performance (meaning no wait states):

2 x clock cycle time - address delay - data setup - decode logic and buffer delay = (2 * 40) - 21 - 7 - 10 = 42ns

Current DRAM access speeds are in the 70ns to 80ns access range. Even with faster access techniques such as FAST PAGE and STATIC COLUMN modes, the DRAM access time is not sufficient to meet zero-wait-state access times.

The alternative to adding wait states to the system and thus degrading performance is to design a system architecture that makes the memory appear faster to the CPU. Approaches that have been implemented include organizing the DRAM in multiple banks, adding some fast SRAM for specific code and data, and caching.

The use of a cache is applicable in high-end systems as well as cost-conscious, medium-performance systems. At the high end, where the goal is to maximize performance on every processor cycle, the only alternative to cache is the use of very fast SRAMs as the main memory to achieve zero-wait-state performance. This is a very expensive solution. The medium performance systems must constantly balance performance and cost. A small cache in these systems can achieve much higher performance with a relatively small, incremental cost.

CACHE OVERVIEW

WHAT IS A CACHE

A cache is small, fast, local storage for frequently accessed code and data. It consists of high-speed memory (usually SRAM) that resides between the CPU and the main memory (usually DRAM) in a processor system. Figure 1 illustrates a typical block diagram of an 80386-based cache system.

The cache increases the effective speed of the main memory by responding quickly with a copy of the most frequently used items in main memory. The cache control logic checks the address of each memory access and, if it is present in the cache, allows the cache to respond instead of main memory. Accesses to the cache are much faster (typically zero wait states) than accesses to main memory. The more accesses that are made to the cache, the better the overall system performance. Hence the goal in designing a cache is to maximize accesses to the cache (known as the cache hit rate).

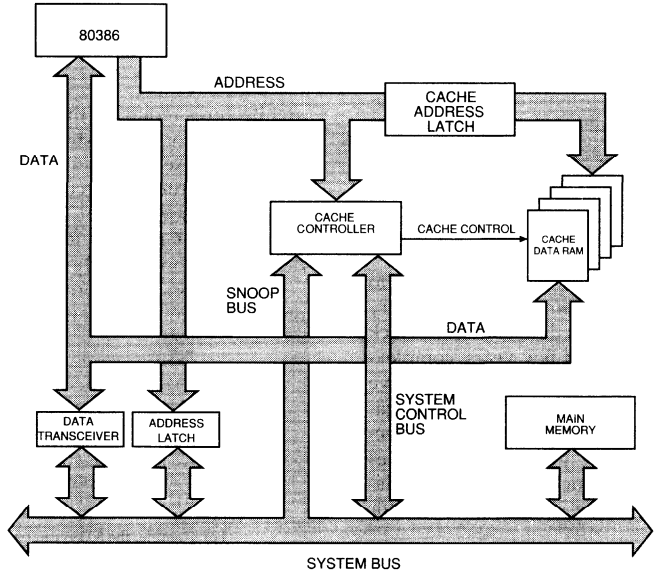


Figure 1
TYPICAL 80386-BASED CACHE SYSTEM

APPLICATION/TECHNICAL NOTE

WHY A CACHE WORKS

The theory of a cache is based on two attributes of computer programs: temporal locality and spacial locality. Temporal locality (locality of time) is an attribute exhibited by computer programs where the same addressed code and data are used repeatedly in a short time. This behavior is typified by program loops, a very prevalent programming structure. Spacial locality (locality of place) is a computer program attribute in which the next needed information is found near the information that was just accessed. This occurs in most programs since related data are stored together (data tables, arrays, etc.) and instructions (code) are typically executed in sequence.

In a cache design, main memory may be thought of as a collection of many small, uniform segments. The cache contains a copy of one or more of these small memory segments that have been used recently. When the processor executes a read from main memory, the cache control determines if that address is contained in one of the small memory segments that are currently resident in the cache memory. If so, the access is completed by the cache. If not, the access is completed by main memory and the memory segment that has just been accessed is placed into the cache for future use. The attribute of spacial locality implies that the information needed next will also be found in the same memory segment just accessed, which is now located in the cache. The attribute of temporal locality implies that the memory location, just accessed, will be used again in the near future.

Table 1

CACHE HIT RATES			
CACHE CONFIGURATION			
HIT RATE (%)*	SIZE (KB)	ASSOCIATIVITY	LINE SIZE (BYTES)
41	1	Direct	4
73	8	Direct	4
81	16	Direct	4
86	32	Direct	4
87	32	Two-way	4
88	64	Direct	4
89	64	Two-way	4
89	64	Four-way	4
89	128	Direct	4
89	128	Two-way	4
91	32	Direct	8
92	64	Direct	8
93	64	Two-way	8
93	128	Direct	8

* Rounded to the nearest whole percent.

PERFORMANCE FACTORS

The performance of the cache (and hence the system) is measured by the cache hit rate, which is the percentage of successful cache accesses. The cache hit rate is determined by specific demands of software being executed and by cache-management policies.

The design factors that influence cache hit rate are: total cache memory size, cache memory organization (associativity), and cache transfer block size. These factors are all interrelated and each needs attention to obtain the optimum cost-effective result. Each factor presents trade-offs of performance, complexity and cost. One factor may be decreased for cost reasons while another may be increased to improve performance. The same or better hit rate may still be obtained. However, the complexity might be increased also. The cache designer must carefully weigh each factor to achieve the best overall cost/performance/complexity ratio. Table 1 compares the cache hit rate of several cache sizes with varying associativity and line sizes.

COHERENCY

Since the cache is a temporary buffer for a section of main memory, the cache designer must take into consideration how to keep the data consistent between main memory and the cache. This is called cache coherency.

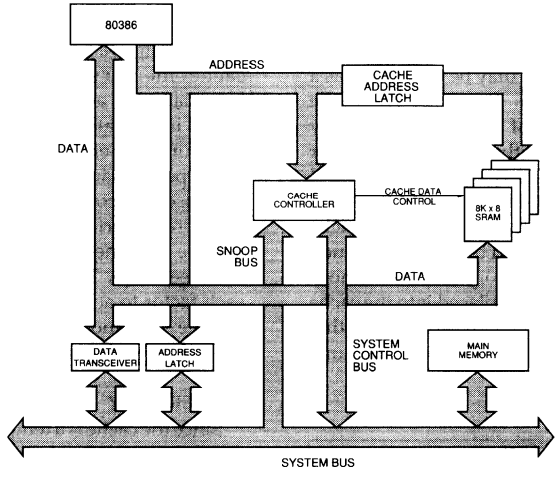
There are instances when an address in the cache might not contain the same information as the same address in main memory. One such situation occurs during a write cycle, where a cache data element is updated to a new value. Now the address in main memory and the same address in the cache have two different values, with the cache containing the newest value. The main memory needs to be updated to contain the same information. This is controlled by the write policy of the cache.

Another such instance occurs when another processor writes information to a main memory address that is also located in the cache. This situation is handled by "snooping". Snooping occurs when the main memory bus is always watched by the cache logic. If a write occurs to a main memory address identical to a cached address, that cache address is marked invalid. This guarantees that if that address is accessed, it will be updated as main memory is accessed for the requested data.

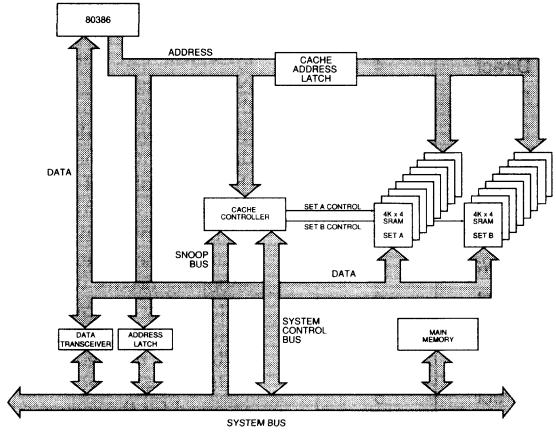
There are two types of cache write policies: write-through and copy-back. A write-through cache will write to both main memory and the cache on each write cycle whenever the addressed location is found to be resident in the cache.

This ensures that the cache and main memory are always coherent, but it requires more main memory accesses, thus increasing bus usage. This also decreases performance due to the large amount of accesses to slower main memory. The main memory accesses may be made more efficient with the addition of write buffers, but this also adds significant complexity and coherency problems in the buffers.

The copy-back policy writes only to the cache, if the address location is present (cache hit), and allows the CPU to proceed. This allows maximum system performance. However, the main memory still needs to be updated. The update of main memory occurs when the line that contains the write address in the cache is replaced by a new line. Main memory write updates occur far less often than the update policy of a write-through design. The copy-back policy also has its drawbacks. Instead of only replacing the data element (possibly one byte) that was written, all the bytes in the line are replaced. This may be as many as four, eight, 16 or more. This can result in a large time penalty when a copy-back occurs.



DIRECT-MAPPED BLOCK DIAGRAM



TWO-WAY-SET BLOCK DIAGRAM

Figure 2

APPLICATION/TECHNICAL NOTE

CACHE CONTROLLERS

All variables in cache design are interrelated and all have trade-offs. For most designs, especially those in the micro arena, caching represents a new realm. Unfortunately, designing a cache from scratch can add an enormous amount of time to the design. Fortunately, several companies have designed off-the-shelf cache controllers, which take into consideration all the trade-offs and performance factors. These controllers meet the majority of the needs of the 80386 cache market.

The three most popular 80386 cache controllers — Intel's 82385, Austek's A38202 and Chips and Technologies' 82C307 and Peak™ — were designed to interface with standard SRAMs as well as additional address latches and possible transceivers.

DIRECT-MAPPED VERSUS TWO-WAY-SET IMPLEMENTATION

The use of an off-the-shelf cache controller eliminates most of the decisions that would occur in a discrete design. The trade-offs that have been made include line size, write update policy, and in some cases, even the cache size and associativity. The majority of controllers allow the user to configure only the associativity (direct or two-way set) and the cache size. The controllers support, without additional logic, both the TWO-WAY-SET ASSOCIATIVE and DIRECT-MAPPED modes.

The trade-off between DIRECT-MAPPED and TWO-WAY-SET ASSOCIATIVE modes is typically one of increased hit rate versus added complexity. Since the controllers have integrated the complexity, it might seem that the only logical choice is to use the TWO-WAY-SET ASSOCIATIVE mode. In a 32 kilobyte (KB) cache, the direct mode will require four 8K x 8 SRAMs (one bank of 8K x 32 bits) while two-way mode will require 16 4K x 4 SRAMs (two banks of 4K x 32 bits). Figure 2 contains typical block diagrams illustrating implementations of direct-mapped and two-way-set designs.

The trade-off, then, is in the additional SRAMs for two-way set. This is reflected as incremental cost, power and board space needed to achieve the higher hit rate obtained over the direct-mapped implementation. For the 32KB cache size, the additional hit rate of the two-way-set implementation makes it the best choice if the board space is available. In the medium-to-high-end performance market, the extra performance (see Table 1) delivered by the two-way-set design is worth the extra cost.

Table 2 compares the board real estate and power requirements of each configuration. The two-way-set implementation requires eight 74F245 transceivers to control the flow of data between each bank and the common data bus. Figure 3 illustrates the board space requirements of each implementation.

The assumptions used for the board space comparison were .050 inch chip-to-chip spacing and .050 inch outside border around the circuitry. The power comparison is based on a 25 MHz design assuming 10ns decoding delay. This gives the following equation for the cache 8K x 8 SRAM access time:

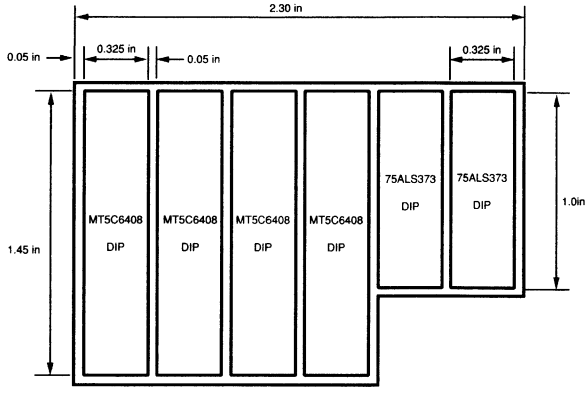
> Cache SRAM available access time = 4 * 386CLK2 - 386 address delay - 386 ready setup - SRAM enable decode - 74F373 delay = (4 * 20ns) - 21ns - 9ns - 10ns - 9ns = 31ns.

The 8K x 8 configuration would require SRAMs with an access time of 25ns. For the two-way-set configuration, an additional 6ns must be subtracted for the delay through the 74F245 transceivers. This barely provides 25ns for the 4K x 4 SRAM access time in this latter implementation. Any other delays that exist in the data access path must also be taken into consideration. In the case of the 4K x 4 SRAMs, a 20ns part will probably be required.

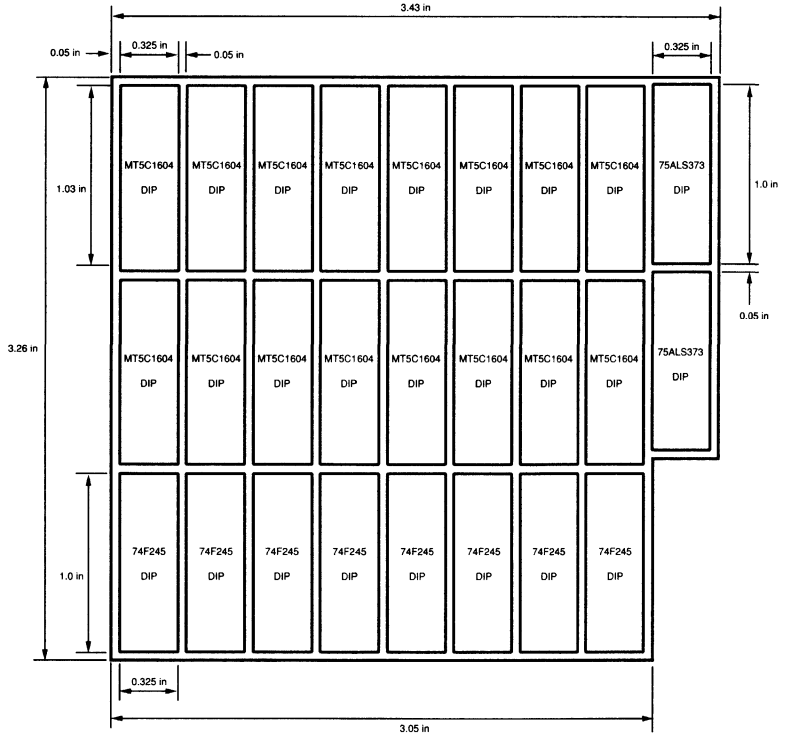
Table 2

32KB CACHE CONFIGURATION COMPARISON				
CONFIGURATION	**SRAM**	**# SRAMs**	**AREA (in²)**	**POWER (W)**
Direct-Mapped	8K x 8	4	3.23	2.75
Two-Way-Set	4K x 4	16	10.57	10.55*

* The 4K x 4 configuration incorporates two banks of eight SRAMs each. One bank is active, while the other is in standby mode. This fact was used in the power calculations.



DIRECT-MAPPED SPACE REQUIREMENT USING 8K x 8 SRAMS



TWO-WAY-SET SPACE REQUIREMENT USING 4K x 4 SRAMS

Figure 3

APPLICATION/TECHNICAL NOTE

MT56C0816 INTEGRATED CACHE SRAM

The MT56C0816 is an application-specific 8K x 16 SRAM designed for, but not limited to, cache data SRAM implementations. The MT56C0816 is designed to be used in either direct-mapped or two-way-set designs. It incorporates an on-chip address latch, on-chip multiplexing between the two SRAM banks (for two-way-set mode), fast output enable times and low power consumption.

Almost all designs have used the MT56C0816 in the TWO-WAY-SET mode of operation. This is due to the fact that the MT56C0816 eliminates the major problems in implementing the TWO-WAY-SET mode architecture, namely the cost, space and power. Before the MT56C0816, a two-way-set implementation required three times the board space and four times the power of a direct-mode design when using standard SRAMs.

Due to the integration of on-chip address latches and multiplexors, often a lower-speed MT56C0816 can be used in place of a higher-speed, more costly standard SRAM. The advantages of the MT56C0816 don't stop here. It is widely second-sourced by other suppliers, the access time has been reduced to 20ns and it is available in the smaller PQFP package.

Table 3 compares the board space, power and access time requirements of standard SRAMs and both packages of the MT56C0816 in a 32KB cache design. The numbers presented are applicable to both DIRECT-MAPPED and TWO-WAY-SET implementations for the MT56C0816 and 4K x 4 SRAMs. The use of 8K x 8 SRAMs in a two-way configuration requires a minimum of 64KB in the cache and is not considered in the comparison. The same board area assumptions are used in Table 3 as in Table 2 regarding chip-to-chip and circuitry border spacing. The area values are normalized to the MT56C0816 in the PQFP package.

The SRAM access time and power considerations are based on a 33 MHz 80386 design assuming a 10ns enable decode time. The cache SRAM access time equation is as follows:

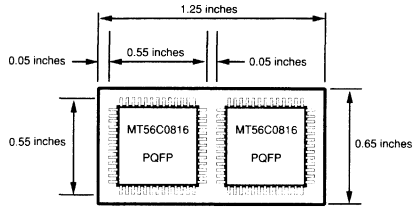
Cache SRAM access time = 4 * 386CLK2 - 386 address delay - 386 ready setup - SRAM enable decode - 74F373 delay = (4 * 15ns) - 15ns - 7ns - 10ns - 9ns = 19ns

This will require 8K x 8 SRAMs with a 15ns access time. The 4K x 4 implementation requires that the transceiver delay time (6ns) also be subtracted, which leaves only 13ns. Hence, a 12ns part must be used.

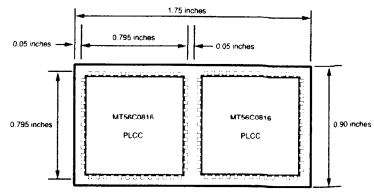
Table 3

CACHE SRAM COMPARISON (33 MHz)				
DEVICE	**NUMBER OF DEVICES**	**PC BOARD AREA**	**POWER (W)**	**ACCESS SPEED (ns) REQUIRED**
MT56C0816 PQFP	2	1.00	2.2	25
MT56C0816 PLCC	2	1.94	2.2	25
8K x 8 SOJ 74F373 SOIC	4 2	2.28	3.15	15
8K x 8 DIP 74F373 DIP	4 2	3.99	3.15	15
4K x 4 SOJ 74F373 SOIC 74F245 SOIC	16 2 8	8.58	12.15*	12
4K x 4 DIP 74F373 DIP 74F245 DIP	16 2 8	13.05	12.15*	12

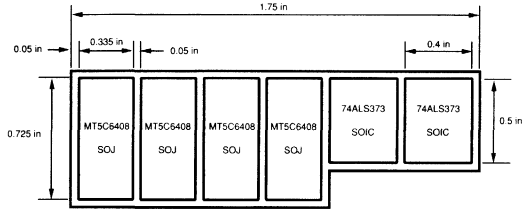
* The 4K x 4 configuration incorporates two banks of eight SRAMs each. One bank is active while the other is in standby mode. This fact was used in the power calculations.



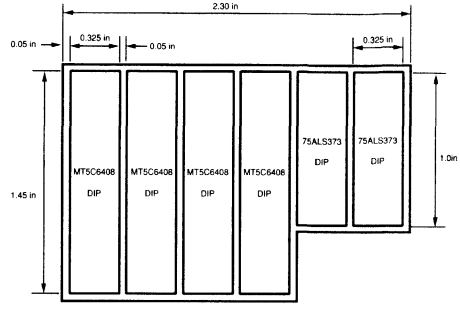
MT56C0816 PQFP



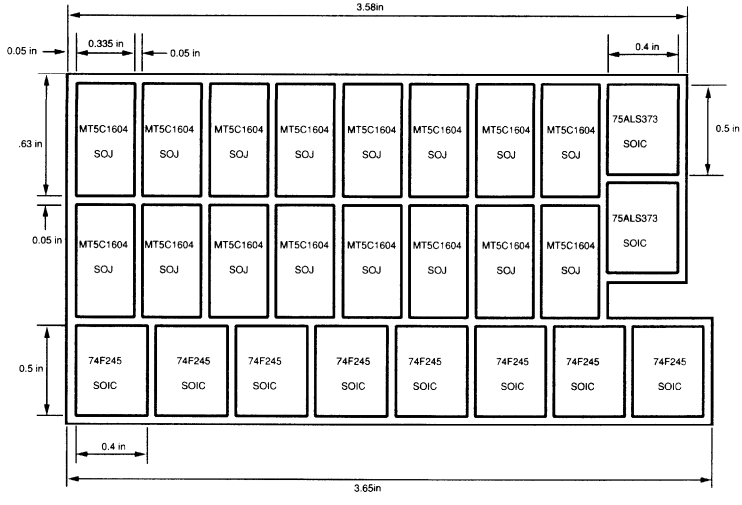
MT56C0816 PLCC



8K x 8 SOJ/SOIC



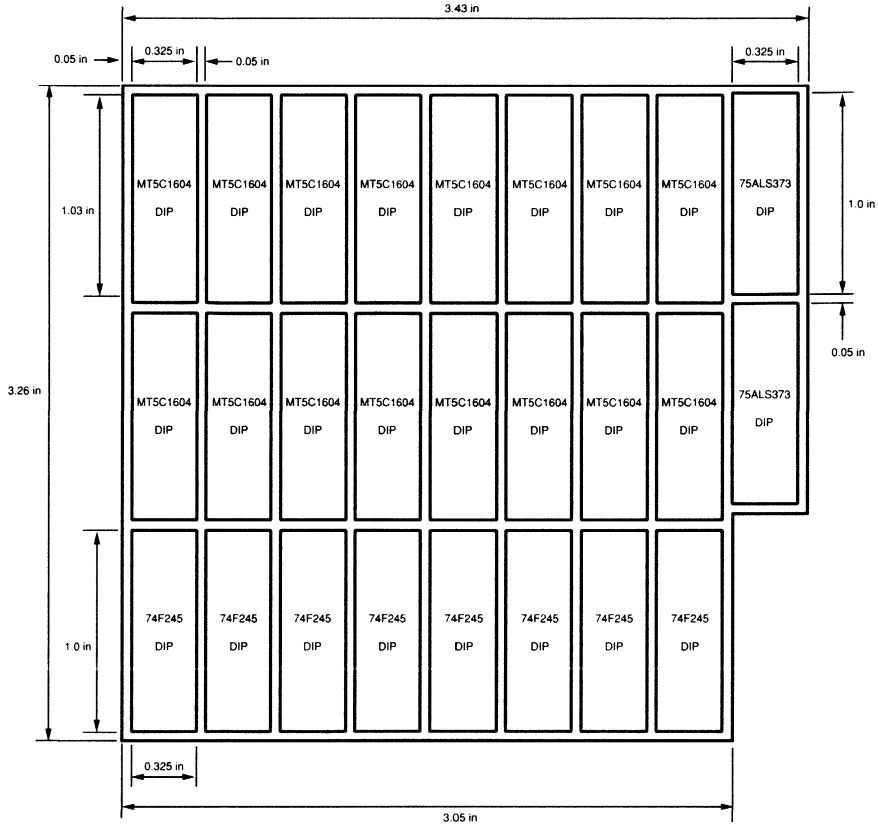
8K x 8 DIP



4K x 4 SOJ/SOIC

Figure 4

APPLICATION/TECHNICAL NOTE



4K x 4 DIP

Figure 5

The MT56C0816 incorporates the address latch on-board and allows 9ns to be added back into the SRAM access time. This yields a 28ns access time for an MT56C0816 design, which is easily met by the 25ns part. This access time is applicable to both the direct mode and two-way set configurations since the data multiplexing is also on-chip.

Figures 4 and 5 illustrate the board space required by the MT56C0816 and the standard SRAM configurations that are summarized in Table 3.

OPTIMUM SYSTEM

The available, off-the-shelf cache controllers allow very quick and efficient cache subsystem designs for 80386-based systems. And an off-the-shelf controller teamed with the MT56C0816 maximizes the system performance/cost ratio. The MT56C0816 allows the controller to be employed in its highest performance mode, two-way-set associativity, without the disadvantages incurred using standard SRAMs.

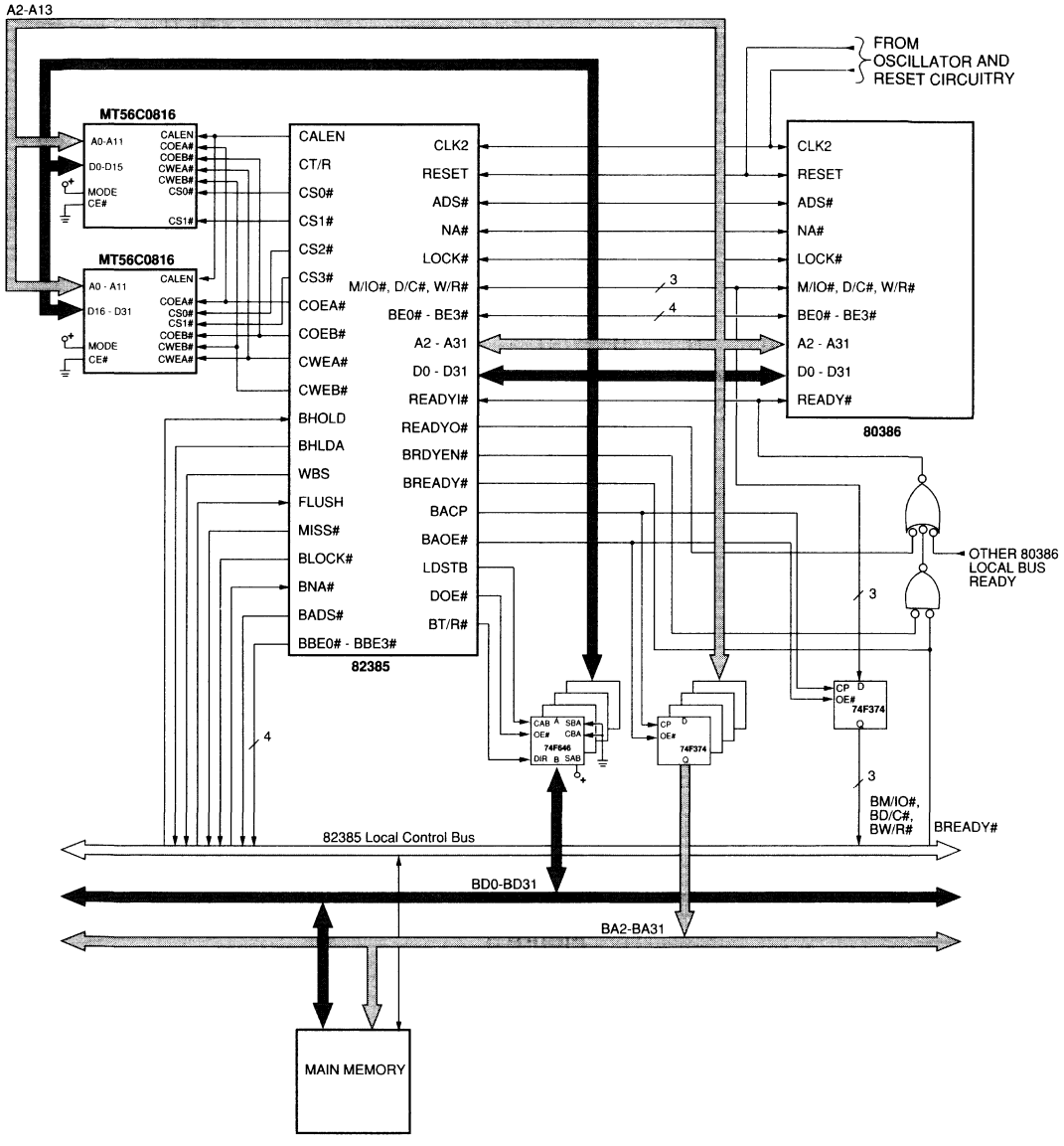


Figure 6

APPLICATION/TECHNICAL NOTE

Table 4

MICRON CACHE SRAM FAMILY				
PART NUMBER	**DESCRIPTION**	**SPEED (ns)**	**PACKAGE**	**AVAILABILITY**
MT56C0816	Dual 4K x 16 or 8K x 16 Addresses 0 through 11 are latched	20, 25, 35	PLCC PQFP	Now
MT56C0818	Dual 4K x 18 or 8K x 18 Addresses 0 through 11 are latched	20, 25, 35	PLCC PQFP	Now
MT56C2818	Dual 4K x 18 or 8K x 18 80486 self-timed write; used on Intel Turbocache 486™ module	24, 28	PLCC PQFP	Now
MT56C3816	Dual 4K x 16 or 8K x 16 Addresses 0 through 12 are latched	20, 25, 35	PLCC PQFP	Now
MT56C3818	Dual 4K x 18 or 8K x 18 Addresses 0 through 12 are latched	20, 25, 35	PLCC PQFP	Now

A TWO-WAY-SET design using the MT56C0816 requires only two parts versus 10 for an 8K x 8 SRAM implementation and 26 for a 4K x 4 implementation. A DIRECT-MAPPED design using the MT56C0816 requires only two parts versus six for an 8K x 8 SRAM implementation and 26 for a 4K x 4 implementation. In addition to the board-space, power and integration advantages, the MT56C0816 offers a direct connection to the controllers. This means higher system reliability and easier design and debugging over the standard SRAM implementations. Figure 6 shows a detailed diagram of a system using the MT56C0816.

MORE SOLUTIONS

An entire family of cache-specific data SRAMs is available. Table 4 lists the members of the cache SRAM family.

In addition, Micron was the first to introduce the MT56C0816 both in a 20ns access speed and in the thin, small-outline PQFP package.

SPECIAL CONSIDERATIONS

The Micron MT56C0816 was designed for a specific generation of cache implementations for the 80386. That generation required a nonlatched A12 address and a faster A12 access time. Since then, designs employing certain off-the-shelf controllers are more efficiently implemented if address line A12 is latched on the cache data SRAM. These designs do not require the faster A12 access time. In order to keep pace with the everchanging design community, Micron introduced time-frame versions of the MT56C0816 and the MT56C0818 with address A12 latched. The part numbers of these new devices are MT56C3816 and MT56C3818 respectively.

The latched A12 version of the cache data SRAM can be appealing in 80386DX designs where the cache uses a TWO-WAY-SET ASSOCIATIVE architecture and the cache size is 64KB or larger. The latched A12 parts are applicable for 80386SX designs where the cache is structured using a TWO-WAY-SET ASSOCIATIVE organization and the cache size is 32KB or larger.

Designs using a DIRECT-MAPPED architecture essentially use the cache data SRAM as an 8K x 16 SRAM and as such the latched version would be advantageous in all cases. Whether the latched or unlatched A12 version of the cache data SRAM is more advantageous depends entirely on the specifics of each individual design.

SUMMARY

The Micron MT56C0816 has been as important to 80386 caching solutions as the off-the-shelf controllers from Intel, Austek and Chips & Technologies. The direct connection of the MT56C0816 to controllers makes its implementation more appealing for the designer from both a design and debug standpoint. The reduced board space, power and comparable cost to commodity SRAM implementations are advantages that make the MT56C0816 the right choice for new designs.

Micron's MT56C0816 adds reliability to systems due to the reduced component count. It also offers other, less obvious cost advantages. For instance, reduced board space requirements directly affect board manufacturing costs and allow more components to be placed on the board. Better reliability means lower costs due to fewer returns and fewer board revisions. The MT56C0816 also minimizes inventory and assembly costs. Clearly the Micron MT56C0816 is a superior solution to standard SRAMs in cache designs.

OVERVIEW

Product reliability is a product's ability to function within given performance limits under specified operational conditions over a specified length of time. This section contains a brief overview of some of the issues that affect the reliability of IC devices and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability Literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_0.

The reliability curve in Figure 1 is divided into three segments: infant mortality, random failure, and wear out. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out these failures, Micron evaluates all our products using intelligent burn-in. Our unique AMBYX® intelligent burn-in/test system, is described in the following section.

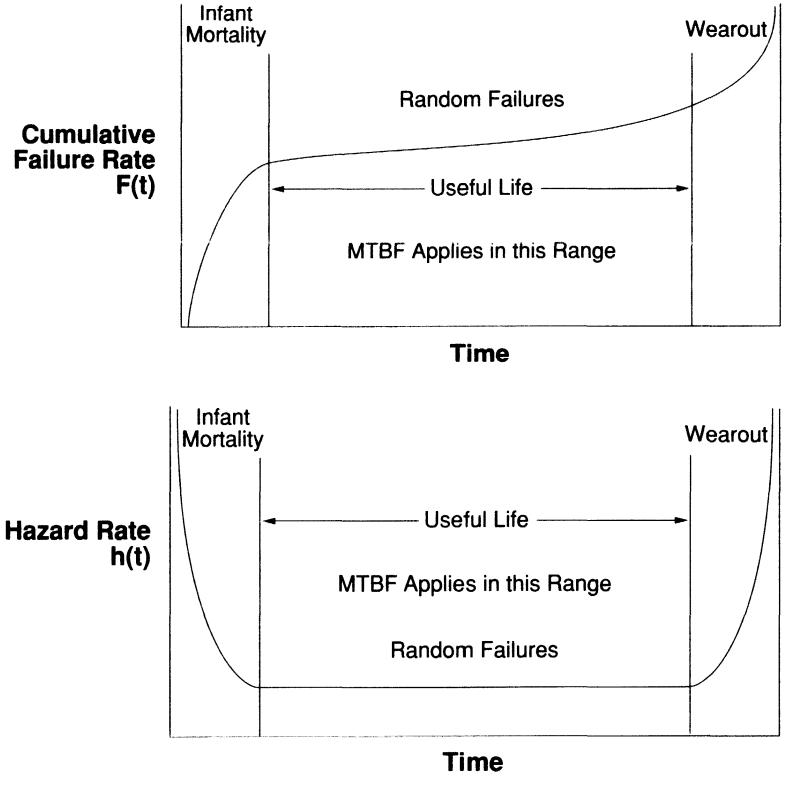


Figure 1
RELIABILITY CURVE

MICRON'S AMBYX® INTELLIGENT BURN-IN AND TEST SYSTEM

As the semiconductor industry has evolved, burn-in has become regarded as critical to product reliability. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. In 1986, we were unable to find a system that met our requirements, so we introduced the concept of "intelligent" burn-in and developed the AMBYX® intelligent burn-in and test system. Today, we use it to test every component and system-level product we make.

With AMBYX, we can determine if the failure rate curves of *individual* product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings the slightest variation in a product's failure rate to our attention.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern, and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then, we ramp up the oven to 85°C for more functional testing. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. The typical test results shown make up the first portion of the bathtub curve of component reliability.

There are two important reasons that Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test. All semiconductor manufacturers use this test to calculate the random field failure rates. Second, we want to be sure we are not introducing new failure modes (failures unrelated to normal wearout) caused by testing under extremely elevated conditions. In this way, Micron ensures that we've effectively screened our products for infant mortalities.

Control charts, such as the one shown in Figure 3, alert us to trends in the failure rates of some lots. When we detect an increase in a certain failure rate, we pinpoint the lots that need additional burn-in cycles to identify all variables that might influence the failure rates of those lots. Such variables could include fabrication and assembly equipment, manufacturing shifts and time frames when the lots were processed through specific steps.

The overall benefits of intelligent burn-in are wide ranging. Four of the most important benefits are summarized below:

- Using the AMBYX system, we are able to determine the optimal amount of burn-in time required for each product and/or process. We are thus able to correlate the burn-in test results with millions of device hours of HTOL testing, used to calculate hard error rates for all Micron products.
- The AMBYX system ensures that all weak devices are removed, while eliminating the cost of additional burn-in time required by unmonitored burn-in systems.
- By using AMBYX, we are able to react quickly to reliability-related process shifts, correlating lots that need additional burn-in cycles with all variables that might be influencing the failure rates of those lots. Examples of such variables might include fabrication and assembly equipment, manufacturing shifts, time frames during which the lots were processed through specific steps, and process recipes.
- AMBYX enables us to ship a consistently reliable product.

Other benefits include the ability to differentiate between hard and soft errors and to check for variation in these parameters on production lots.

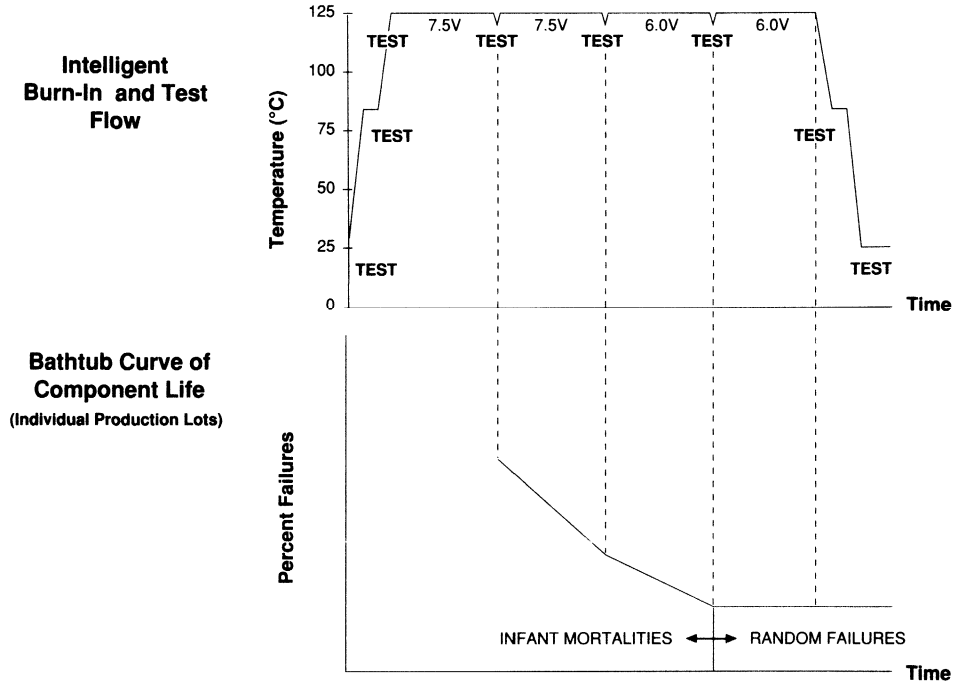


Figure 2
AMBYX BURN-IN/TEST FLOW AND TEST RESULTS

ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of environmental stress tests.

During these tests, we stress the devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under *normal use.* Figure 3 shows the conditions for these environmental stress tests. The EPM program described in Figure 3 is for Micron's 1 Meg SRAM.

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 6.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	100 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% R.H., 5.5V, Alternating Bias)	1,008 Hours	50 Devices
AUTOCLAVE (121°C, 100% R.H., 15 PSI, No Bias)	288 Hours	25 Devices
LOW TEMPERATURE LIFE (-25°C, 7.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	5 Devices
TEMPERATURE CYCLE (-65°C TO +150°C, Air to Air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C TO +125°C, Liquid to Liquid)	700 Cycles	10 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015.7	40 Devices
HIGH TEMPERATURE STEADY STATE (150°C, 6.5V)	1,008 Hours	5 Devices
V_{CC} BLOW (≥100 mA)	–	10 Devices

NOTE: Samples pulled from five different lots at finished goods.

Figure 3
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 1 MEG SRAM

FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours), and is calculated as follows:

$$\text{Failure Rate} = \frac{\text{Pn}}{\text{Device hours} \times \text{AF environment}}$$

AF is relative to the typical operating environment.

where: Pn = Poisson Statistic (at a given confidence level). In our example, Pn = 0.916 at 60 percent confidence level.

Device hours = sample size multiplied by test time (in hours) In our example, device hours equal 1.893×10^6 in an accelerated environment.

AF = acceleration factor between the stress environment and *typical* use conditions. For the 1 Meg SRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 93. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 1 Meg SRAM family is computed as follows:

$$\text{Failure Rate} = \frac{0.916}{(3.04 \times 106)\ (93)}$$
$$= 5.388 \times 10\text{-}9$$

where: total device hours at test conditions = 1.893×10^6. Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of 93 equals: $93(1.893 \times 10^6) = 176 \times 10^6$.

To translate this failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

$$\text{Failure Rate} = (5.203^8 \times 10^{-9}) \times 10^9$$
$$= 0.0005203\% \text{ or } 0.0005\% \text{ per 1K device hours}$$

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

$$\text{Failure Rate} = (5.203 \times 10^{-9}) \times 10^9$$
$$= 5.203 \text{ or } 5 \text{ FITs}$$

ACCELERATION FACTOR CALCULATION

Again, using the 1 Meg SRAM for our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5.5V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$AF_{t1/t2} = e^{\left[\frac{E_a}{kT_1} - \frac{E_a}{kT_2}\right]}$$

where: k = Boltzmann's constant , which is equal to 8.617×10^{-5} eV/K

T_1 and T_2 = typical operating and stress temperatures, respectively, in kelvins

E = activation energy in eV (For oxide defects, which is the most common failure mechanism for the 1 Meg SRAM, used in our example, the activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.622.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$AF_{v1/v2} = e^{[\beta (v_1 - v_2)]}$$

where:

v_1 and v_2 = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 1 Meg SRAM used in our example, ß equals 2.5).

Thus, the voltage acceleration factor for the 1 Meg SRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 12.182.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$\begin{aligned} AF_{overall} &= AF_{temperature} \times AF_{voltage} \\ &= 7.622 \times 12.182 \\ &= 93 \end{aligned}$$

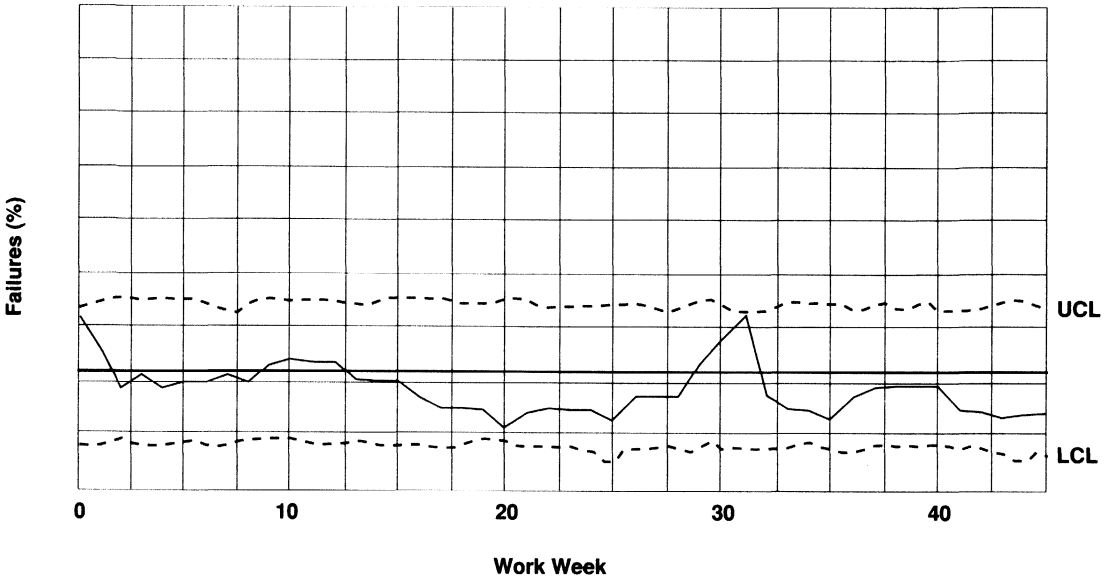


Figure 4
AMBYX FOURTH QUARTER FAILURES

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a one-percent sample from each production lot. These samples are subjected to visual and electrical testing in order to measure the acceptable quality level (AQL) of all outgoing product. Figure 4 shows a flowchart illustrating Micron's AQL test procedure.

Visual or mechanical testing consists of an unaided visual inspection of the sample devices for any physical irregularities that could negatively affect their performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using ATE (automatic test equipment) systems. Testing is conducted at room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. If after completing this analysis, the quality assurance engineer determines which production monitor or test should have caught the failure, and the entire lot is retested at that point in the test flow. These are important steps to preserve the integrity of our test process.

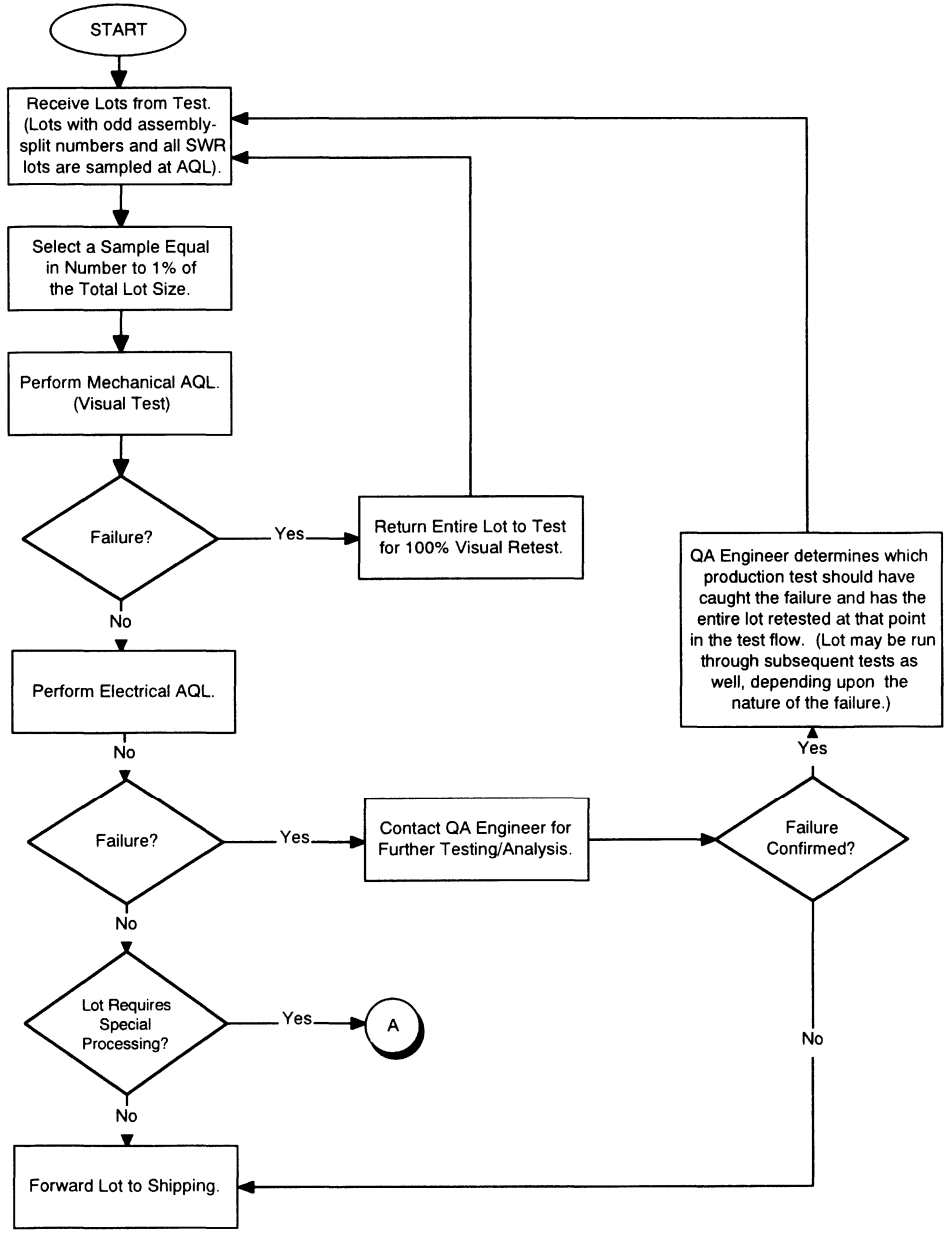


Figure 5
AQL TEST FLOW FOR ALL OUTGOING PRODUCTS

Example of Special Processing:
Lot Mounted on Tape and Reel

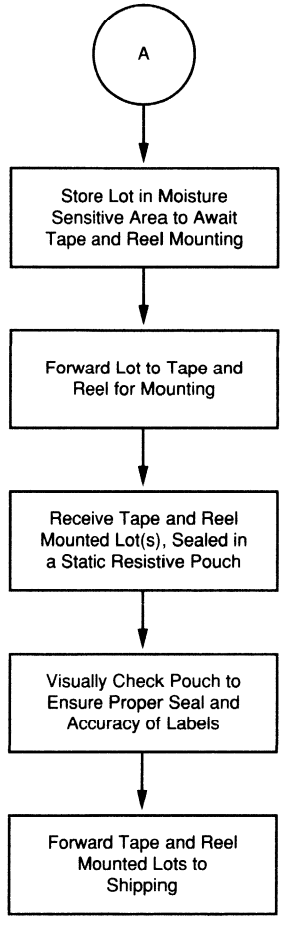


Figure 6
AQL TEST FLOW — SPECIAL PROCESSING

AUTOMATED DATA CAPTURE & ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 5 shows the various functional areas that provide the input to our VAX data bases.

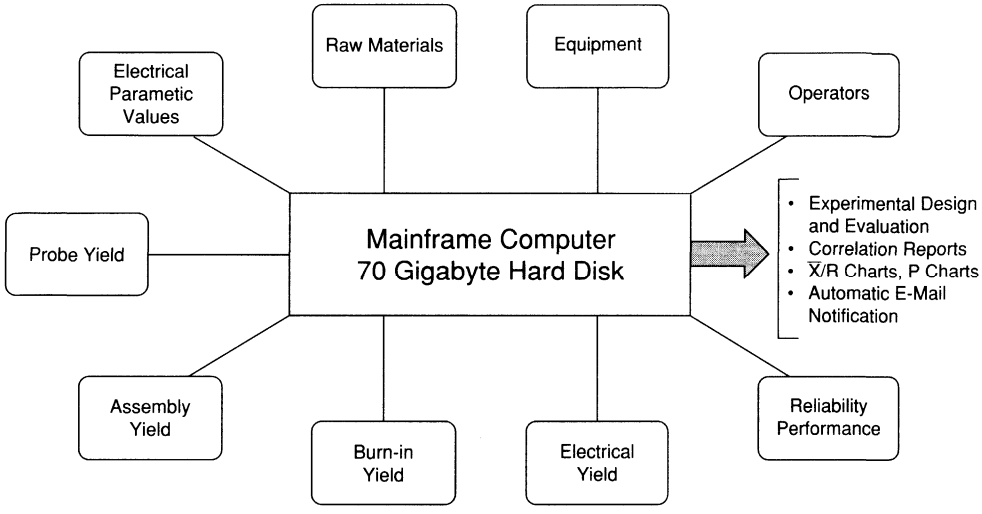


Figure 7
STATISTICAL CORRELATION

DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\overline{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) are entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material, and environmental variables.

DEVICE TRACEABILITY

Each Micron device can be traced to its original fabrication lot through an alphanumeric code inscribed on both the top and bottom of the package. Alphanumeric codes are maintained in our computer network and can be assessed from any computer terminal. The system user can request information relative to a particular scribe or series of scribes. Information provided by the system includes: the lot number associated with each scribe specified, the date and time that the lot was inscribed and the part type associated with the lot. If the scribe number is not readily available, this same information can also be requested by entering a specific lot number or lot number series, or by specifying the date and time that a device or lot of interest was inscribed.

In addition to the package scribe, we are in the process of adding a laser mark to each individual die on the wafer. This new laser mark will provide a level of traceability yet unmatched in the industry by identifying the location of the parent wafer within the fabrication lot as well as the precise location of the die on the wafer. This *complete* traceability will provide significant advantages in analyzing reliability issues and further enhance our ability to continuously improve product performance.

STATISTICAL TECHNIQUES AND TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means.

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular pieces of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

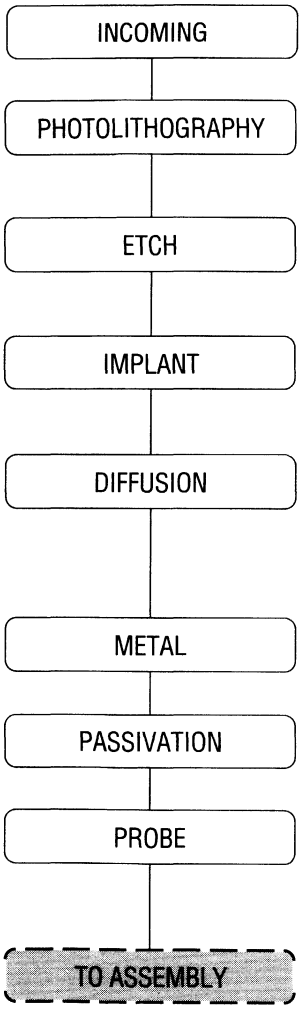
Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE

This analysis software is used for experimental design, and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and for trouble shooting. It is also used to determine the relationships between process output and probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide for more accurate fabrication output planning.

FABRICATION



Incoming
All starting material is verified for cleanliness, uniformity and compliance with Micron's specifications. Each wafer receives an individual laser scribe for total product traceability.

Photolithography
Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch
The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Implant
Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping," and forms conductive regions on the wafer.

Diffusion
Silicon dioxide, nitrate and polysilicon layers are formed on the wafer during a number of high-temperature furnace processes. The wafers are exposed to various gases, which either react with the silicon, causing it to oxidize and form an SiO_2 layer, or react with each other, forming polysilicon and nitride deposits. These layers are patterned using photolithography, and form the layers of diodes, transistors and capacitors making up the circuit. High temperature furnaces are also used to introduce and diffuse dopants into the wafers.

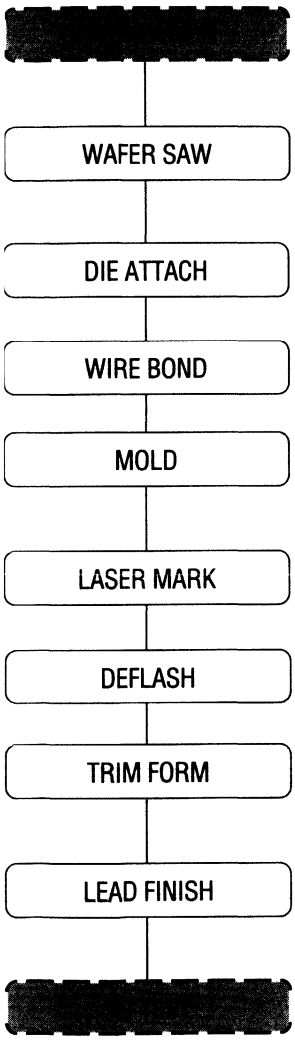
Metal
A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

Passivation
The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe
When the fabrication process is complete, each wafer consists of many "die." Each die on the wafer is taken individually through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map" storing data on each functioning (good) die. All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good die are packaged.

Assembly (see next page)

ASSEMBLY



Fabrication
The fabrication process yields silicon wafers containing many discrete integrated circuits or die. Following fabrication, the wafers undergo assembly processing where the individual die are separated and encapsulated according to package specifications.

Wafer Saw
Wafers that have finished fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach
With automated pick-and-place equipment, the good die as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Wire Bond
With high-speed automated equipment, interconnections are made with gold wire (the diameter of a human hair). These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Mold
A heated mold with a hydraulic press is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

Laser Mark
A laser mark is scribed on the bottom side of the package. This mark is a code used to identify the assembly manufacturing lot.

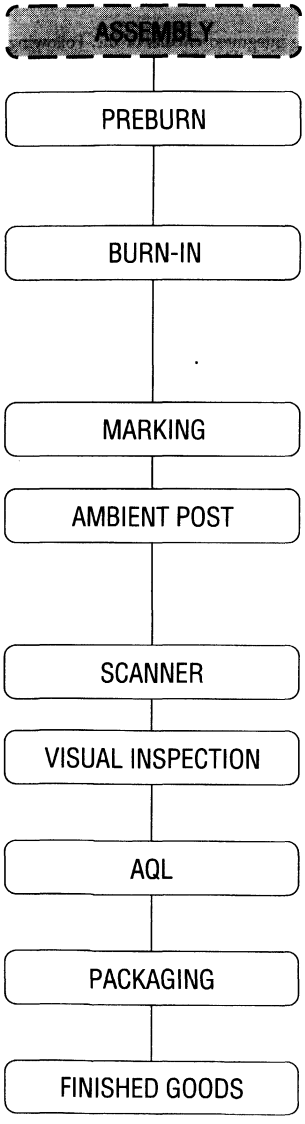
Deflash
Prior to lead-finish processing, the leadframes are run through chemical baths to remove contaminants. This process is known as deflash.

Trim/Form
A press-and-tool set is used to cut the leadframes, separating the encapsulated die into discrete devices and forming the leads into the appropriate shape for the package specified (ZIP and DIP packages for through-hole applications; SOJ, PLCC, and TSOP packages for surface-mount applications).

Lead Finish
The leads of each device receive a finish of tin/lead solder or tin/lead electroplating to ensure reliable application by the customer. If the leads receive an electroplated rather than solder finish, the lead-finish step is performed prior to the trim and form.

Test (see next page)

TEST



Assembly
Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Preburn
All testing is conducted at 125°C. Parametric tests are performed to detect opens, shorts, and input/output leakage and to determine whether standby/operating currents are within specified limits. Functional tests include low and high Vcc margin and vbump. Patterns performed include march, scan and address complement. Backgrounds used include solids and checkerboard. The specific tests performed depend upon the product being tested.

Burn-in
Micron uses its exclusive AMBYX® intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 7.5V Vcc for the first two intervals and 125°C, 6V Vcc for the final two intervals. Functional testing is performed at 85°C and back to 25°C AMBYX tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 7.5V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Marking
Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Ambient Post
All testing is conducted at 25°C. Parametric tests are performed to detect opens, shorts, and input/output leakage. These tests also determine whether high and low levels of voltage input and output as well as standby and operating currents are within specified limits. Functional tests include low and high Vcc margin and vbump. Patterns performed include march, scan and address complement. Backgrounds used include solids and checkerboard. The specific tests performed depend upon the product being tested.

Scanner
Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection
All devices, now tested to be functional, are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired if possible. Data on the type of defects found is carefully recorded and used for improving the manufacturing processes in both assembly and test.

AQL
A quality assurance monitoring program oversees the electrical and environmental performance of all production lots. New products that have not met required production volume and ppm (parts per million) levels are held at this stage until it is confirmed that electrical and environmental test results meet Micron requirements.

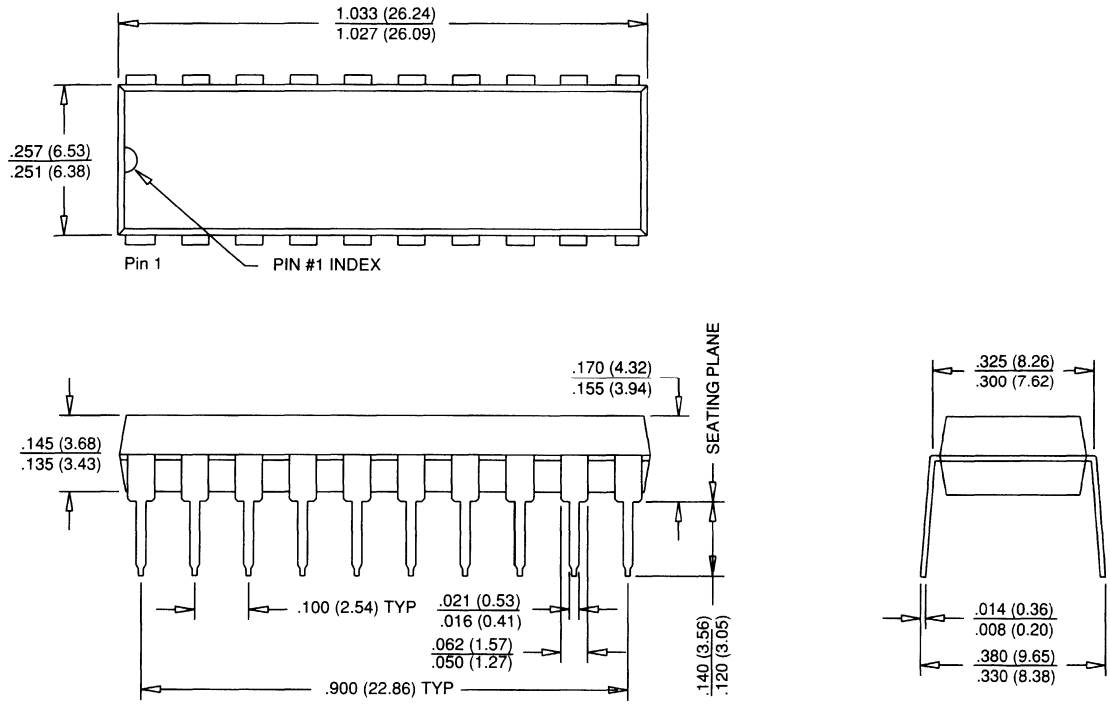
Packaging
Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry packed in vacuum sealed bags with a desiccant, or placed in black antistatic bags.

Finished Goods
Devices are shipped through a system that maintains lot identity.

MICRON

20-PIN PLASTIC DIP

SA-1



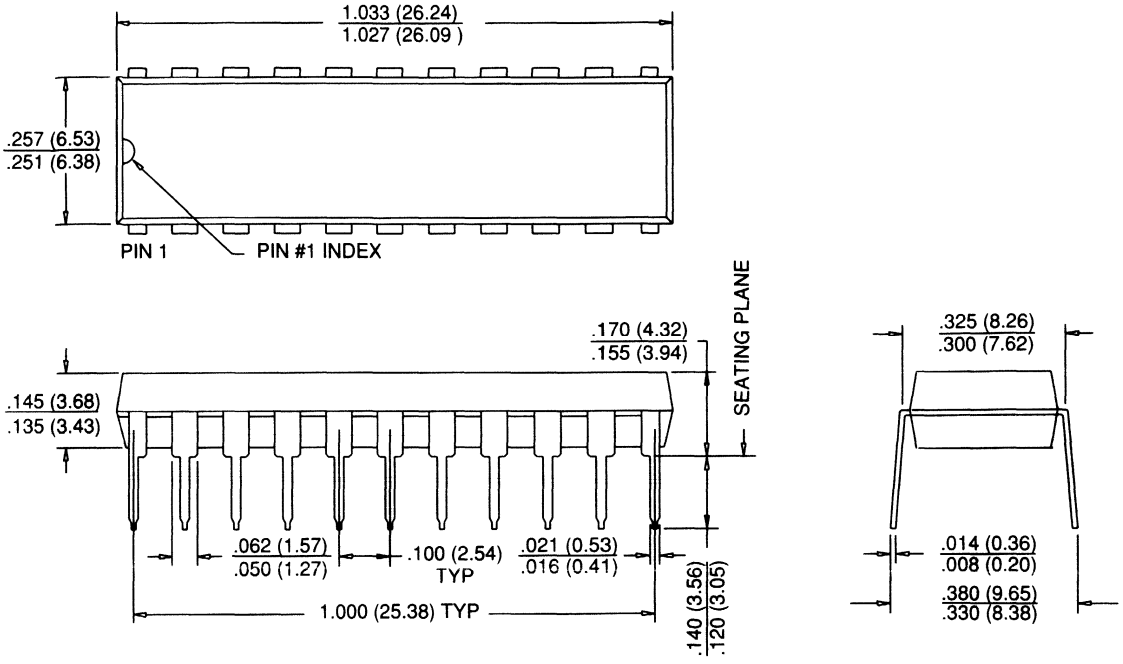
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

22-PIN PLASTIC DIP

SA-2

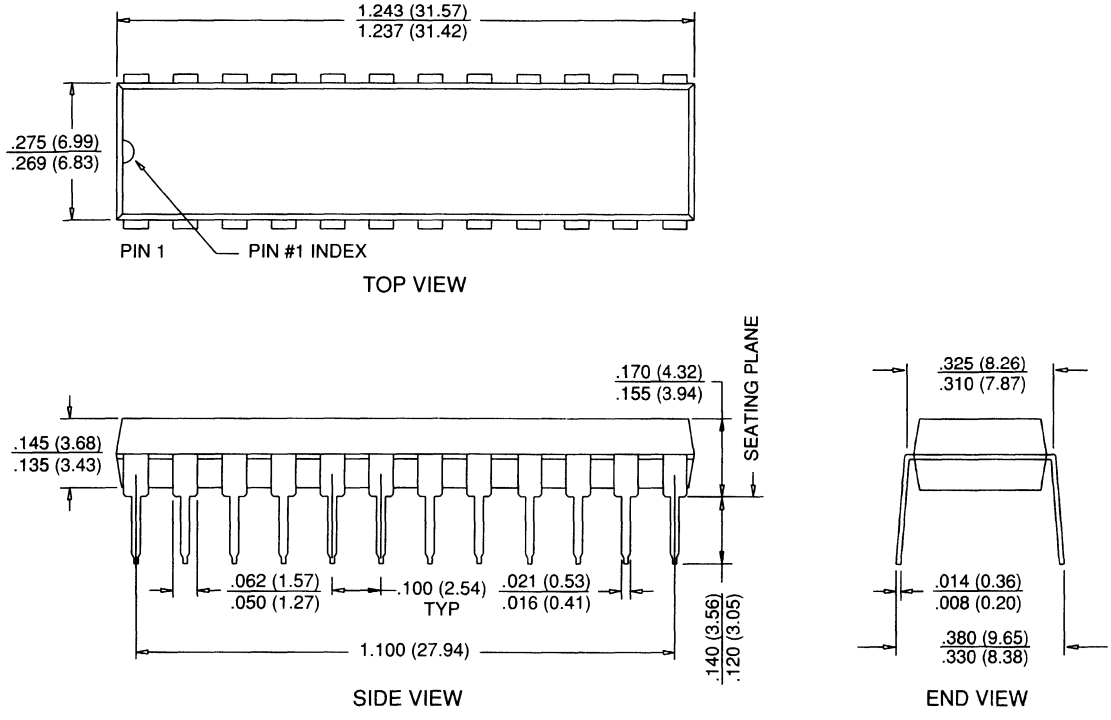


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC DIP

SA-3

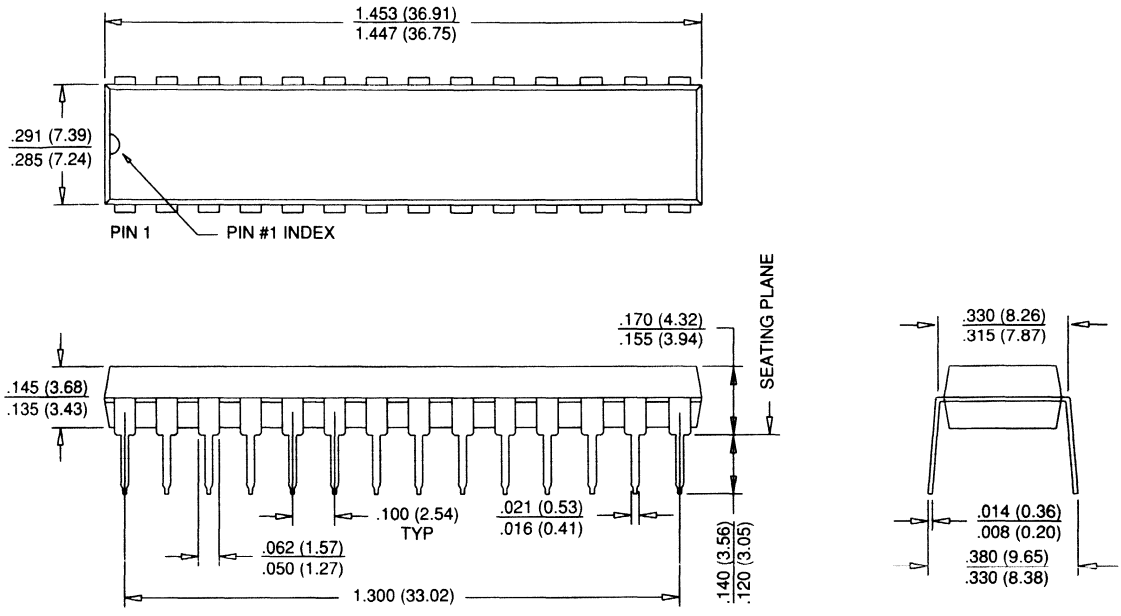


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

SA-4

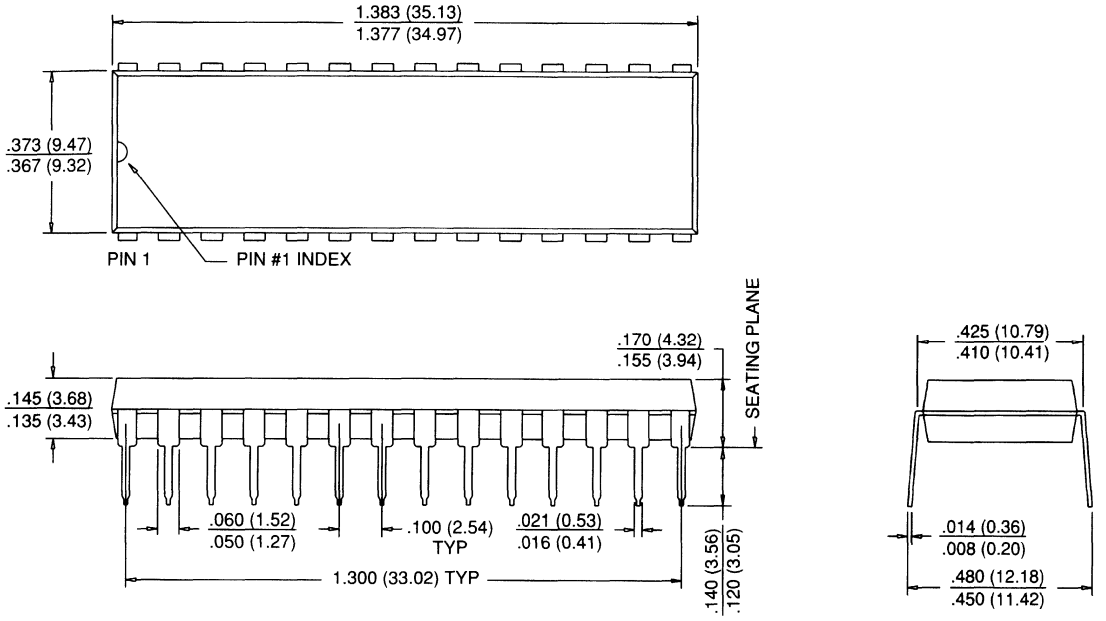


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

SA-5



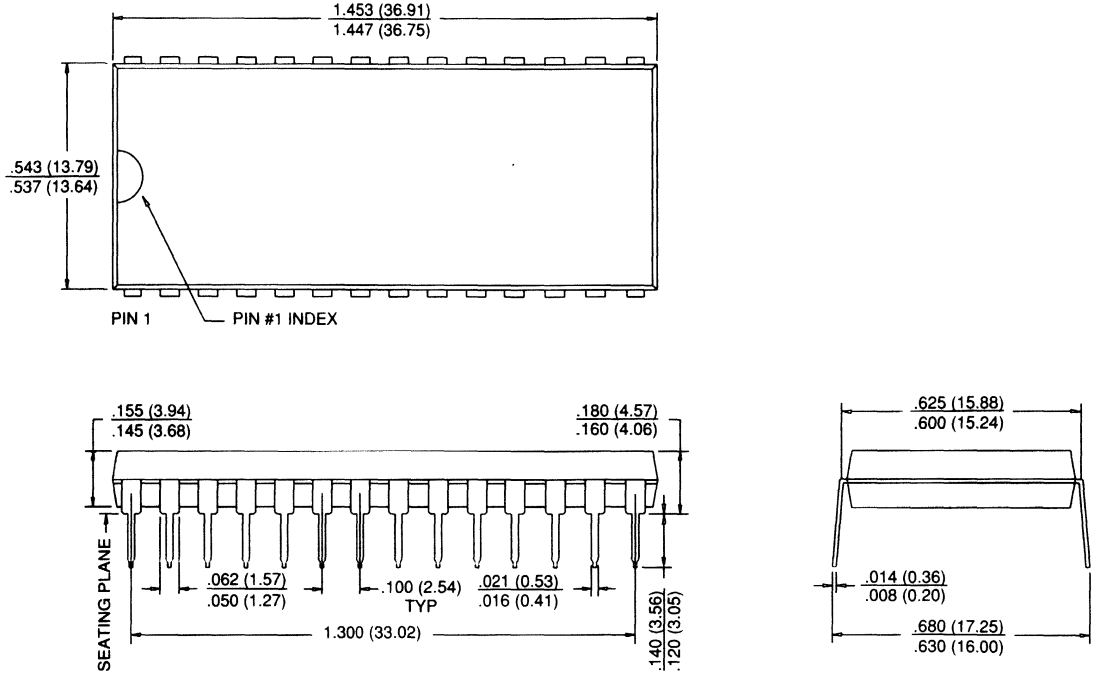
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

28-PIN PLASTIC DIP

SA-6

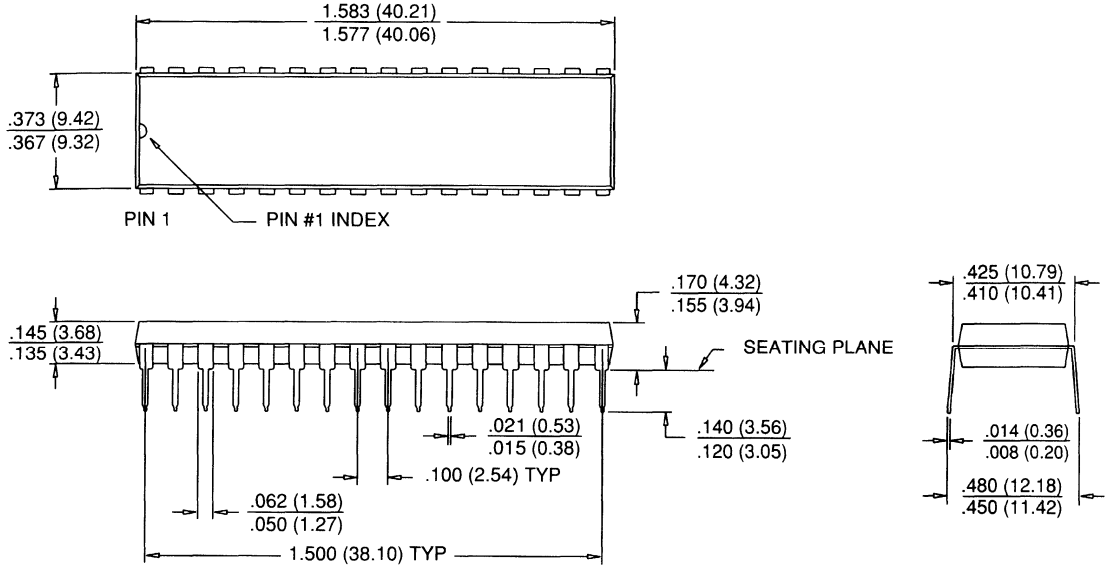


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC DIP

SA-7

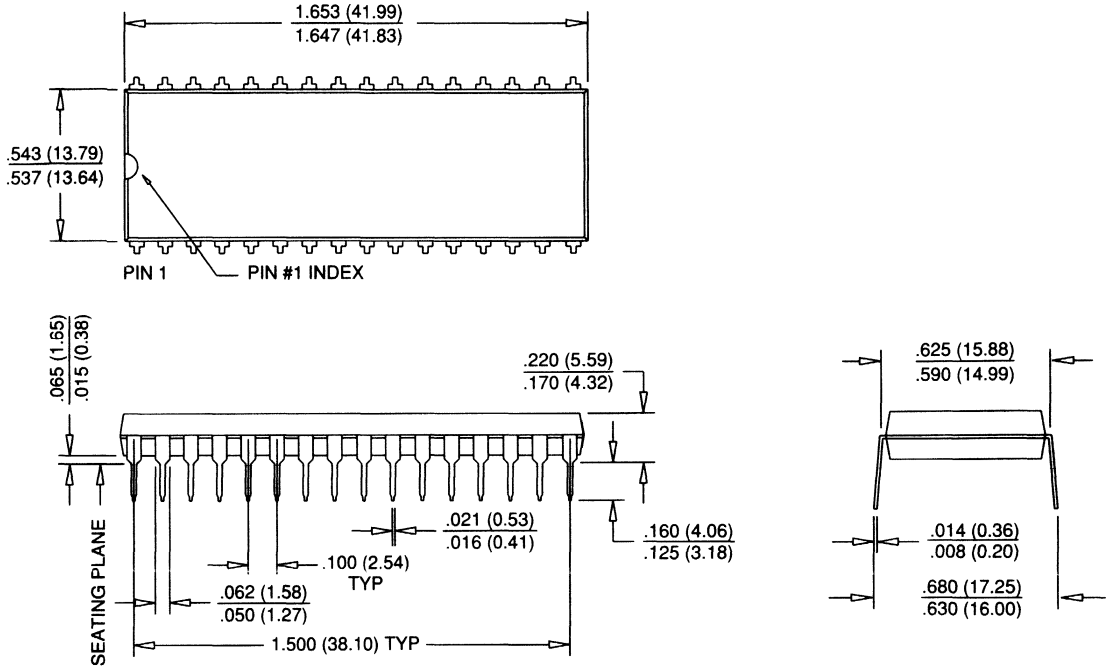


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

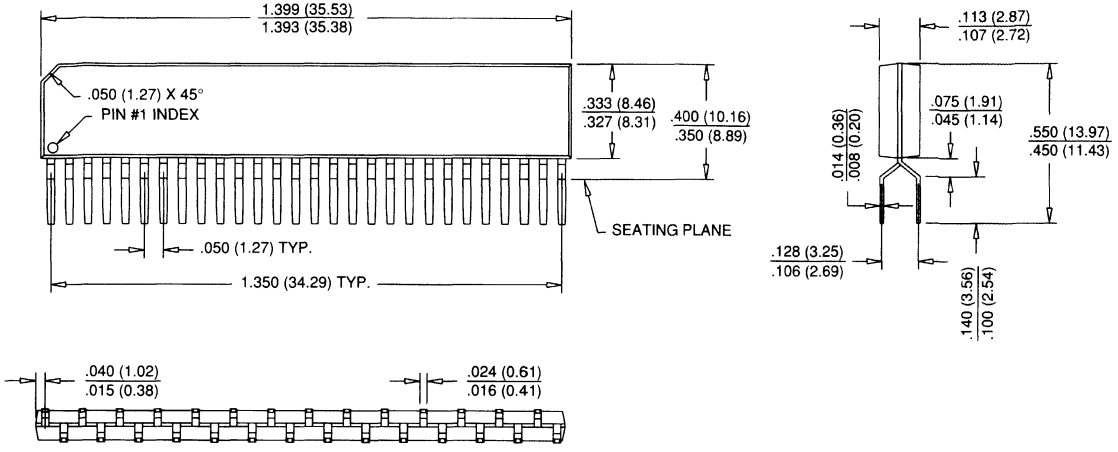
32-PIN PLASTIC DIP

SA-8



28-PIN PLASTIC ZIP

SB-1

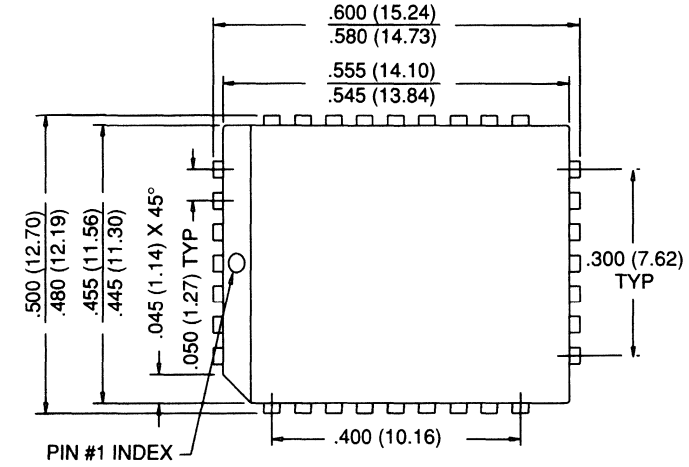


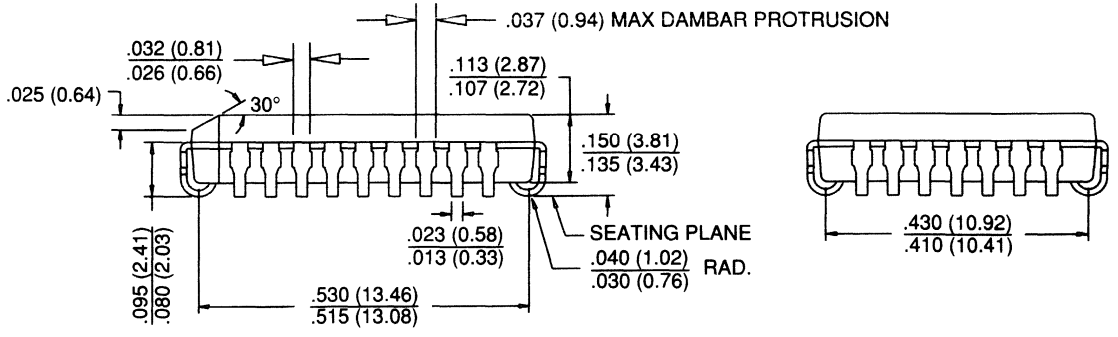
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLCC

SC-1



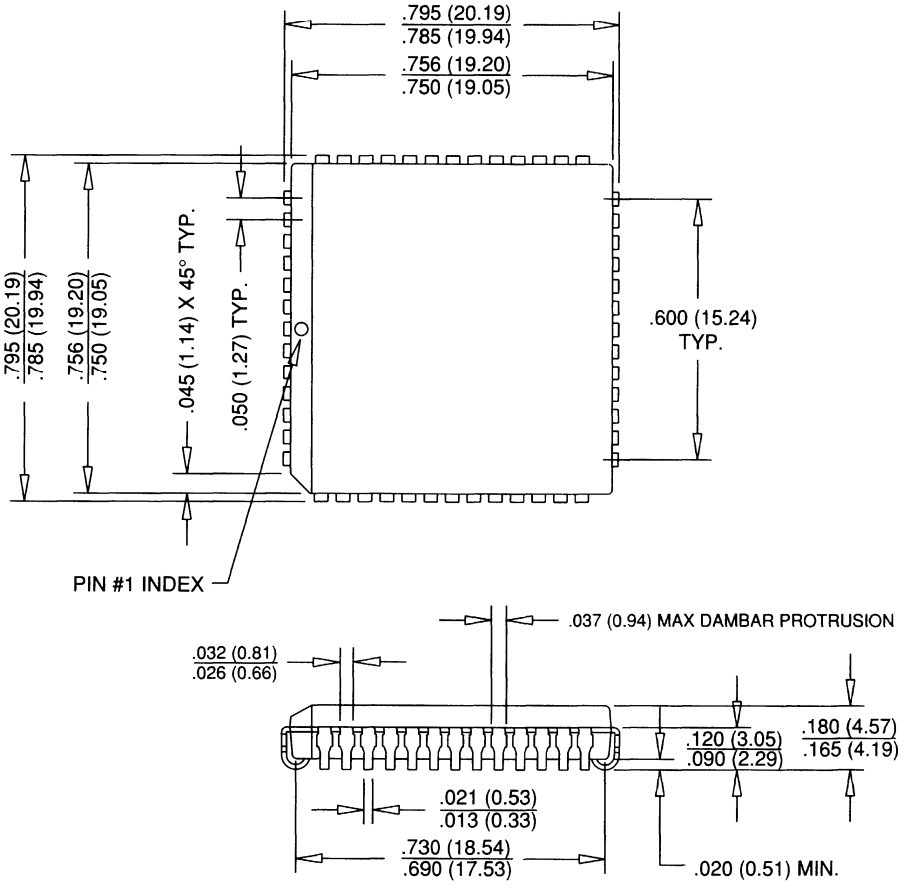


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

52-PIN PLCC

SC-2



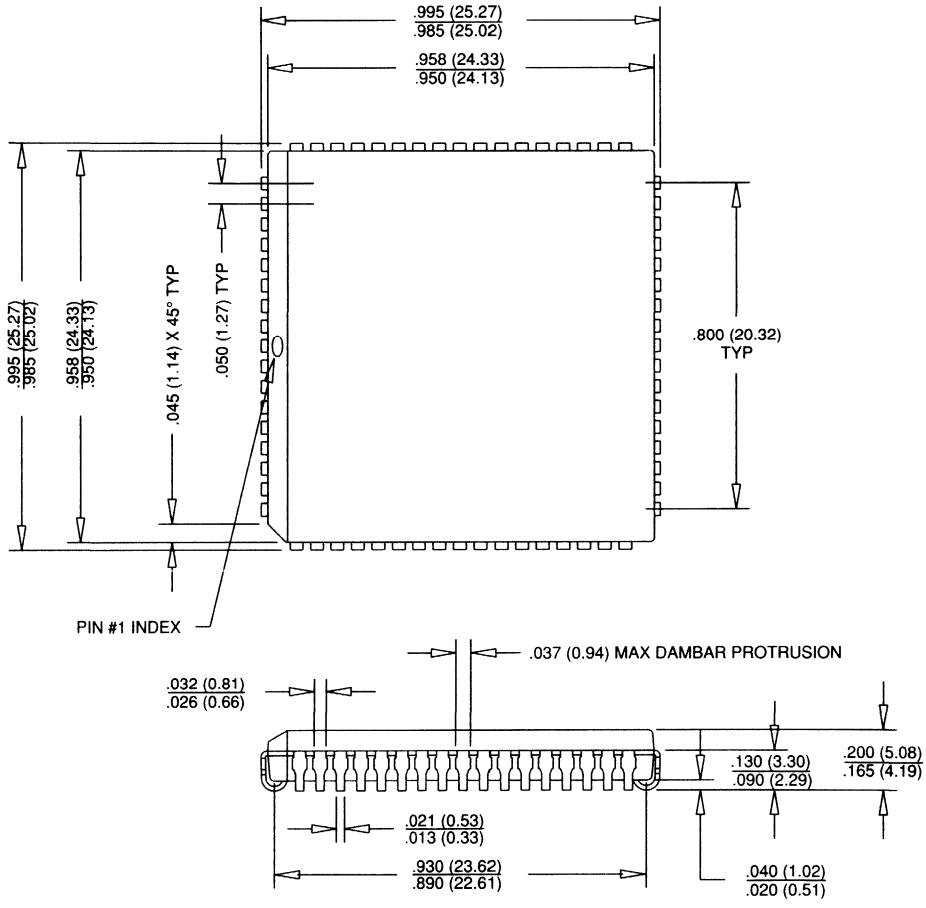
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

68-PIN PLCC

SC-3

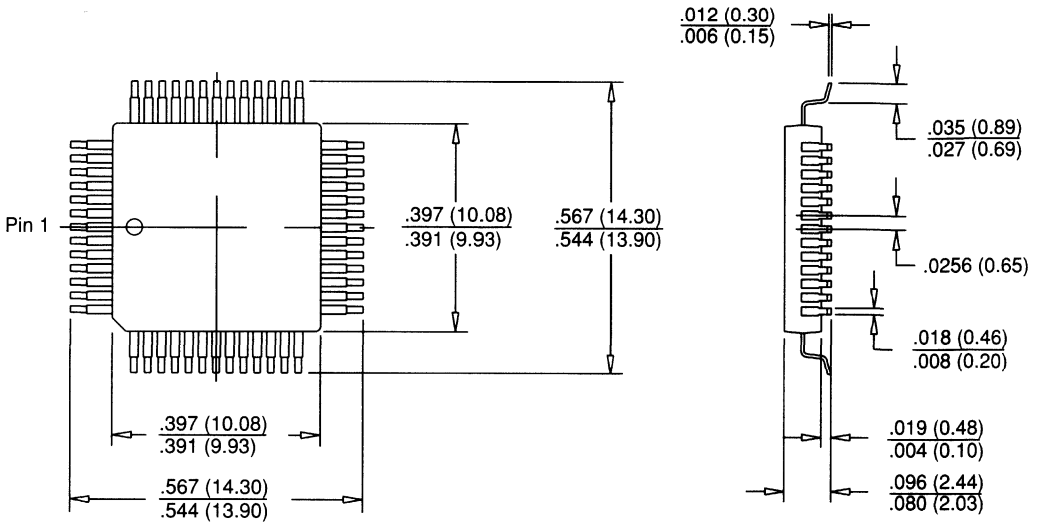


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

52-PIN PQFP

SC-4

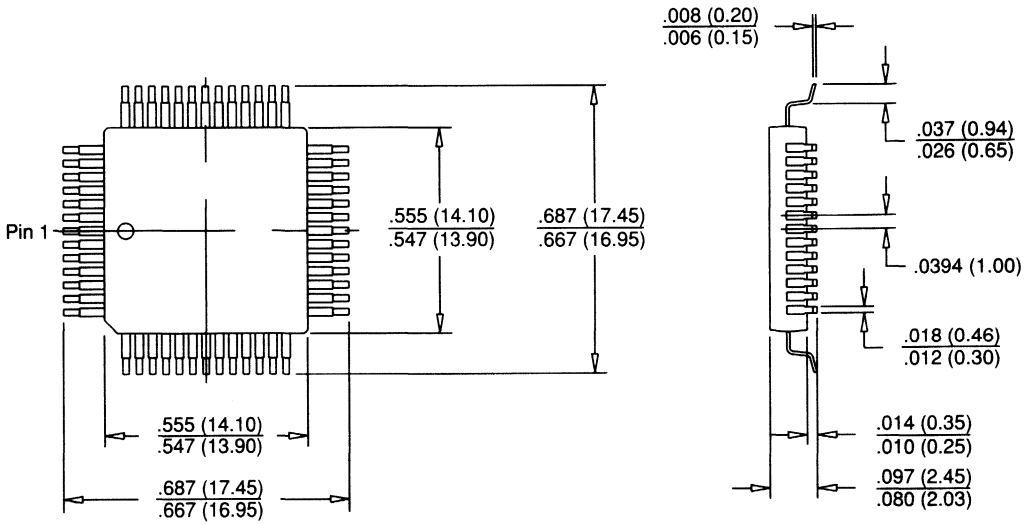


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

52-PIN PQFP

SC-5

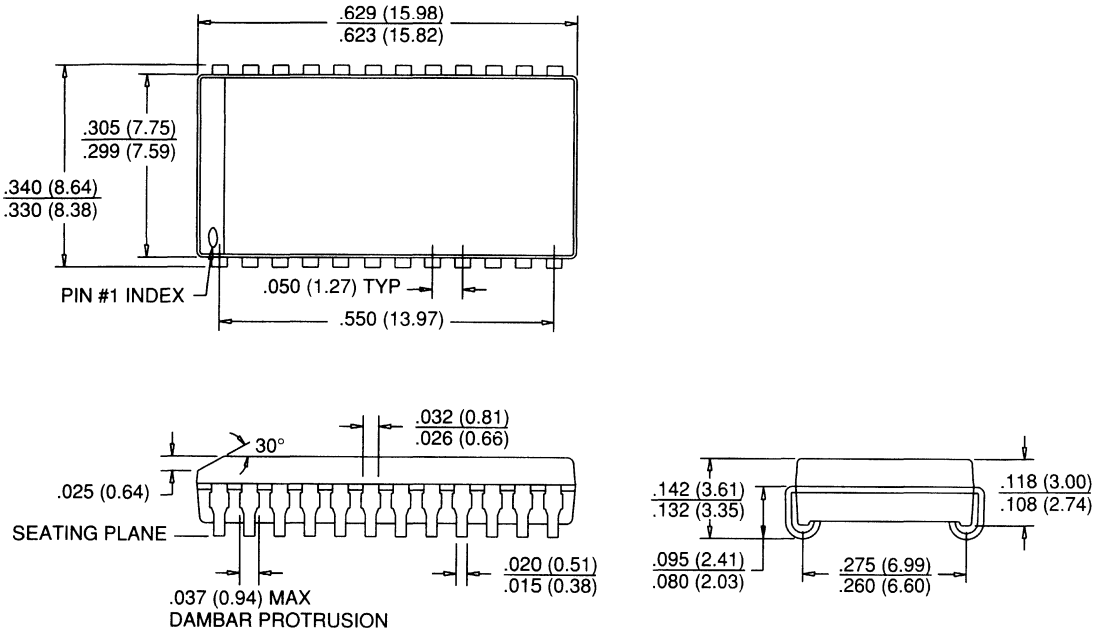


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC SOJ

SD-1



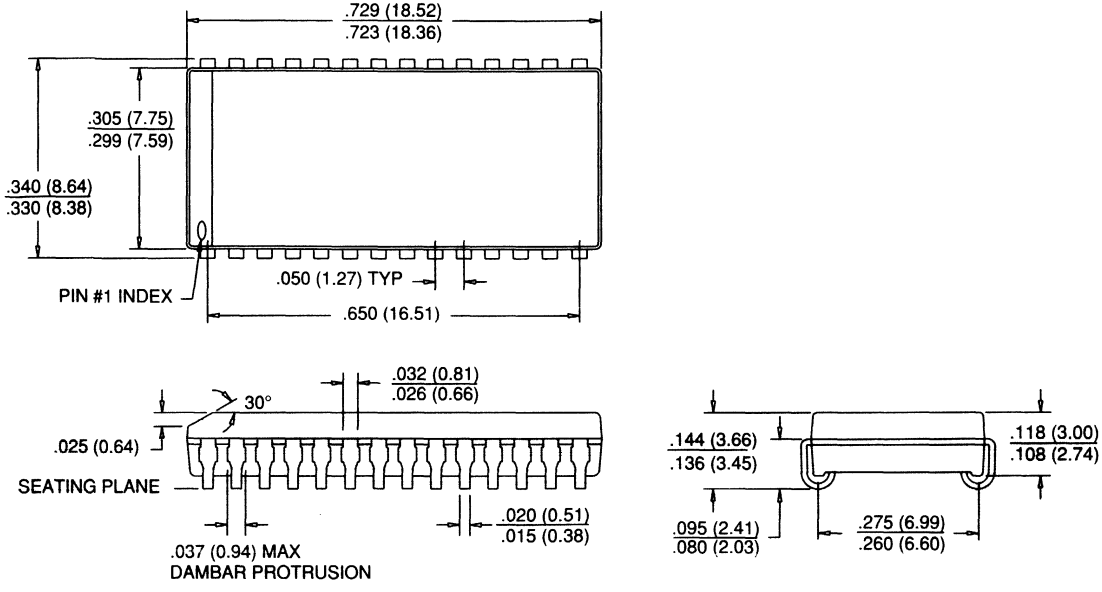
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

28-PIN PLASTIC SOJ

SD-2

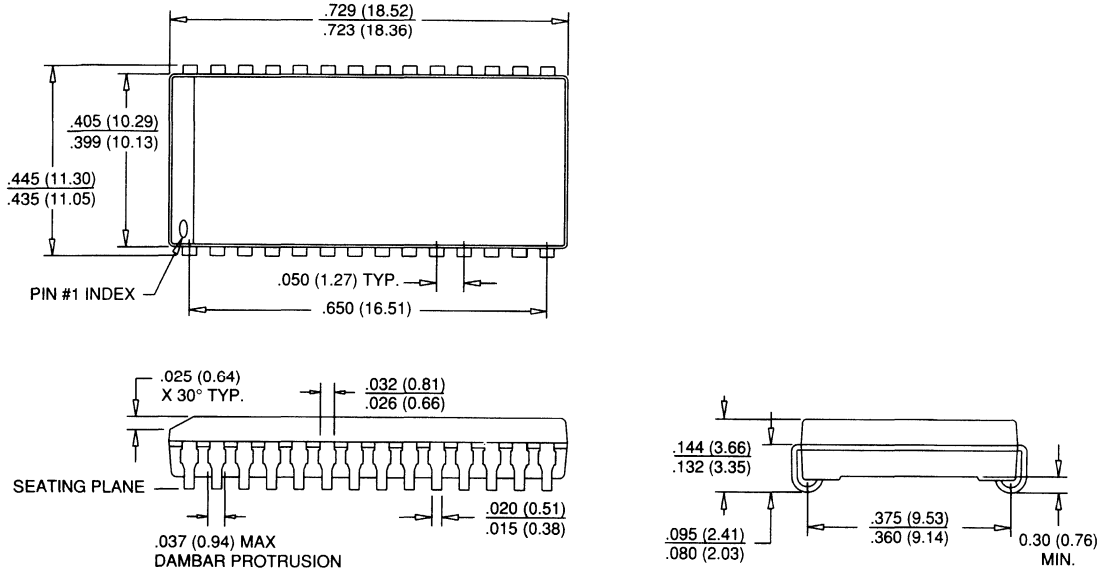


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SD-3



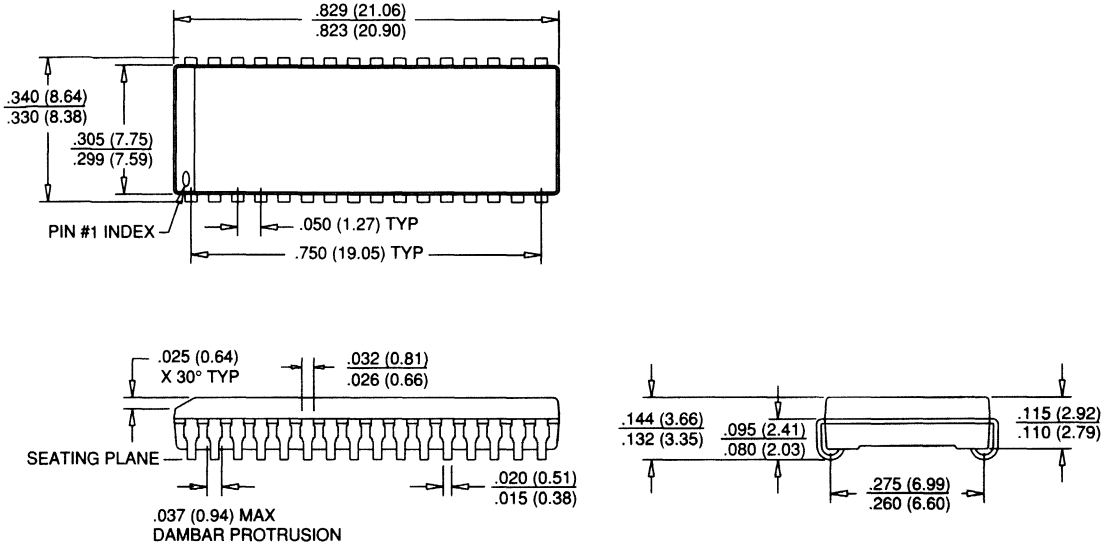
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

32-PIN PLASTIC SOJ

SD-4

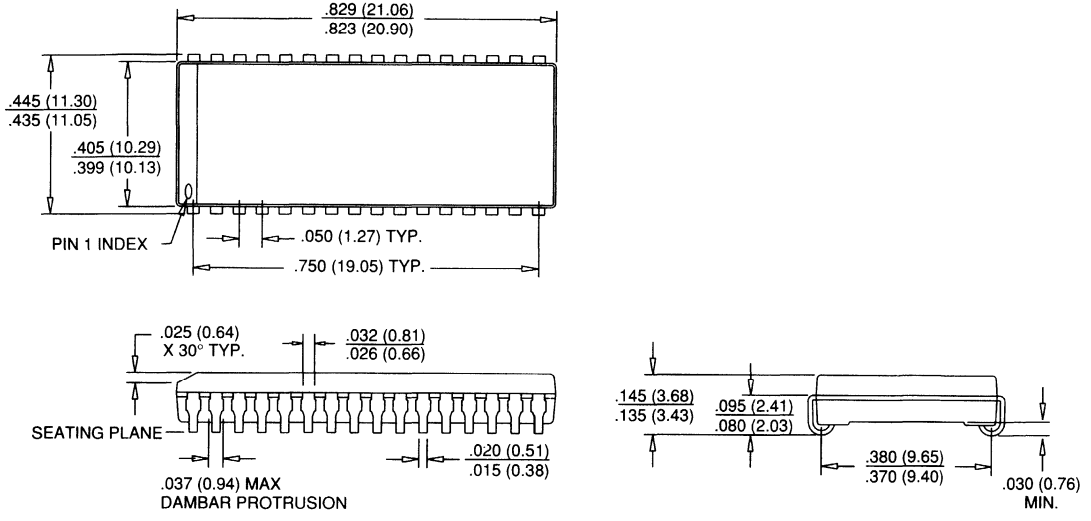


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC SOJ

SD-5



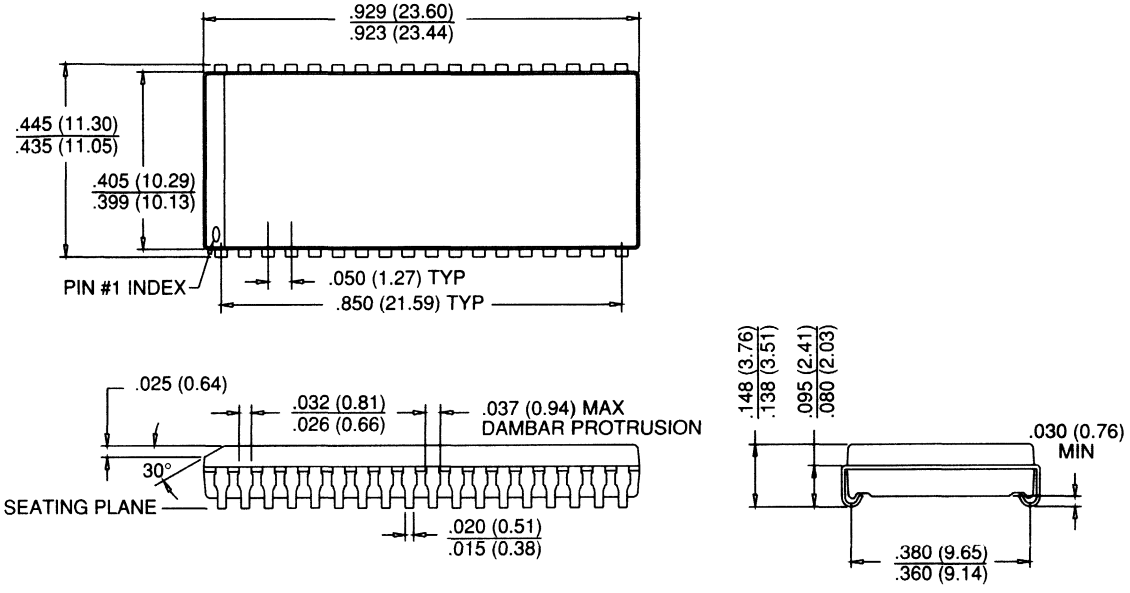
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

36-PIN PLASTIC SOJ

SD-6

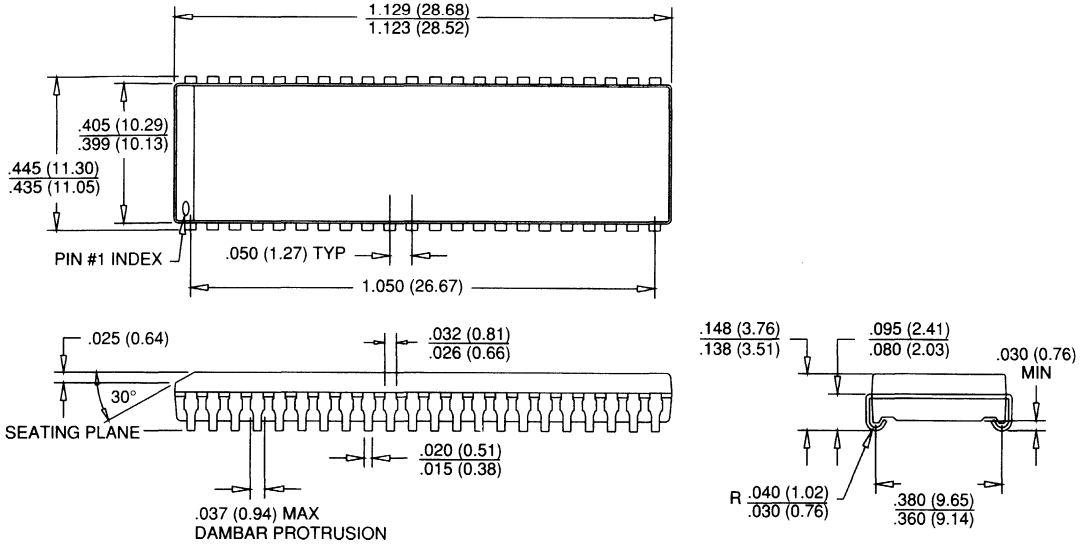


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

44-PIN PLASTIC SOJ

SD-7



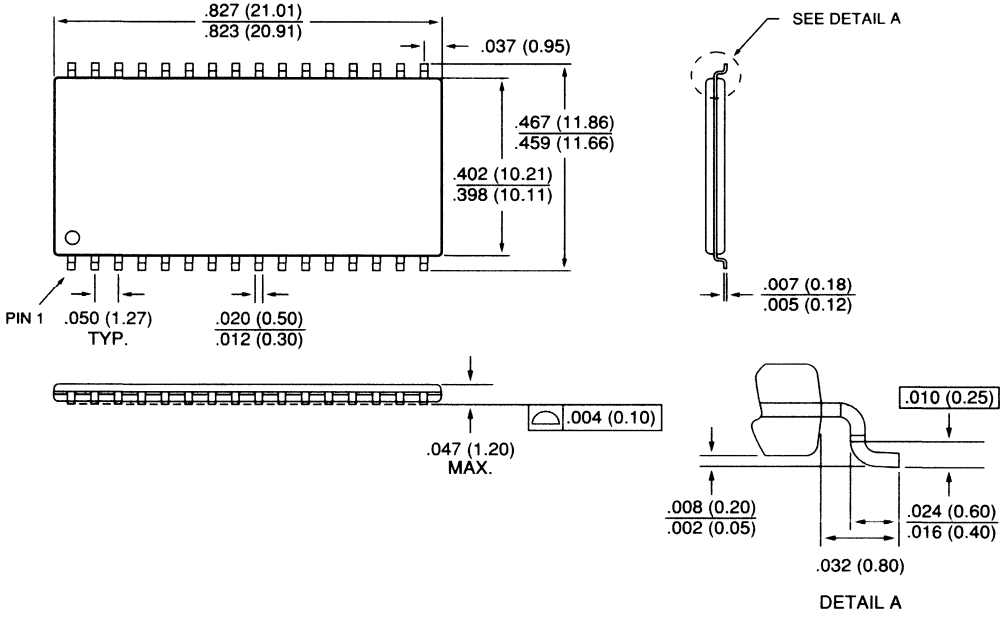
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC TSOP

SE-1



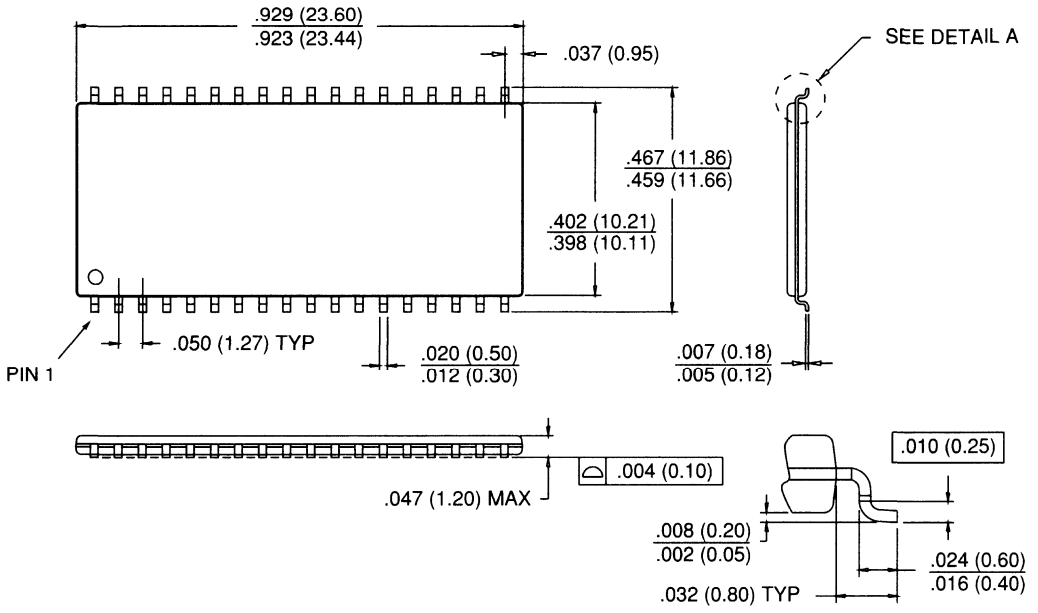
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

36-PIN PLASTIC TSOP

SE-2

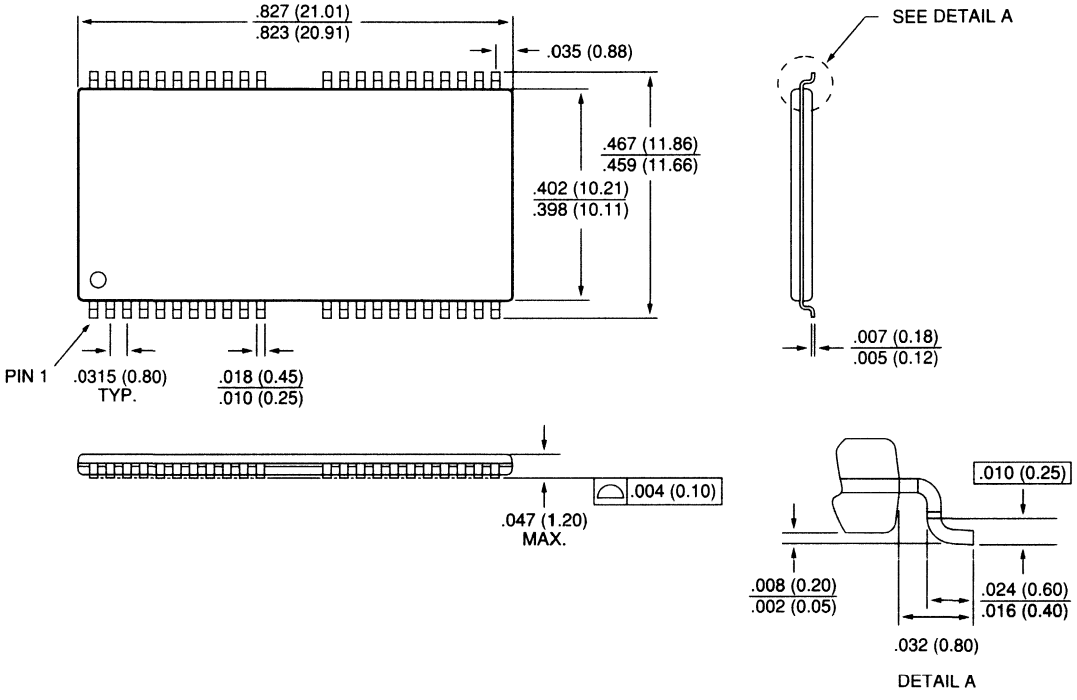


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

44/50-PIN PLASTIC TSOP

SE-3



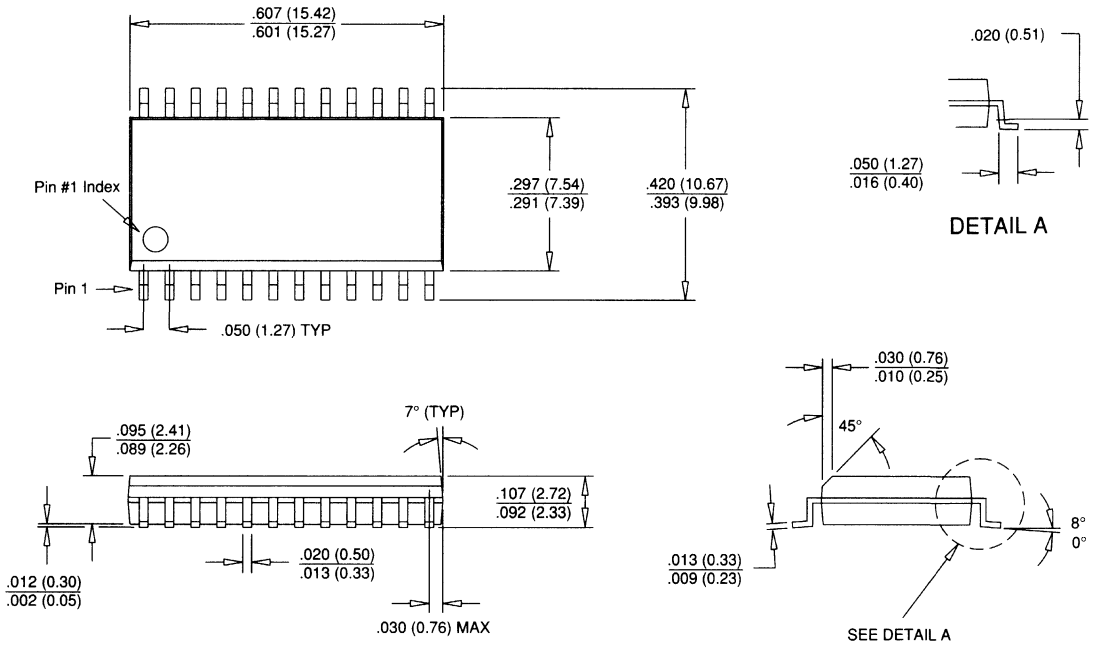
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

24-PIN PLASTIC SOIC

SF-1



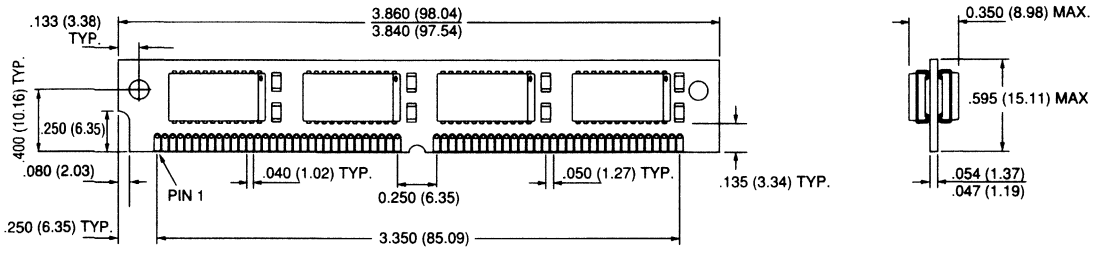
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

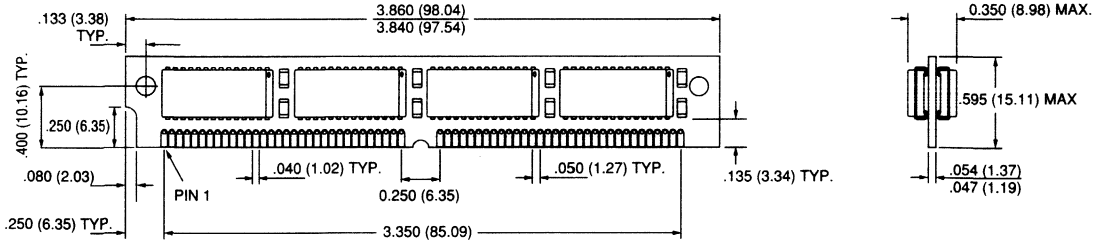
64-PIN MODULE SIMM

SG-1



64-PIN MODULE SIMM

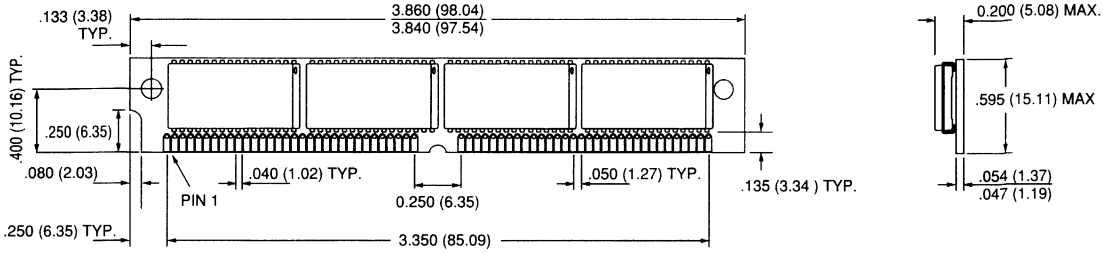
SG-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

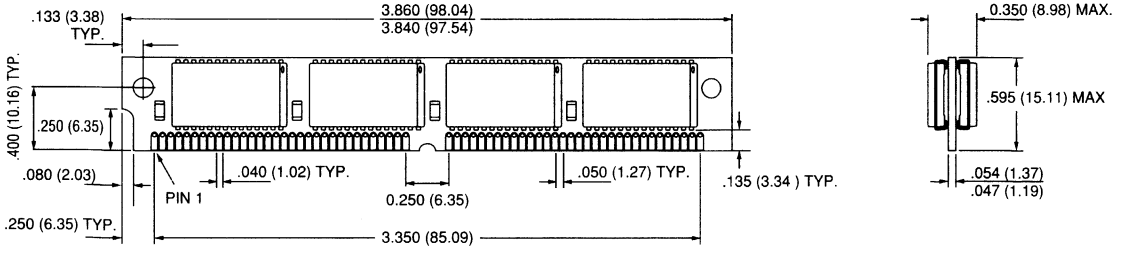
64-PIN MODULE SIMM

SG-3



64-PIN MODULE SIMM

SG-4

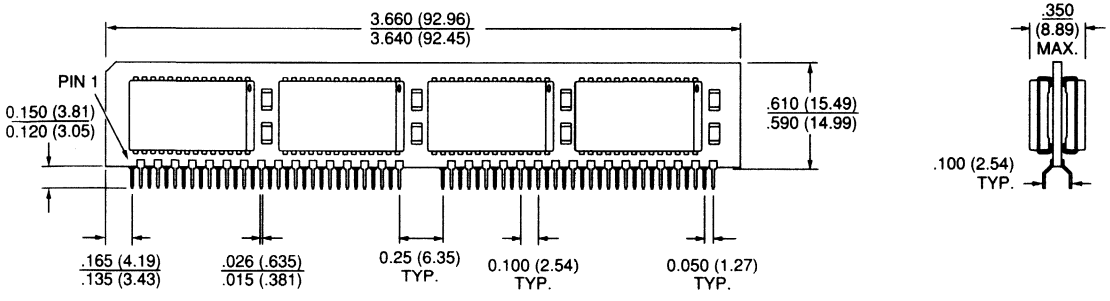


PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

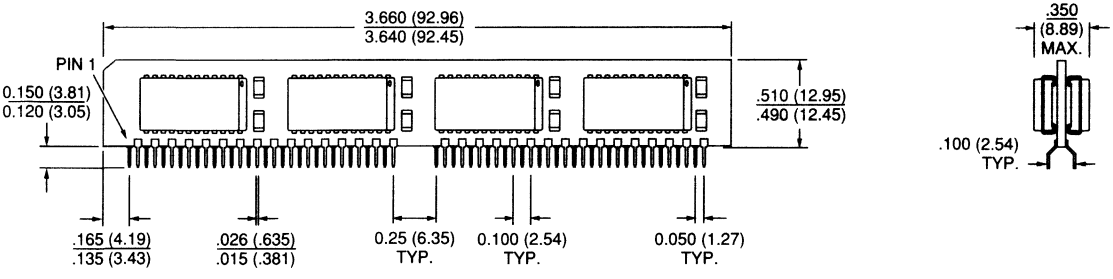
64-PIN MODULE ZIP

SH-1



64-PIN MODULE ZIP

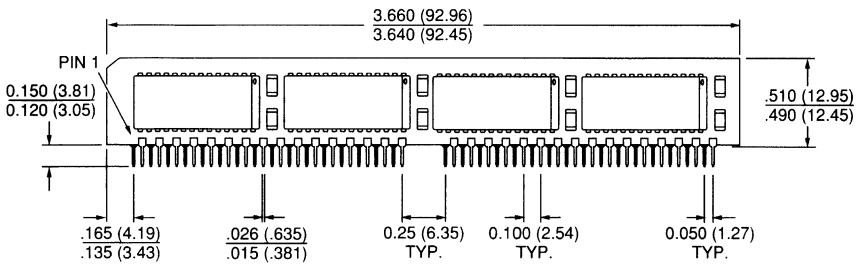
SH-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

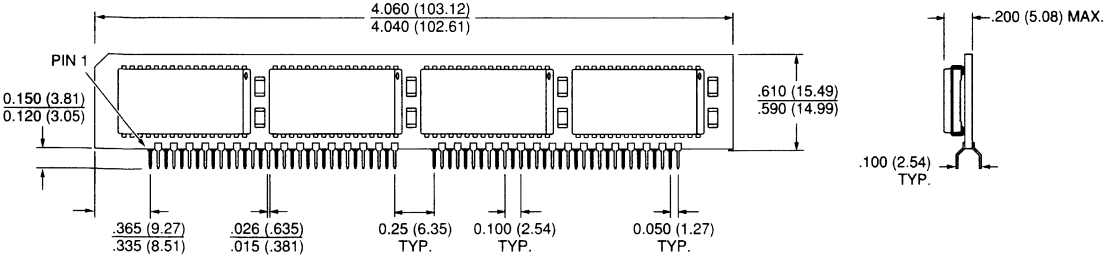
64-PIN MODULE ZIP

SH-3



64-PIN MODULE ZIP

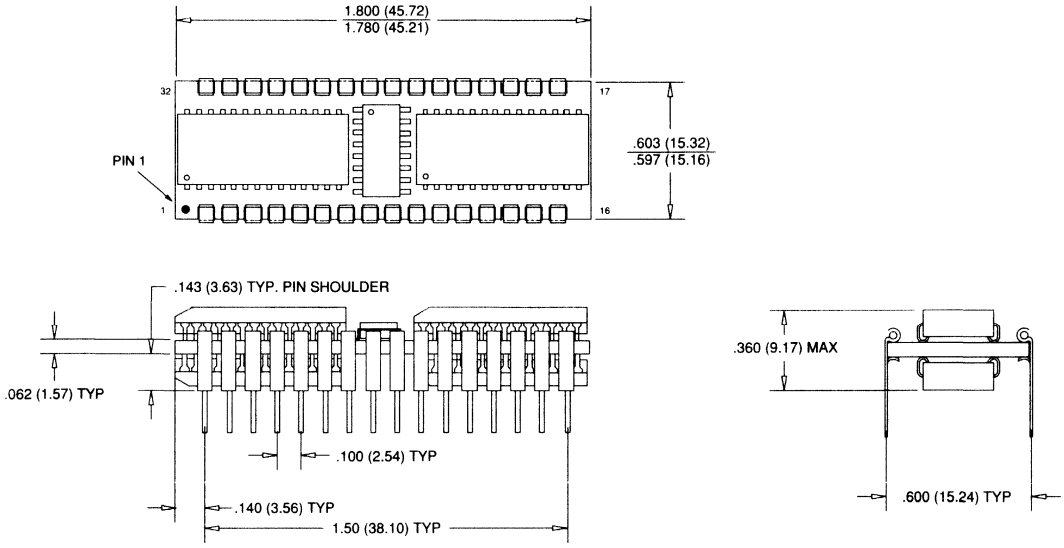
SH-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

32-PIN MODULE DIP

SI-1

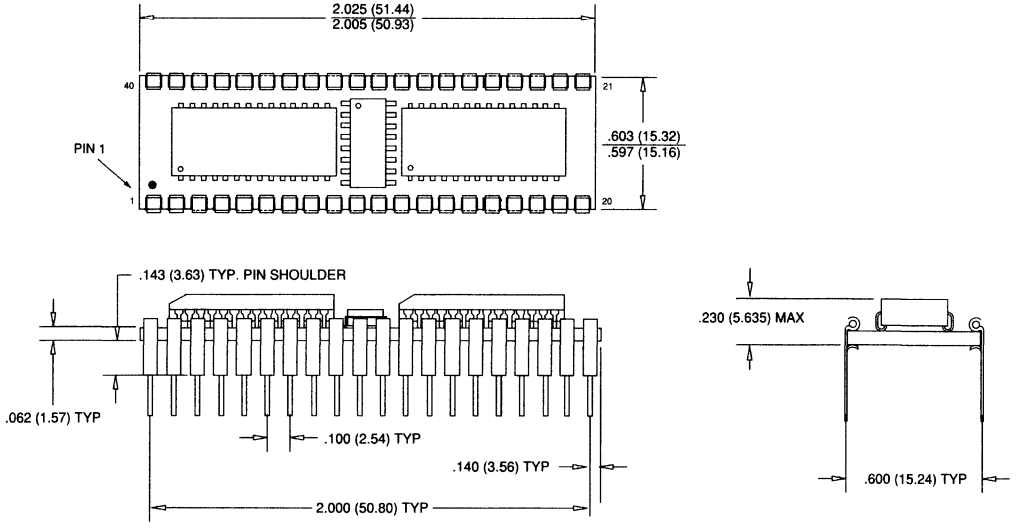


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

PACKAGE INFORMATION

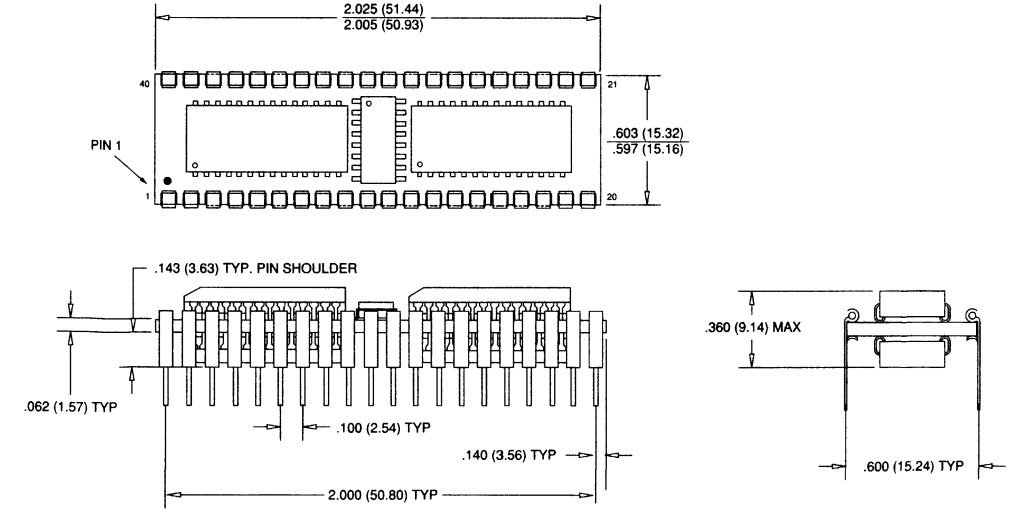
40-PIN MODULE DIP

SI-2



40-PIN MODULE DIP

SI-3



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MICRON

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Effective July 1, 1991, Micron implemented new standard bar coding labels that will accompany all shipments. These labels conform to EIA Standard 556.

Samples and tape-and-reel boxes will have their own individual bar code labels (see **CSN-02**). The bar code labels will allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar coding label.

BAR CODE INFORMATION

The information provided on the label is:

(S) — Serial: Individual box serial number
(13Q) — Special: Individual box number and total number of boxes in the shipment (example: 2 of 10)
(Q) — Quantity: Total quantity of parts in the box
(K) — Trans ID: Customer purchase order number
(P) — Customer Product ID: Customer part number. If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name: Customer's name and ship-to address
Ship-From-Name: Micron name and address
Lot Date Code: Indicates date of oldest lot in the box

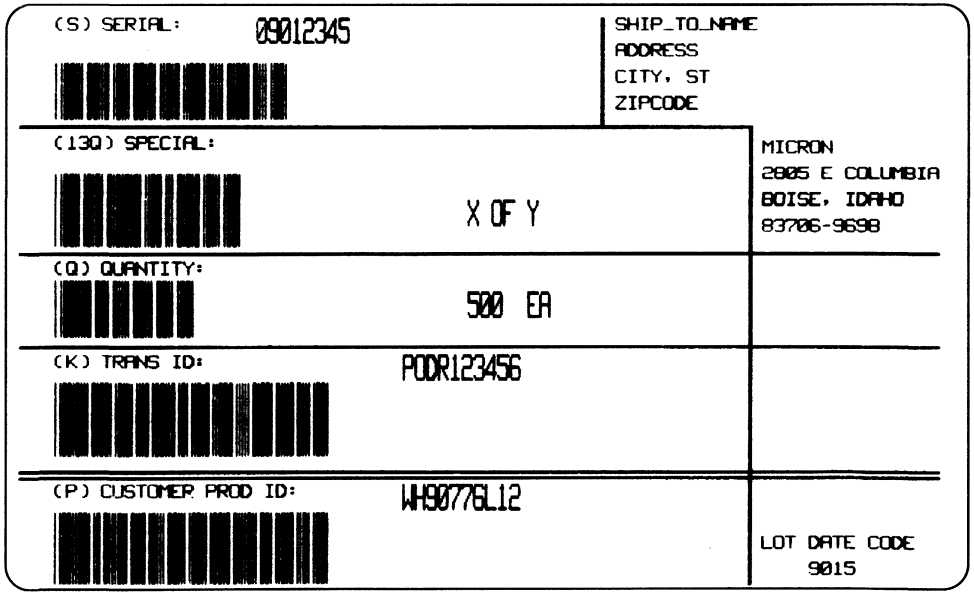


Figure 1
Standard Bar Code Label

SALES INFORMATION

CUSTOMER SERVICE NOTE

TAPE-AND-REEL/SAMPLE BAR CODE LABELS

INTRODUCTION

Micron provides a standard bar code label on each individual sample and tape-and-reel box. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multi-box shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*

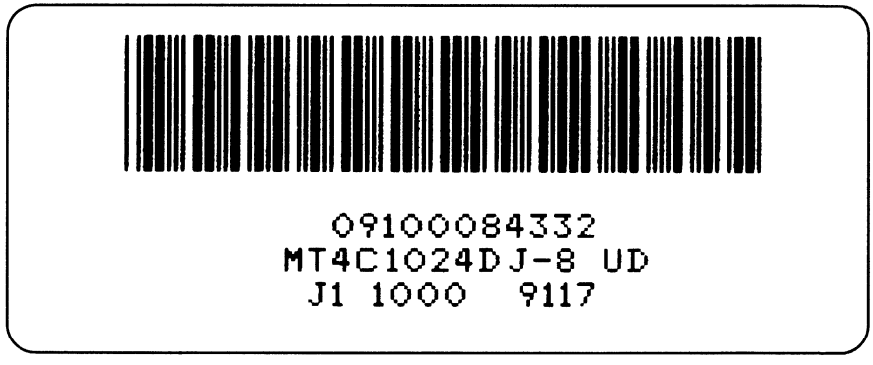
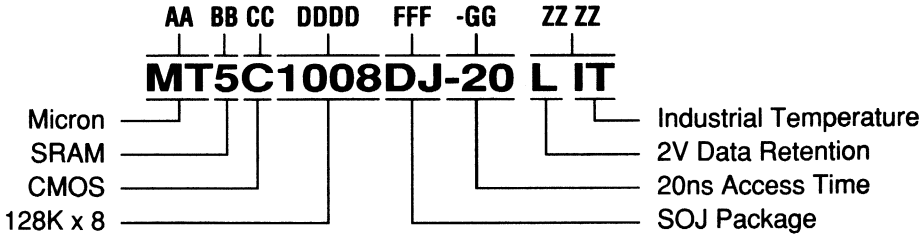


Figure 1
Label 1

*Indicates that more than one date code is contained on the reel.

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM (VRAM)	42
TPDRAM	43
SRAM	5
FIFO	52
Cache Data SRAM	56
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM	Width, Density
DPDRAM (VRAM)	Width, Density
TPDRAM	Width, Density
SRAM	Total Bits, Width
CACHE	Density, Width
Latched SRAM	Total Bits, Width
FIFO	Width, Total Bits
Synchronous SRAM	Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required)

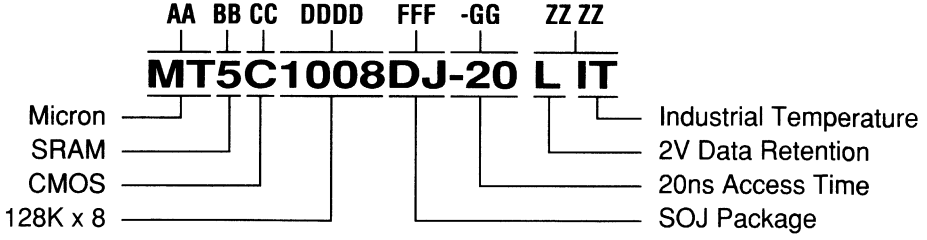
JEDEC Test Mode (4 Meg DRAM)	J
Errata on Base Part	Q

FFF – PACKAGE CODES

PLASTIC	
DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL
DIE	
Die	XDC†
Wafer	XWC†
Military Die	XDM†
Military Wafer	XWM†
Ceramic	
DIP	C
DIP (Narrow Body)	CN
DIP (Wide Body)	CW
LCC	EC
LCC (Narrow Body)	ECN
LCC (Wide Body)	ECW
SOP/SOIC	CG
SOJ	DCJ
PGA	CA
FLAT PACK	F

† A "1", "2" or "3" appears as part of the die identifier (e.g. XDM1.) A "1" indicates standard probe. A "2" indicates hot probe with speed grading. A "3" indicates that the die has been tested to meet all data sheet AC and DC parametrics as well as having gone through the full AMBYX® burn-in process.

CURRENT COMPONENT EXPANDED NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order).

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as: V L IT

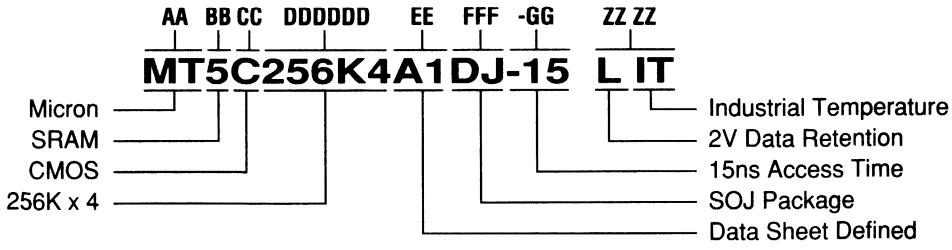
Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL

ZZ ZZ – PROCESSING CODES (continued)

Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP
Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape and Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

DRAM	4
DPDRAM (VRAM)	42
TPDRAM	43
Synchronous DRAM	48
SRAM	5
FIFO	52
Latched SRAM	56
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory

No Letter	Bits
K	Kilobits
M	Megabits
G	Gigabits

EE – DEVICE VERSIONS

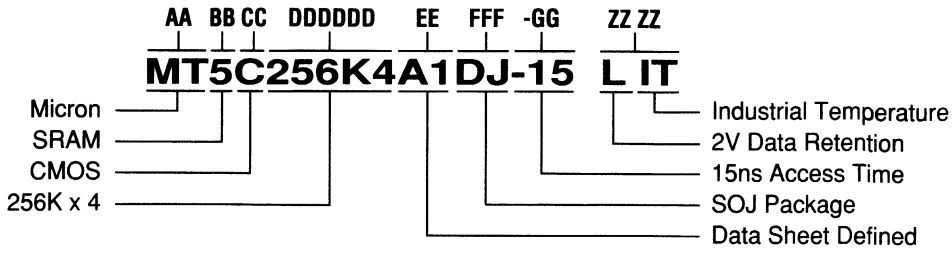
(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet

FFF – PACKAGE CODES

Plastic	
DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL
DIE	
Die	XDC†
Wafer	XWC†
Military Die	XDM†
Military Wafer	XWM†
CERAMIC	
DIP	C
DIP (Narrow Body)	CN
DIP (Wide Body)	CW
LCC (Narrow Body)	ECN
LCC	EC
LCC (Wide Body)	ECW
SOP/SOIC	CG
SOJ	DCJ
PGA	CA
FLAT PACK	F

† A "1", "2" or "3" appears as part of the die identifier (e.g. XDM1.) A "1" indicates standard probe. A "2" indicates hot probe with speed grading. A "3" indicates that the die has been tested to meet all data sheet AC and DC parametrics as well as having gone through the full AMBYX® burn-in process.

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as: V L IT

Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	VL

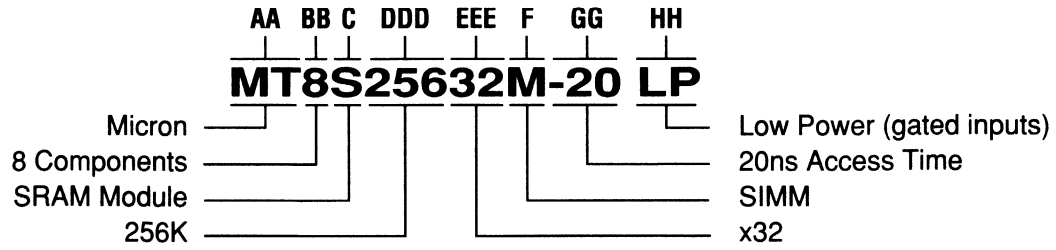
ZZ ZZ – PROCESSING CODES (continued)

Low Power (Self Refresh)	S
Low Voltage, Low Power (Self Refresh)	VS
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Low Voltage, Low Power	VP
Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape and Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

SALES INFORMATION

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – RAM FAMILY
- SRAM ..... S
- DRAM ..... D

DDD – DEPTH

EEE – WIDTH

F – PACKAGE CODE
- DIP ..... D
- ZIP ..... Z
- SIMM ..... M
- SIP ..... N
- Gold SIMM ..... G

GG – ACCESS TIME
- -10 ..... 10ns
- -12 ..... 12ns
- -15 ..... 15ns
- -20 ..... 20ns
- -25 ..... 25ns
- -30 ..... 30ns
- -35 ..... 35ns

HH – SPECIAL DESIGNATOR
- Low Volt, Data Retention L
- Low Power (gated inputs) ..... LP

ORDER INFORMATION*

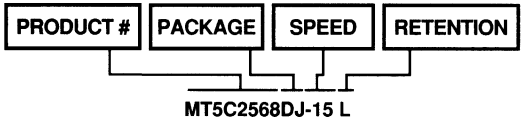
Each Micron component family is manufactured and quality controlled in the USA at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX® intelligent burn-in and test system.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's quality assured policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

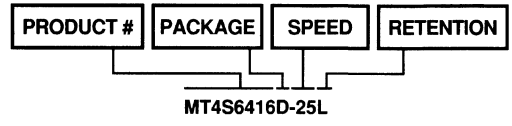
Telephone: (208) 368-3900
FAX: (208) 368-4431
Customer Comment Line:
(800) 932-4992 (USA)
01 (208) 368-3410 (Intl.)

ORDER EXAMPLES

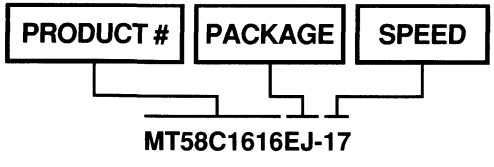
SRAM
32K x 8, 15ns in Plastic SOJ



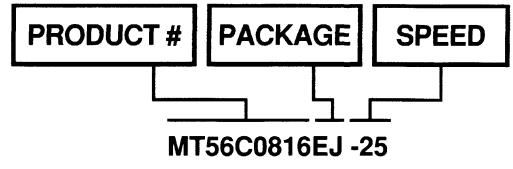
SRAM MODULE
64K x 16, 25ns in DIP Module with 2V Data Retention



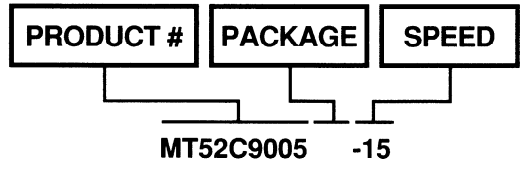
SYNCHRONOUS SRAM
16K x 16, 17ns in Plastic LCC



CACHE DATA SRAM
Dual 4K x 16, Single 8K x 16, 25ns in Plastic LCC



FIFO
512 x 9, 15ns DIP



*For more detailed information, refer to the Product Numbering charts on pages 12-5 through 12-9.

SALES INFORMATION

ALABAMA

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
Phone - 205-534-2376
FAX - 205-534-2384

Distributors

Hall-Mark Electronics Corporation
4890 University Square
Business Center, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
FAX - 205-830-2565

Hamilton/Avnet Electronics
4960 Corporate Drive, Suite 135
Huntsville, AL 35805
Phone - 205-837-7210
FAX - 205-721-0356

Pioneer Technology
4835 University Square, Suite 5
Huntsville, AL 35818
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
1750 West Broadway, Suite 114
Oviedo, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

ARIZONA

Representative

Quatra Associates
4645 South Lakeshore Drive, Suite 1
Tempe, AZ 85282
Phone - 602-820-7050
FAX - 602-820-7054

Distributors

Anthem Electronics Incorporated
1555 10th Place, Suite 101
Tempe, AZ 85281
Phone - 602-966-6600
FAX - 602-966-4826

Hamilton/Avnet Electronics
1626 South Edwards
Tempe, AZ 85281
Phone - 602-961-1211
FAX - 602-961-4555

Hall-Mark Electronics Corporation
4637 S. 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Wyle Laboratories
4141 E. Raymond Street, Suite 1
Phoenix, AZ 85040
Phone - 602-437-2088
FAX - 602-437-2124

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

ARKANSAS

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Distributors

Anthem Electronics, Inc.
651 N. Plano Road, Suite 429
Richardson, TX 75081
Phone - 214-238-7100
FAX - 214-238-0237

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
FAX - 214-343-5988

Hamilton/Avnet Electronics
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
FAX - 407-678-1878

Pioneer Electronics
13765 Beta Road
Dallas, TX 75244
Phone - 214-386-7300
FAX - 214-490-6419

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214- 235-9953
FAX - 214-644-5064

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

CALIFORNIA

Representatives (Northern California)

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315 W
San Jose, CA 95110
Phone - 408-452-8133
FAX - 408-452-8139

Bay Area Electronics Sales, Inc.
9119 Eden Oak Circle
Loomis, CA 95650
Phone - 916-652-6777
FAX - 916-652-5678

Representatives (Southern California)

Jones & McGeoy Sales, Incorporated
801 Parkcenter Drive, Suite 250
Santa Ana, CA 92705
Phone - 714-547-6466
FAX - 714-547-7670

Jones & McGeoy Sales, Incorporated
5060 Shoreham Place, Suite 200
San Diego, CA 92122
Phone - 619-458-5856
FAX - 619-453-0034s

Jones & McGeoy Sales, Incorporated
20501 Ventura Blvd., Suite 130
Woodland Hills, CA 91364
Phone - 818-715-7161
FAX - 818-715-7199

Distributors

Anthem Electronics Incorporated
1160 Ridder Park Drive
San Jose, CA 95131
Phone - 408-453-1200
FAX - 408-452-2281

Anthem Electronics Incorporated
9131 Oakdale Avenue
Chatsworth, CA 91311
Phone - 818-700-1000
FAX - 818-775-1302
Military FAX - 818-775-1814

Anthem Electronics Incorporated
1 Old Field Drive
East Irvine, CA 92718-2809
Phone - 714-768-4444
FAX - 714-768-6456

Anthem Electronics Incorporated
580 Menlo Drive, Suite 8
Rocklin, CA 95677
Phone - 916-624-9744
FAX - 916-624-9750

Anthem Electronics Incorporated
9369 Carroll Park Drive
San Diego, CA 92121
Phone - 619-453-9005
FAX - 619-546-7893

Hall-Mark Electronics Corporation
9420 Topanga Canyon Blvd.
Chatsworth, CA 91311
Phone - 818-773-4500
FAX - 818-773-4555

Hall-Mark Electronics Corporation
580 Menlo Drive, Suite 2
Rocklin, CA 95677
Phone - 916-624-9781
FAX - 916-961-0922

Hall-Mark Electronics Corporation
3878 Ruffin Road, Unit 10B
San Diego, CA 92123
Phone - 619-268-1201
FAX - 619-268-0209

Hall-Mark Electronics Corporation
2105 Lundy Avenue
San Jose, CA 95030
Phone - 408-432-4000
FAX - 408-432-4044

Hall-Mark Electronics Corporation
#1 Mauchly
Irvine, CA 92718
Phone - 714-727-6000
FAX - 714-727-6066

Hamilton/Avnet Electronics
3170 Pullman Street
Costa Mesa, CA 92626
Phone - 714-641-4100
FAX - 714-754-6033

Hamilton/Avnet Electronics
10950 Washington Blvd.
Culver City, CA 90232
Phone - 213-327-3693
FAX - 213-327-3794

Hamilton/Avnet Electronics
755 Sunrise Avenue, Suite 150
Roseville, CA 95661
Phone - 916-925-2216
FAX - 916-925-3478

Hamilton/Avnet Electronics
4545 Viewridge Avenue
San Diego, CA 92123
Phone - 619-571-1900
FAX - 619-571-8761

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, CA 94089
Phone - 408-743-3300
FAX - 408-745-6679

Hamilton/Avnet Electronics
21150 Califa Street
Woodland Hills, CA 91367
Phone - 818-594-0404
FAX - 818-594-8234

Pioneer Technologies
134 Rio Robles
San Jose, CA 95134
Phone - 408-954-9100
FAX - 408-954-9113

Pioneer Technologies
217 Technology Drive, Suite 110
Irvine, CA 92718
Phone - 714-753-5500
FAX - 714-753-5074

Wyle Laboratories
(Accounting Office Only)
128 Maryland Avenue
El Segundo, CA 90245
Phone - 213-322-1763
FAX - 213-322-1763

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
FAX - 408-727-5896

Wyle Laboratories
17872 Cowan Avenue
Irvine, CA 92714
Phone - 714-863-9953
FAX - 714-863-0473

Wyle Laboratories
2951 Sunrise Blvd., Suite 175
Rancho Cordova, CA 95742
Phone - 916-638-5282
FAX - 916-638-1491

Wyle Laboratories
9525 Chesapeake Drive
San Diego, CA 92123
Phone - 619-565-9171
FAX - 619-565-0512

Wyle Laboratories
26010 Mureau Road, Suite 150
Calabasas, CA 91302
Phone - 818-880-9000
FAX - 818-880-5510

Military Distributors

Anthem Electronics Incorporated
9131 Oakdale Avenue
Chatsworth, CA 91311
Phone - 818-700-1000
FAX - 818-775-1814

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
22700 Savi Ranch Parkway
Yorba Linda, CA 92686
Phone - 714-921-9000
FAX - 714-921-2715

Zeus Components, Inc.
5236 Colony Drive, Suite 102
Agoura Hills, CA 91301
Phone - 818-889-3838
FAX - 818-889-2464

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

CANADA

Representatives

Clark-Hurman Associates
20 Regan Road, Unit 14
Brampton, Ontario L7A 1C3
Phone - 416-840-6066
FAX - 416-840-6091

Clark-Hurman Associates
66 Colonnade Road, Suite 205
Nepean, Ontario K2E 7K7
Phone - 613-727-5626
FAX - 613-727-1707

Clark-Hurman Associates
4 Chester
Pointe Claire, Quebec H9R 4H7
Phone - 514-426-0453
FAX - 514-426-0455

Davetek Marketing
107-3738 North Fraser Way
Burnaby, BC V5J 5G1
Phone 604-430-3680
FAX - 604-435-5490

Distributors

Hamilton/Avnet Electronics
8610 Commerce Court
Burnaby, BC V5A 4N6
Phone - 604-420-4101
FAX - 604-420-5376

Hamilton/Avnet Electronics
151 Superior Blvd., Unit 1-6
Mississauga, Ontario L5T 2L1
Phone - 416-564-6060
FAX - 416-564-6036

Hamilton/Avnet Electronics
190 Colonnade Road
Nepean, Ontario K2E 7J5
Phone - 613-226-1700
FAX - 613-226-1184

Hamilton/Avnet Electronics
2795 Rue Halpern
St. Laurent, Quebec H4S 1P8
Phone - 514-335-1000
FAX - 514-335-2481

Semad Electronic
85 Spy Court
Markham, Ontario L3R 4Z4
Phone - 416-475-3922
FAX - 416-475-4158

Semad Electronic
1825 Woodward Drive
Ottawa, Ontario K2C OR3
Phone - 613-727-8325
FAX - 613-727-9489

Semad Electronic
8563 Government Street
Burnaby, B.C. V3N 4S9
Phone - 604-420-9889
FAX - 604-420-0124

Semad Electronic
243 Place Frontenac
Pointe Claire, PQ H9R 4Z7
Phone - 514-694-0860
FAX - 514-694-0965

Semad Electronic
6120 3rd Street S.E., Unit 9
Calgary, Alberta T2H 1K4
Phone - 403-252-5664
FAX - 403-255-0966

COLORADO

Representative

Wescom Marketing
4891 Independence Street
Wheatridge, CO 80033
Phone - 303-422-8957
FAX - 303-422-9892

Distributors

Anthem Electronics Incorporated
373 Inverness Drive
Englewood, CO 80112
Phone - 303-790-4500
FAX - 303-790-4532

Hall-Mark Electronics Corporation
12503 E. Euclid Drive, Suite 20
Englewood, CO 80111
Phone - 303-790-1662
FAX - 303-790-4991

Hamilton/Avnet Electronics
9605 Maroon Circle, Suite 200
Englewood, CO 80112
Phone - 303-799-7800
FAX - 303-799-7801

Wyle Laboratories
451 E. 124th Street
Thornton, CO 80241
Phone - 303-457-9953
FAX - 303-457-4831

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

CONNECTICUT

Representative

Advanced Tech Sales Incorporated
Westview Office Park
Building 2, Suite 1C
850 N. Main Street Extension
Wallingford, CT 06492
Phone - 203-284-0838
FAX - 203-284-8232

Distributors

Anthem Electronics
61 Mattatuck Heights
Waterbury, CT 06705
Phone - 203-575-1575
FAX - 203-596-3232

Hall-Mark Electronics Corporation
125 Commerce Court, Unit 6
Cheshire, CT 06410
Phone - 203-271-2844
FAX - 203-272-1704

Hamilton/Avnet Electronics
Stillriver Corporate Center
55 Federal Road, Suite 103
Dansburry, CT 06810
Phone - 203-743-6077
FAX - 203-791-9050

Pioneer Standard
112 Main Street
Norwalk, CT 06851
Phone - 203-853-1515
FAX - 203-838-9901

Military Distributor

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

DELAWARE

Representative

Omega Electronic Sales Incorporated
2655 Interplex Drive, Suite 104
Trevose, PA 19053
Phone - 215-244-4000
FAX - 215-244-4104

Distributor

Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
FAX - 215-674-3107

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

DISTRICT OF COLUMBIA

Representative

Electronic Engineering & Sales, Inc.
305 Kramer Road
Pasadena, MD 21122
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics, Inc.
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Hamilton/Avnet Electronics
7172 Gateway Drive
Columbia, MD 21046
Phone - 301-621-8410
FAX - 301-995-3593

Pioneer Technologies
9100 Gaither Road
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

FLORIDA

Representatives

Photon Sales, Inc.
1600 Sarno Road, Suite 21
Melbourne, FL 32935
Phone - 407-259-8999
FAX - 407-259-1323

Photon Sales, Inc.
715 Florida Street
Orlando, FL 32806
Phone - 407-896-6064
FAX - 407-896-6197

Photon Sales, Inc.
11210 Garfield Court
Seffner, FL 33584
Phone - 813-689-6751
FAX - 813-689-6811

Photon Sales, Inc.
3475 B. East Bay Drive
Largo, FL 34641
Phone - 813-531-2272
FAX - 813-536-4599

Distributors

Anthem Electronics Incorporated
2555 Enterprise Road, Suite 11-2
Clearwater, FL 34623
Phone - 813-797-2900
FAX - 813-796-4880

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
FAX - 407-290-0164

Hall-Mark Electronics Corporation
10491 72nd Street North, Suite 303
Largo, FL 34647
Phone - 813-541-7440
FAX - 813-544-4394

Hall-Mark Electronics Corporation
3161 Southwest 15th Street
Pompano Beach, FL 33069-4806
Phone - 305-971-9280
FAX - 305-971-9339

Hall-Mark Electronics Corporation
489 E. Semoran Blvd., Suite 145
Casselberry, FL 32707
Phone - 407-830-5855
FAX - 407-767-5002

Hamilton/Avnet Electronics
5371 N.W. 33rd Avenue, Suite 204
Ft. Lauderdale, FL 33309
Phone - 305-767-6377
FAX - 305-767-6406

Hamilton/Avnet Electronics
3247 Tech Drive North
St. Petersburg, FL 33716
Phone - 813-573-3930
FAX - 813-572-4329

Hamilton/Avnet Electronics
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
FAX - 407-678-1878

Pioneer Technologies
337 South-North Lake, Suite 1000
Altamonte Springs, FL 32701
Phone - 407-834-9090
FAX - 407-834-0865

Pioneer Technologies
674 S. Military Trail
Deerfield Beach, FL 33442
Phone - 305-428-8877
FAX - 305-481-2950

Military Distributor

Zeus Components, Inc.
285 Cantrell Parkway, Suite 1730
Altamonte Springs, FL 32714
Phone - 407-788-9100
FAX - 407-788-0981

GEORGIA

Representative

Southeast Technical Group
2620 Deer Isle Cove
Lawrenceville, GA 30244
Phone - 404-979-2055
FAX - 404-979-2055

Distributors

Hall-Mark Electronics Corporation
3425 Corporate Way, Suite A
Duluth, GA 30136-2552
Phone - 404-623-4400
FAX - 404-476-8806

Hamilton/Avnet Electronics
3425 Corporate Way, Suite G
Duluth, GA 30136
Phone - 404-446-0611
FAX - 404-446-1011

Pioneer Technologies
4250 C Rivergreen Parkway
Duluth, GA 30136
Phone - 404-623-1003
FAX - 404-623-0665

Military Distributor

Zeus Components, Inc.
1750 West Broadway, Suite 114
Oveido, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

HAWAII

Representatives

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315
San Jose, CA 95110
Phone - 408-452-8133
FAX - 408-452-8139

Bay Area Electronics Sales, Inc.
5711 Reinhold Street
Fair Oaks, CA 95628
Phone - 916-863-0563
FAX - 916-863-0615

Distributors

Anthem Electronics Incorporated
1160 Ridder Park Drive
San Jose, CA 95131
Phone - 408-453-1200
FAX - 408-452-2281

Hall-Mark Electronics Corporation
2105 Lundy Avenue
San Jose, CA 95030
Phone - 408-432-4000
FAX - 408-432-4044

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
FAX - 408-727-5896

IDAHO

Representative

Contact Micron
Component Sales
Phone - 208-368-3900

Distributors

Anthem Electronics, Inc.
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Corporation
12503 E. Euclid Drive, Suite 20
Englewood, CO 80111
Phone - 303-790-1662
FAX - 303-790-4991

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, CA 94089
Phone - 408-743-3300
FAX - 408-745-6679

Wyle Laboratories
1325 West 2200 South, Suite E
West Valley, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

ILLINOIS

Representatives

Advanced Technical Sales
13755 St. Charles Rock Road
Bridgeton, MO 63044
Phone - 314-291-5003
FAX - 314-291-7958

Industrial Representatives, Inc.
8430 Gross Point Road
Skokie, IL 60077
Phone - 708-967-8430
FAX - 708-967-5903

Distributors

Anthem Electronics Incorporated
1300 Remington, Suite A
Schaumburg, IL 60173
Phone - 708-884-0200
FAX - 708-884-0480

Hall-Mark Electronics Corporation
210 Mittel Drive
Wooddale, IL 60191
Phone - 708-860-3800
FAX - 708-860-0239

Hamilton/Avnet Electronics
1130 Thorndale Avenue
Bensenville, IL 60106
Phone - 708-860-7700
FAX - 708-860-8530

Pioneer Standard
2171 Executive Drive, Suite 200
Addison, IL 60101
Phone - 708-495-9680
FAX - 708-495-9831

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

INDIANA

Representatives

Scott Electronics, Inc. (S. Indiana)
7321 Shadeland Station, Suite 256
Indianapolis, IN 46256
Phone - 317-841-0010
FAX - 317-841-0107

Scott Electronics, Inc. (N. Indiana)
Lima Valley Office Village
8109 Lima Road
Fort Wayne, IN 46818
Phone - 219-489-5690
FAX - 219-489-1842

Distributors

Hall-Mark Electronics Corporation
4275 W. 96th Street
Indianapolis, IN 46268
Phone - 317-872-8875
FAX - 317-876-7165

Hamilton/Avnet Electronics
655 West Carmel Drive, Suite 160
Carmel, IN 46032
Phone - 317-844-9333
FAX - 317-844-5921

Pioneer Standard
9350 N. Priority Way, West Drive
Indianapolis, IN 46240
Phone - 317-573-0880
FAX - 317-573-0979

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

IOWA

Representative

Advanced Technical Sales
375 Collins Road N.E.
Cedar Rapids, IA 52402
Phone - 319-393-8280
FAX - 319-393-7258

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Drive, Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
210 Mittel Drive
Wooddale, IL 60191
Phone - 708-860-3800
FAX - 708-860-0239

Hamilton/Avnet Electronics
2335-A Blairs Ferry Road, N.E.
Cedar Rapids, IA 52402
Phone - 319-393-7050
FAX - 319-362-4757

Pioneer Standard
7625 Golden Triangle Drive
Eden Prarie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

KANSAS

Representative

Advanced Technical Sales
601 N. Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
FAX - 913-782-8641

Distributors

Hall-Mark Electronics Corporation
10809 Lakeview Avenue
Lenexa, KS 66215
Phone - 913-888-4747
FAX - 913-888-0523

Hamilton/Avnet Electronics
15313 West 95th Street
Lenexa, KS 66219
Phone - 913-888-8900
FAX - 913-541-7951

Pioneer Electronics
111 Westport Plaza, Suite 625
St. Louis, MO 63146
Phone - 314-542-3077
FAX - 314-542-3078

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

KENTUCKY

Representative

Scott Electronics, Inc.
10901 Reed-Hartman Hwy., Suite 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
FAX - 513-791-8059

Distributors

Hall-Mark Electronics Corporation (E. Ky.)
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Hall-Mark Electronics Corporation (W. Ky.)
4275 W. 96th Street
Indianapolis, IN 46268
Phone - 317-872-8875
FAX - 317-876-7165

Hamilton/Avnet Electronics
1847 Mercer Road, Suite G
Lexington, KY 40511
Phone - 606-259-1475
FAX - 606-288-4936

Pioneer Standard (W. Ky.)
9350 N. Priority Way, W. Drive
Indianapolis, IN 46240
Phone - 317-573-0880
FAX - 317-573-0979

Pioneer Standard (E. Ky.)
4433 Interpoint Blvd.
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

LOUISIANA

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Distributors

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
FAX - 214-343-5988

Hamilton/Avnet Electronics
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
FAX - 407-678-1878

Pioneer Electronics
13765 Beta Road
Dallas, TX 75244
Phone - 214-386-7300
FAX - 214-490-6419

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214-235-9953
FAX - 214-644-5064

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MAINE

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Wyle Laboratories
15 3rd Avenue
Burlington, MA 01803
Phone - 617-272-7300
FAX - 617-272-6809

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

MARYLAND

Representative

Electronic Engineering & Sales, Inc.
305 Kramer Road
Pasadena, MD 21122
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Hamilton/Avnet Electric
7172 Gateway Drive
Columbia, MD 21046
Phone - 301-995-3500
FAX - 301-995-3593

Pioneer Technologies
9100 Gaither Road
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

MASSACHUSETTS

Representative

Advanced Tech Sales, Inc.
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics, Inc.
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Hamilton/Avnet Electronics
10D Centennial Drive
Peabody, MA 01960
Phone - 508-531-7430
FAX - 508-532-9802

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Wyle Laboratories
15 3rd Avenue
Burlington, MA 01803
Phone - 617-272-7300
FAX - 617-272-6809

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone 617-246-8200
FAX - 617-246-8293

MICHIGAN

Representative

Rathsburg Associates Incorporated
34605 Twelve Mile Road
Farmington Hills, MI 48331-3263
Phone - 313-489-1500
FAX - 313-489-1480

Distributors

Hall-Mark Electronics Corporation
38027 Schoolcraft Road
Livonia, MI 48150
Phone - 313-462-1205
FAX - 313-462-1830

Hamilton/Avnet Electronics
2215 29th Street S.E., Space A-5
Grand Rapids, MI 49508
Phone - 616-243-8805
FAX - 616-531-0059

Pioneer Standard
4505 Broadmoor Avenue, S.E.
Grand Rapids, MI 49512
Phone - 616-698-1800
FAX - 616-698-1831

Pioneer Standard
44191 Plymouth Oaks Blvd., Suite 1300
Plymouth, MI 48170
Phone - 313-416-5800
FAX - 313-416-5811

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

MINNESOTA

Representative

High Technology Sales Associates
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
FAX - 612-844-9930

Distributors

Anthem Electronics Inc.
7646 Golden Triangle Drive, Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
FAX - 612-881-9461

Hamilton/Avnet Electronics
9800 Bren Road East, Suite 410
Minnetonka, MN 55343
Phone - 612-932-0600
FAX - 612-932-6711

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

MISSISSIPPI

Representative

Southeast Technical Group
Route 10, Box 368
Meridian, MS 39301
Phone - 601-485-7055
FAX - 601-485-7063

Distributors

Hall-Mark Electronics Corporation
4890 University Square
Business Center, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
FAX - 205-830-2565

Hamilton/Avnet Electronics
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
FAX - 407-678-1878

Pioneer Technologies
4835 University Square, Suite 5
Huntsville, AL 35818
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MISSOURI

Representative

Advanced Technical Sales
13755 St. Charles Rock Road
Bridgeton, MO 63044
Phone - 314-291-5003
FAX - 314-291-7958

Distributors

Hall-Mark Electronics Corporation
3783 Rider Trail South
Earth City, MO 63045
Phone - 314-291-5350
FAX - 314-291-0362

Hamilton/Avnet Electronics
739 Goddard Avenue
Chesterfield, MO 63005
Phone - 314-537-1600
FAX - 314-537-4248

Pioneer Standard
111 Westport Plaza, Suite 625
St. Louis, MO 63146
Phone - 314-542-3077
FAX - 314-542-3078

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MONTANA

Distributor

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, CA 94089
Phone - 408-743-3300
FAX - 408-745-6679

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEBRASKA

Representative

Advanced Technical Sales
601 North Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
FAX - 913-782-8641

Distributors

Hall-Mark Electronics Corporation
10809 Lakeview Drive
Lenexa, KS 66215
Phone - 913-888-4747
FAX - 913-888-0523

Hamilton/Avnet Electronics
1130 Thorndale Avenue
Bensenville, IL 60106
Phone - 708-860-7700
FAX - 708-860-8530

Wyle Laboratories
451 E. 124th Street
Thornton, CO 80241
Phone - 303-457-9953
FAX - 303-457-4831

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

NEVADA

Representatives

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315
San Jose, CA 95110
Phone - 408-452-8133
FAX - 408-452-8139

Quatra Associates (Clark County)
4645 S. Lakeshore Drive, Suite 1
Tempe, AZ 85282
Phone - 602-820-7050
FAX - 602-820-7054

Distributors

Anthem Electronics Incorporated
580 Menlo Drive, Suite 8
Rocklin, CA 95677
Phone - 916-624-9744
FAX - 916-624-9750

Hall-Mark Electronics Corporation
580 Menlo Drive, Suite 2
Rocklin, CA 95677
Phone - 916-624-9781
FAX - 916-961-0922

Wyle Laboratories
2951 Sunrise Blvd., Suite 175
Rancho Cordova, CA 95742
Phone - 916-638-5282
FAX - 916-638-1491

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEW HAMPSHIRE

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

NEW JERSEY

Representatives

Omega Electronics
2655 Interplex Drive, Suite 104
Trevose, PA 19053
Phone - 215-244-4000
FAX - 215-244-4104

Parallax, Inc.
734 Walt Whitman Road
Melville, NY 11747
Phone - 516-351-1000
FAX - 516-351-1606

Distributors

Anthem Electronics, Inc.
355 Business Center Drive
Horsham, PA 19044
Phone - 215-443-5150
FAX - 215-675-9875

Anthem Electronics, Inc.
26 Chapin Road, Unit K
Pine Brook, NJ 07058
Phone - 201-227-7960
FAX - 201-227-9246

Hall-Mark Electronics Corporation
Moorestown West Corporate Center
225 Executive Drive, Suite 5
Moorestown, NJ 08057
Phone - 609-235-1900
FAX - 609-235-3381

Hamilton/Avnet Electronics
1 Keystone Avenue, Bldg. #36
Cherry Hill, NJ 08003
Phone - 609-424-0100
FAX - 609-751-2552

Hamilton/Avnet Electronics
10 Lanidex Plaza West
Parsippany, NJ 07054
Phone - 201-575-3390
FAX - 201-575-5839

Hall-Mark Electronics Corporation
200 Lanidex Plaza, 2nd Floor
Parsippany, NJ 07054
Phone - 201-515-3000
FAX - 201-515-4475

Pioneer Standard
14A Madison Road
Fairfield, NJ 07006
Phone - 201-575-3510
FAX - 201-575-3454

Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
FAX - 215-674-3107

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

NEW MEXICO

Representative

Quatra Associates Incorporated
600 Autumnwood Place, S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
FAX - 505-292-2092

Distributors

Anthem Electronics Inc.
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
Phone - 602-966-6600
FAX - 602-966-4826

Hall-Mark Electronics Corporation
4637 South 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Hamilton/Avnet Electronics
7801 Academy Road N.E., Bldg. 1
Suite 204
Albuquerque, NM 87109
Phone - 505-345-0001
FAX - 505-345-1867

Wyle Laboratories
4141 E. Raymond Street, Suite 1
Phoenix, AZ 85040
Phone - 602-437-2088
FAX - 602-437-2124

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEW YORK

Representatives

Electra Sales Corporation
3000 Winston Road South, Bldg. E
Rochester, NY 14623
Phone - 716-427-7860
FAX - 716-427-0614

Electra Sales Corporation
1 Adler Drive
East Syracuse, NY 13057
Phone - 315-463-1248
FAX - 315-463-1717

Parallax, Inc.
734 Walt Whitman Road
Melville, NY 11747
Phone - 516-351-1000
FAX - 516-351-1606

Distributors

Anthem Electronics-Military
47 Mall Drive
Commack, NY 11725-5703
Phone - 516-864-6600
FAX - 516-493-2244

Anthem Electronics, Inc.
26 Chapin Road, Unit K
Pinebrook, NJ 07058
Phone - 201-227-7960
FAX - 201-227-9246

Hall-Mark Electronics Corporation
6605 Pittsford - Palmyra Road, Suite E8
Fairport, NY 14450
Phone - 716-425-3300
FAX - 716-425-7195

Hall-Mark Electronics Corporation
3075 Veterans Memorial Hwy.
Ronkonkoma, NY 11779
Phone - 516-737-0600
FAX - 516-737-0838

Hall-Mark Electronics Corporation
200 Lanidex Plaza, 2nd Floor
Parsippany, NJ 07054
Phone - 201-515-3000
FAX - 201-515-4475

Hamilton/Avnet Electronics
933 Motor Parkway
Hauppauge, NY 11788
Phone - 516-231-9800
FAX - 516-434-7426

Hamilton/Avnet Electronics
100 Elwood Davis Road
North Syracuse, NY 13212
Phone - 315-437-2641
FAX - 315-432-0740

Hamilton/Avnet Electronics
2060 Townline Road
Rochester, NY 14623
Phone - 716-292-0730
FAX - 716-292-0810

Pioneer Standard
68 Corporate Drive
Binghamton, NY 13904
Phone - 607-722-9300
FAX - 607-722-9562

Pioneer Standard
14A Madison Road
Fairfield, NJ 07006
Phone - 201-575-3510
FAX - 201-575-3454

Pioneer Standard
840 Fairport Park
Fairport, NY 14450
Phone - 716-381-7070
FAX - 716-381-5955

Pioneer Standard
60 Crossways Park West
Woodbury, NY 11797
Phone - 516-921-8700
FAX - 516-921-2143

Military Distributors

MAST Distributors, Inc.
710-2 Union Parkway
Ronkonkoma, NY 11779
Phone - 516-471-4422
FAX - 516-471-2040

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2110 Smithtown Avenue
Ronkonkoma, NY 11779
Phone - 516-737-4500
FAX - 516-737-4520

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

NORTH CAROLINA

Representative

Southeast Technical Group
700 N. Arendell Avenue
Zebulon, NC 27597
Phone - 919-269-5589
FAX - 919-269-5670

Distributors

Hall-Mark Electronics Corporation
5234 Green's Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
FAX - 919-878-8729

Hamilton/Avnet Electronics
5250 77 Center Drive, Suite 28
Charlotte, NC 28217
Phone - 704-527-2485
FAX - 704-527-8058

Hamilton/Avnet Electronics
3510 Spring Forest Road
Raleigh, NC 27604
Phone - 919-878-0810
FAX - 919-872-4435

Pioneer Technologies
2200 Gateway Center Blvd., Suite 215
Morrisville, NC 27560
Phone - 919-460-1530
FAX - 919-460-1540

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

NORTH DAKOTA

Representative

High Technology Sales Associates
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
FAX - 612-844-9930

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Drive, Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
FAX - 612-881-9461

Hamilton/Avnet Electronics
1130 Thorndale Avenue
Bensenville, IL 60106
Phone - 708-860-7700
FAX - 708-860-8530

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

OHIO

Representatives

Scott Electronics, Inc.
Corporate Headquarters
3131 S. Dixie Drive, Suite 200
Dayton, OH 45439-2223
Phone - 513-294-0539
FAX - 513-294-4769

Scott Electronics, Inc.
360 Alpha Park
Cleveland OH 44143-2240
Phone - 216-473-5050
FAX - 216-473-5055

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Scott Electronics, Inc.
10901 Reed-Hartman Hwy., Suite 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
FAX - 513-791-8059

Distributors

Hall-Mark Electronics Corporation
5821 Harper Road
Solon, OH 44139
Phone - 216-349-4632
FAX - 216-248-4803

Hall-Mark Electronics Corporation
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Hamilton/Avnet Electronics
2600 Corporate Exchange Drive, Suite 180
Columbus, OH 43231
Phone - 614-882-7004
FAX - 614-882-8650

Hamilton/Avnet Electronics
7760 Washington Village Drive
Dayton, OH 45459
Phone - 513-439-6700
FAX - 513-439-6711

Hamilton/Avnet Electronics
2 Summit Park Drive, Suite 520
Independence, OH 44131
Phone - 708-860-7700
FAX - 708-860-8530

Pioneer Standard
4800 E. 131st Street
Cleveland, OH 44105
Phone - 216-587-3600
FAX - 216-587-3906

Pioneer Standard
4433 Interpoint Blvd.
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

Pioneer Standard
6421 E. Main Street, Suite 201
Reynoldsburg, OH 43608
Phone - 614-221-0043
FAX - 614-759-1955

Military Distributors

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

OKLAHOMA

Representative

Nova Marketing Incorporated
8125 E. 51st Street, Suite 1339
Tulsa, OK 74145
Phone - 918-660-5105
FAX - 918-665-3815

Distributors

Hall-Mark Electronics Corporation
5411 S. 125th East Avenue, Suite 305
Tulsa, OK 74146
Phone - 918-254-3200
FAX - 918-254-6207

Hamilton/Avnet Electronics
12101 East 51st Street, Suite 106
Tulsa, OK 74146
Phone - 918-664-0444
FAX - 918-250-8763

Pioneer Standard
4110 South 100th East Avenue, Suite 100
Tulsa, OK 74146
Phone - 918-665-7840
FAX - 918-665-1891

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

OREGON

Representative

Westerberg & Associates
7165 S.W. Fir Loop
Portland, OR 97223
Phone - 503-620-1931
FAX - 503-684-5376

Distributors

Anthem Electronics Incorporated
9090 S.W. Gemini Drive
Beaverton, OR 97005
Phone - 503-643-1114
FAX - 503-626-7928

Hamilton/Avnet Electronics
9750 S.W. Nimbus Avenue
Beaverton, OR 97005
Phone - 503-526-6200
FAX - 503-641-5939

Wyle Laboratories
9640 Sunshine Court, Suite 200, Bldg. G
Beaverton, OR 97005
Phone - 503-643-7900
FAX - 503-646-5466

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

PENNSYLVANIA

Representatives

Omega Electronic Sales Incorporated
2655 Interplex Drive, Suite 104
Trevose, PA 19053
Phone - 215-244-4000
FAX - 215-244-4104

Scott Electronics, Inc. (W. PA)
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Distributors

Anthem Electronics, Inc.
355 Business Center Drive
Horsham, PA 19044
Phone - 215-443-5150
FAX - 215-675-9875

Hall-Mark Electronics Corporation
Moorestown W. Corporate Center
225 Executive Drive, Suite 5
Moorestown, NJ 08057
Phone - 609-235-1900
FAX - 609-235-3381

Hall-Mark Electronics Corporation (W. PA)
5821 Harper Road
Solon, OH 44139
Phone - 216-349-4632
FAX - 216-248-4803

Hamilton/Avnet Electronics
213 Executive Drive, Suite 320
Mars, PA 16046
Phone - 412-281-4150 (Mars)
Phone - 814-455-6767 (Erie)
FAX - 412-772-1890

Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
FAX - 215-674-3107

Pioneer Technologies (W. PA)
259 Kappa Drive
Pittsburgh, PA 15238
Phone - 412-782-2300
FAX - 412-963-8255

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

PUERTO RICO

Representative

Photon Sales, Inc.
1600 Sarno Road, Suite 21
Melbourne, FL 32935
Phone - 407-259-8999
FAX - 407-259-1323

Distributor

Hamilton/Avnet Electronics
Villas De San Francisco Plaza
#87 De Diego Avenue, Suite 215
Rio Piedras, PR 00926
Phone - 809-731-1110
FAX - 809-754-4350

RHODE ISLAND

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
61 Mattatuck Heights
Waterbury, CT 06705
Phone - 203-575-1575
FAX - 203-596-3232

Hall-Mark Electronics Corporation
125 Commerce Court, Unit 6
Cheshire, CT 06410
Phone - 203-271-2844
FAX - 203-272-1704

Pioneer Standard
112 Main Street
Norwalk, CT 06851
Phone - 203-853-1515
FAX - 203-838-9901

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

SOUTH CAROLINA

Representative

Southeast Technical Group
700 N. Arendell Avenue
Zebulon, NC 27597
Phone - 919-269-5589
FAX - 919-269-5670

Distributors

Hall-Mark Electronics Corporation
5234 Green's Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
FAX - 919-878-8729

Pioneer Technologies
9401 L. Southern Pine Blvd.
Charlotte, NC 28273
Phone - 704-526-8188
FAX - 704-522-8564

Pioneer Technologies
2810 Meridian Parkway, Suite 148
Durham, NC 27713
Phone - 919-544-5400
FAX - 919-544-5885

Military Distributor

Zeus Components, Inc.
1750 West Broadway, Suite 114
Oviedo, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

SOUTH DAKOTA

Representative

High Technology Sales Associates
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
FAX - 612-844-9930

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Drive, Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
FAX - 612-881-9461

Hamilton/Avnet Electronics
1130 Thorndale Avenue
Bensenville, IL 60106
Phone - 708-860-7700
FAX - 708-860-8530

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

TENNESSEE

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
Phone - 205-534-2376
FAX - 205-534-2384

Distributors

Hall-Mark Electronics Corporation
4890 University Square
Business Center, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
FAX - 205-830-2565

Hamilton/Avnet Electronics
3425 Corporate Way, Suite G
Duluth, GA 30136
Phone - 800-241-6928
FAX - 404-446-1011

Pioneer Technologies
4835 University Square, Suite 5
Huntsville, AL 35818
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

TEXAS

Representatives

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Nova Marketing Incorporated
9207 Country Creek, Suite 141
Houston, TX 77036
Phone - 713-988-6082
FAX - 713-774-1014

Nova Marketing Incorporated
8310 Capitol of Texas Hwy. North, Suite 180
Austin, TX 78731
Phone - 512-343-2321
FAX - 512-343-2487

Quatra Associates, Inc. (El Paso, TX)
600 Autumnwood Place, S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
FAX - 505-292-2092

Distributors

Anthem Electronics, Inc.
651 N. Plano Road, Suite 429
Richardson, TX 75081
Phone - 214-238-7100
FAX - 214-238-0237

Hall-Mark Electronics Corporation
12211 Technology Blvd.
Austin, TX 78727
Phone - 512-258-8848
FAX - 512-258-3777

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
FAX - 214-343-5988

Hall-Mark Electronics Corporation
8000 Westglen
Houston, TX 77063
Phone - 713-781-6100
FAX - 713-953-8420

Hamilton/Avnet Electronics
1826 F Kramer Lane
Austin, TX 78758
Phone - 512-837-8911
FAX - 512-832-4315

Hamilton/Avnet Electronics
4004 Beltline Road, Suite 200
Dallas, TX 75244
Phone - 214-308-8111
FAX - 214-308-8109

Hamilton/Avnet Electronics
1235 North Loop West, Suite 521
Houston, TX 77008
Phone - 713-240-7733
FAX - 713-861-6541

Pioneer Electronics
13765 Beta Drive
Dallas, TX 75244
Phone - 214-419-5503
FAX - 214-490-6419

Pioneer Standard
1826 Kramer Lane, Suite D
Austin, TX 78758
Phone - 512-835-4000
FAX - 512-835-9829

Pioneer Standard
10530 Rockley Road, Suite 100
Houston, TX 77099
Phone - 713-495-4700
FAX - 713-495-5642

Wyle Laboratories
4030 W. Braker Lane, Suite 420
Austin, TX 78759
Phone - 512-345-8853
FAX - 512-834-0981

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214-235-9953
FAX - 214-644-5064

Wyle Laboratories
11001 S. Wilcrest, Suite 100
Houston, TX 77099
Phone - 713-879-9953
FAX - 713-879-6540

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

UTAH

Representative

Wescom Marketing
3500 S. Main, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801-269-0665

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Corporation
12503 E. Euclid Drive, Suite 20
Englewood, CO 80111
Phone - 303-790-1662
FAX - 303-790-4991

Hamilton/Avnet Electronics
1100 East 6600 South, Suite 120
Salt Lake City, UT 84121
Phone - 801-263-0104
FAX - 213-558-2845

Wyle Laboratories
1325 West 2200 South, Suite E
Salt Lake City, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

VERMONT

Representative

Advanced Tech Sales Incorporated
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 508-667-0902
FAX - 508-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

VIRGINIA

Representative

Electronic Engineering & Sales, Inc.
305 Kramer Road
Pasadena, MD 21122
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Pioneer Technologies
9100 Gaither Drive
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

WASHINGTON

Representative

Westerberg & Associates
12505 N.E. Bel-Red Road, Suite 112
Bellevue, WA 98005
Phone - 206-453-8881
FAX - 206-453-8758

Distributors

Anthem Electronics Incorporated
19017-120th Avenue N.E., Suite 102
Bothell, WA 98011
Phone - 206-483-1700
FAX - 206-486-0571

Hall-Mark Electronics Corporation
250 N.W. 39th, Suite 4
Seattle, WA 98107
Phone - 206-547-0415
FAX - 206-632-4814

Hamilton/Avnet Electronics
545 West 2925 North
Goldie Road, Unit B
Oak Harbor, WA 98277
Phone - 206-679-5576
FAX - 206-675-5770

Hamilton/Avnet Electronics
17761 N.E. 78th Place, Bldg. C
Redmond, WA 98052
Phone - 206-881-6697
FAX - 206-867-0159

Wyle Laboratories
15385 N.E. 90th Street
Redmond, WA 98052-3522
Phone - 206-881-1150
FAX - 206-881-1567

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

WEST VIRGINIA

Representative

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Distributor

Hall-Mark Electronics Corporation
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

WISCONSIN

Representatives

High Technology Sales Associates (E. WI)
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
FAX - 612-844-9930

Industrial Representatives, Inc. (W. WI)
16745 W. Bluemound Road, Suite 340
Brookfield, WI 53005
Phone - 414-789-9393
FAX - 414-789-9272

Distributors

Anthem Electronics, Inc.
1300 Remington, Suite A
Schaumburg, IL 60173
Phone - 708-884-0200
FAX - 708-884-0480

Hall-Mark Electronics Corporation
210 Mittle Drive
Wood Dale, IL 60191
Phone - 708-860-3800
FAX - 708-860-0239

Hall-Mark Electronics Corporation
16255 West Lincoln Avenue
New Berlin, WI 53151
Phone - 414-797-7844
FAX - 414-797-9259

Hamilton/Avnet Electronics
20875 Crossroads Circle, Suite 400
Waukesha, WI 53186
Phone - 414-784-4510
FAX - 414-784-9509

Pioneer Standard
120 Bishops Way, Suite 163
Brookfield, WI 53005
Phone - 414-784-3480
FAX - 414-784-8207

Military Distributors

Zeus Components, Inc.
100 Midland Avenue
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Suite 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

WYOMING

Representative

Wescom Marketing
3500 South Main, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801- 269-0665

Distributors

Anthem Electronics Incorporated
373 Inverness Drive
Englewood, CO 80112
Phone - 303-790-4500
FAX - 303-790-4532

Wyle Laboratories
1325 West 2200 South, Suite E
West Valley, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, CA 94089
Phone - 408-743-3300
FAX - 408-745-6679

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Avenue, Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

AUSTRALIA

Representative

Reptechnic Pty. Ltd.
3/36 Bydown Street
Neutral Bay NSW 2089
Phone - 612-953-9844
FAX - 612-953-9683

AUSTRIA

Representative & Distributor

Thomas Neuroth GmbH
Hietzinger Hauptstrasse 22/A/2
A-1130 Wien
Phone - 431-877-5645
FAX - 431-876-4920

BELGIUM

Representative & Distributor

Microtron
Generaal Dewittelaan
2800 Mechelen
Phone - 32-15-212223
FAX - 32-15-210069

DENMARK

Representative

Delco A/S
Mejeribakken 8
3540 Lynge
Phone - 45-42-18-95-33
FAX - 45-42-18-95-30

Distributor

E.V. Johanssen Elektronik A/S
Titangade 15
DK-2200 Copenhagen N
Phone - 45-31-83-90-22
FAX - 45-31-83-92-22

FINLAND

Representative & Distributor

Integrated Electronics OY AB
Turkhaudantie 1
P.O. Box 160
SF-00700 Helsinki
Phone - 358-0-351-3133
FAX - 358-0-351-3134

FRANCE

Representative

Rep'Tronic S.A.
1 Bis, rue Marcel Paul
Bâtiment A
Z.I la Bonde
91300 Massy
Phone - 33-1-60-13-93-00
FAX - 33-1-60-13-91-98

Distributors

Arrow Electronique S.A.
73-79, rue des Solets
Silic 585
94663 Rungis Cedex
Phone - 33-1-49-78-4848
FAX - 33-1-49-78-0699

Avnet EMG SA
79, rue Pierre Semard
92320 Chatillon
Phone - 33-1-49-65-2600
FAX - 33-1-49-65-2649

Paris Sud Electronique Composants
12, rue René Cassin
91300 Massy
Phone - 33-1-69-20-6699
FAX - 33-1-69-20-7532

Thomson Composants Distribution
30, Avenue de l'Epi d'Or
94807 Villejuif, Cedex
Phone - 33-1-46-87-2224
FAX - 33-1-46-87-0711

GERMANY

Sales & Customer Service Office

Micron Semiconductor (Deutschland) GmbH
Marsstrasse 3
D-8011 Aschheim
Phone - 49-89-903-0021
FAX - 49-89-904-3114

Representative & Distributor

EBV Elektronik GmbH
Hans-Pinsel-Str. 4
D-8013 Haar b. München
Phone - 49-89-4-60-96-0
FAX - 49-89-46-44-88

Distributors

Metronik GmbH
Leonhardsweg 2
D-8025 Unterhaching b. München
Phone - 49-89-611-08-0
FAX - 49-89-611-22-46

Neumüller Elektronik GmbH
Eschenstrasse 2
Postfach 1250
D-8028 Taufkirchen
Phone - 49-89-612-08-0
FAX - 49-89-612-08-248

HONG KONG

Sales & Customer Service Office

Micron Semiconductor, Inc.
Apt. A, 15/F, Block 3
Pacific View, 38 Tai Tam Road
Phone - 852-813-5075
FAX - 852-813-5914

Representative

Lestina International Ltd.
14/F, Park Tower
15 Austin Road
Tsimshatsui
Phone - 852-735-1736
FAX - 852-730-5260

INDIA

Distributor

Silicon Electronics
1148 Sonora Court
Sunnyvale, CA 94086
Phone - 408-738-8235
FAX - 408-738-0698

INDONESIA

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

IRELAND

Representative

New England Technical Sales
The Diamond
Malahide County Dublin
Phone - 353-18-450635
FAX - 353-18-453625

Distributor

Lyco Ltd.
Estuary House
New Street
Malahide, Dublin
Phone - 353-18-452-020
FAX - 353-18-451-741

ISRAEL

Representative & Distributor

C.R.G. Electronics Ltd.
29 Hagaaton Str.
P.O.B. 154
Nahariya 22100
Phone - 972-4-925-819
FAX - 972-4-924-065

ITALY

Representative & Distributor

Claitron SPA
Via Gallarate, 211
20151 Milano
Phone - 39-2-33-40-40-00
FAX - 39-2-38-00-14-14

Distributor

EUR Elettronica S.p.A.
Via E. Fermi, 8
20094 Assago
Milano
Phone - 39-2-45-78-41
FAX - 39-2-48-80-27-5

JAPAN

Distributor

Sanyo Electronic Co. Ltd.
Import Promotion Division
1-1-10 Ueno
Taito-ku, Tokyo 110
Phone - 81-3-3837-6346
FAX - 81-3-3837-6379

KOREA

Sales & Customer Service Office

Micron Semiconductor, Inc.
Block 3, 15/F, Apt. A
Pacific View, 38 Tai Tam Road
Hong Kong
Phone - 852-813-5075
FAX - 852-813-5914

Representative

I & C Microsystems Co. Ltd.
3rd Floor, Jungnem Bldg.
191-3 Poi-Dong
Kangnam-Ku
Seoul
Phone - 822-577-9131
FAX - 822-577-9130

MALAYSIA

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

THE NETHERLANDS

Representative & Distributor

Microtron
Postbus 188
1243 ZK's Graveland
Phone - 31-35-61834
FAX - 31-35-62709

NEW ZEALAND

Representative

Reptechnic
3/36 Bydown Street
Neutral Bay, NSW 2089
Australia
Phone - 612-953-9844
FAX - 612-953-9683

NORWAY

Representative & Distributor

BIT Elektronikk A/S
Smedsvigen 4
P.O. Box 194
1364 Hvalstad
Phone - 47-2-981370
FAX - 47-2-981371

PHILLIPINES

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

PORTUGAL

Representative & Distributor

ATD Electrónica, LDA.
Rua Drive Faria de Vasconcelos, 3-A
1900 Lisboa
Phone - 351-1-847-2200
FAX - 351-1-847-2197

SINGAPORE

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

SOUTH AFRICA

Distributor

Computer Parts cc
CNR Athol and Louis Botha Avenue
Highlands North
Johannesburg 2192
Phone - 27-11-887-2438
FAX - 27-11-887-2514

SPAIN

Representative & Distributor

ATD Electronica, S.A.
Avda. de la Industria 32
Nave 17, 2o B.
28100 Alcobendas
Madrid
Phone - 341-661-6551
FAX - 341-661-6300

SWEDEN

Representative & Distributor

IE Komponenter AB
Box 11 113
S-161 11 Bromma
Phone - 46-8-804685
FAX - 46-8-262286

SWITZERLAND

Representative & Distributor

Alltron AG
Hintermättlistrasse 3
5506 Mägenwil
Phone - 41-64-56-00-00
FAX - 41-64-56-00-05

TAIWAN, R.O.C.

Representative

ASEC International Corporation
4F, 223, Chung Yang Road
Nan Kang District
Taipei
Phone - 886-2-786-6677
FAX - 886-2-651-0060

THAILAND

Representative

Desner Electronics (FE) Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
FAX - 65-284-9466

UNITED KINGDOM

Sales & Customer Service Office

Micron Europe Limited
Centennial Court
Easthampstead Road
Bracknell
Berkshire RG12 1JA
Phone - 44-344-360055
FAX - 44-344-869504

Representatives

Cedar Technologies U.K. Ltd.
The Old Water Works
Howse Lane
Bicester
Oxon OX6 8XF
Phone - 44-869-322366
FAX - 44-869-322377

Distributors

Abacus Electronics Ltd.
Abacus House
Bone Lane
Newbury
Berkshire RG14 5SF
Phone - 44-635-36222
FAX - 44-635-38432

Bytech Components Ltd.
12 A Cedarwood
Chineham Business Park
Crockford Lane
Basingstoke
Hampshire RG24 OWD
Phone - 44-256-707107
FAX - 44-256-707162

Thame Components Ltd.
Thame Park Road
Thame
Oxfordshire OX9 3UQ
Phone - 44-844-261188
FAX - 44-844-261681

MICRON

MICRON

Micron Semiconductor, Inc.
2805 East Columbia Road
Boise, Idaho 83706
Tel: (208) 368-3900
Fax: (208) 368-4431
Customer Comment Line:
800-932-4992 (USA)
01-208-368-3410 (Intl.)

Micron Europe Limited
Centennial Court
Easthampstead Road
Bracknell
Berkshire RG12 1JA
United Kingdom
Tel: 44-344-360055
Fax: 44-344-869504

Micron Semiconductor
(Deutschland) GmbH
Marsstrasse 3
D-8011 Aschheim
Germany
Tel: 49-89-903-0021
Fax: 49-89-904-3114

Micron Semiconductor, Inc.
Block 3, 15/F, Apt. A
Pacific View
38 Tai Tam Road
Hong Kong
Tel: 852-813-5075
Fax: 852-813-5914

MICRON
SEMICONDUCTOR, INC.